

17 June 2005

To: Paul Philp
DOE Project Manager, Run IIb CDF Detector Project

From: Pat Lukens
Project Manager for the Run IIb CDF Detector Project

Subject: Run IIb CDF Detector Project May 2005 Report

Attached is the monthly report summarizing the May 2005 activities and progress for the Fermilab RunIIb CDF Detector Project. This report is available electronically at:

<http://www-cdf.fnal.gov/run2b.html>

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RunIIb CDF Detector Project
Progress Report No. 30
1 - 31 May 2005

I. PROJECT DESCRIPTION

The primary goal of the CDF Run IIb Detector Project is to enable the detector to exploit the physics opportunities available during Tevatron operation through 2008. The data from Run II will represent a set of detailed measurements that can be compared with the predictions of the Standard Model at the highest available collision energy. The increased size of the data sample will allow us to study the top quark by measuring the details of its production and decay mechanism. In addition, we plan precision electroweak and QCD measurements, continued searches for a variety of phenomena that are predicted to exist beyond the Standard Model framework, and to explore CP violation in the b quark sector. The detailed physics goals of the upgrade are described in the Technical Design Report (TDR).

The major tasks of this upgrade are:

- Upgrade the calorimeter by replacing the Central Preradiator Chamber with a device with shorter response time to allow operation in a high-luminosity environment, and adding timing information to the electromagnetic calorimeters.
- Upgrade the data acquisition and trigger systems to increase throughput needed for higher luminosity operation and efficiently trigger on the higher multiplicity events of Run IIb.

II. OVERVIEW OF PROJECT STATUS – P. Lukens

The project made steady progress during May, 2005. The completion of the projects allowed the cost codes used for the calorimeter upgrades to be closed. The project is estimating that all components that require collision hall access for installation will be available by 5 Sept. 2005.

A review of contingency needs was performed during May, and presented to staff of the Office of Science. A reduction of the total project cost is being considered as a result of this reevaluation. Documentation for this action is being developed at this time.

III. PROJECT MILESTONE SUMMARY (as of 31 May 2005)

CDF Data Acquisition & Trigger (L1 and L2) Milestones Sorted by Baseline Completion Date

WBS	Title	Baseline Comp. Date	Forecast/Actual Completion Date	Complete
1.3.2.6.3	Begin production of Level 2 Pulsar system	12 Nov 03	12 Nov 03	Yes
1.3.1.6.6	First Prototype TDC available for testing	19-Nov-03	16-Feb-04	Yes
1.3.4.4.1.4	Prototype Event Builder hardware arrives	3-Jun-04	31 Mar 04	Yes
1.3.2.10	Pulsar Hardware Ready for Installation	31-Aug-04	20-Aug-04	Yes
1.3.6.1.1.7	Begin AMS Design Work	1-Sept-04	2-Aug-04	Yes
1.3.6.1.3.7	Begin Track Fitter Design	1-Sept-04	2-Aug-04	Yes
1.3.4.5.3	Production Readiness Review - Event Builder	4-Oct-04	2-Jun-04	Yes
1.3.4.5.4.4	Arrival of the Event Builder hardware	15-Oct-04	15-Oct-04	Yes
1.3.11.8.5.5	Begin Purchase of Pulsar Board components	20-Oct-04	4-Nov-04	Yes
1.3.11.5.3.8	Begin Production TDC Mezzanine Card	28-Oct-04	3-Nov-04	Yes
1.3.6.2.6.4	Begin Amp Chip Production	10-Jan-05	22-Nov-04	Yes
1.3.6.2.1.1.5	Begin AMS Mezzanine Card Production	14-Jan-05	11-Nov-04	Yes
1.3.1.17.4	TDC Readout System Complete	21-Jan-05	10-Dec-04	Yes
1.3.11.6.3.6	Receipt of TDC to Finder cables complete	18-Mar-05	7-July-05	
1.3.5.3.7	Arrival of 15 PCs from the vendor	23-Mar-05	18-Mar-05	Yes
1.3.2.9	Pulsar Level 2 subproject ready for installation	1-Apr-05	11-Mar-05	Yes
1.3.11.8.8	Begin Joint Testing with Finder Board	4-Apr-05	2-May-05	
1.3.11.7.5.8	Begin Production of SLAM Boards	18-Apr-05	8-Jun-05	
1.3.11.4.4.8	Begin Production TDC Fiber Transition Boards	21-Apr-05	31-May-05	Yes
1.3.11.5.3.9	Checkout of TDC Mezzanine Cards Complete	6-Jun-05	5-Jul-05	
1.3.11.2.5.1	Begin Production XFT Finder Boards	8-Jun-05	31-May-05	Yes
1.3.6.1.2.5	Hit Buffer Firmware Complete for Board Test	23-Jun-05	13-Jul-05	
1.3.6.1.3.5	Track Fitter Firmware Complete for Board Test	28-Jun-05	20-Apr-05	Yes
1.3.1.12.6	Installation of Modified TDC's Complete	27-July-05	31-Aug-05	
1.3.4.8	Finish Event-Builder Upgrade	28-July-05	29-Jun-05	
1.3.10.2	Ready for Accelerator Shutdown 2005	8-Aug-05	9-Sept-05	
1.3.1.12.8	TDC Modification Complete	10-Aug-05	15-Sept-05	
1.3.5.5.5	Arrival of 70 Level3 and 15 DAQ PCs	15-Aug-05	18-Mar-05	Yes
1.3.5.6.5	Arrival of 192 L3 Farm PC's from the vendor	15-Aug-05	29-Aug-05	
1.3.6.1.1.5	AMS Firmware Complete for Board Test	19-Aug-05	14-Apr-05	Yes
1.3.6.3	SVT ready for installation	25-Aug-05	28-Sept-05	
1.3.5.8	Finish Purchase of Computers for L3 DAQ system	6-Sept-05	20-Sept-05	
1.3.11.4.4.9	Checkout of TDC Transition Boards Complete	16-Sept-05	9-Sept-05	
1.3.11.7.5.9	Checkout of SLAM Boards Complete	28-Sept-05	6-Oct-05	
1.3.11.2.5.10	Finder Board Checkout Complete	29-Sept-05	16-Nov-05	
1.3.11.10	XFT Ready for Installation at CDF	29-Sep-05	16-Nov-05	
1.3.8	Finish Run 2b Trigger DAQ project	30-Sep-05	16-Nov-05	
1.3.9	DAQ and Trigger Upgrades Ready for Installation	17-Jan-06	16-Nov-05	

CDF Project Run IIb Data Acquisition & Trigger Milestones (Level 1 and 2)

Name	Forecast	Baseline	Variance	2005								2006	
				Q3	Q4	Q1	Q2	Q3	Q4	Q1			
Event Builder Production Readiness Review	6/2/04	10/4/04	-17 wks	★	◆								
Begin AMS Design Work	8/2/04	9/1/04	-4.4 wks		★◆								
Begin Track Fitter Design	8/2/04	9/1/04	-4.4 wks		★◆								
Pulsar Hardware Ready for Installation	8/20/04	8/31/04	-1.4 wks		★◆								
Arrival of the Event Builder hardware	10/15/04	10/15/04	0 wks			◆							
Begin Production TDC Mezzanine Card	11/3/04	10/28/04	0.8 wks			◆							
Begin Purchase of Pulsar Board components	11/4/04	10/20/04	2 wks			◆★							
Begin AMS Mezzanine Card Production	11/11/04	1/14/05	-8.2 wks			◆★	◆						
Begin Ampchip Production	11/22/04	1/10/05	-5.8 wks			◆★	◆						
Pulsar Level 2 subproject ready for installation	3/11/05	4/1/05	-3 wks					◆★					
Arrival of 70 Level3 and 15 DAQ PCs from the vendor	3/18/05	8/15/05	-21 wks					◆★			◆		
Arrival of 15 PCs from the vendor	3/18/05	3/23/05	-0.6 wks					◆					
AMS Firmware Complete for Board Test	4/14/05	8/19/05	-18 wks					◆★			◆		
Track Fitter Firmware Complete for Board Test	4/20/05	6/28/05	-9.8 wks					◆★			◆		
Begin Joint Testing with Finder Board	5/2/05	4/4/05	3.8 wks					◆	◇				
Begin Production TDC Fiber Transition Boards	5/31/05	4/21/05	5.2 wks					◆	◆★				
Begin Production XFT Finder Boards	5/31/05	6/8/05	-1.4 wks					◆	◆				
Begin Production of SLAM Boards	6/8/05	4/18/05	7 wks					◆	◇				
Finish Event-Builder Upgrade	6/29/05	7/28/05	-4 wks							◇	◆		
Checkout of TDC Mezzanine Cards Complete	7/5/05	6/6/05	4 wks							◆	◇		
Receipt of TDC to Finder cables Complete	7/7/05	3/18/05	15.4 wks					◆		◇	◇		
Hit Buffer Firmware Complete for Board Test	7/13/05	6/23/05	2.4 wks							◆	◇		
Arrival of 192 L3 farm PCs from the vendor	8/29/05	8/15/05	2 wks								◆	◇	
Installation of Modified TDC's Complete	8/31/05	7/27/05	5 wks								◆	◇	
TDC Modification Complete	9/15/05	8/10/05	5 wks								◆	◇	
Ready for Accelerator Shutdown 2005	9/19/05	8/8/05	6 wks								◆	◇	
Checkout of TDC Transition Boards Complete	9/19/05	9/16/05	0.2 wks									◆	
Finish Purchase of Computers for Level3/DAQ system	9/20/05	9/6/05	2 wks									◆	◇
SVT ready for installation	9/28/05	8/25/05	4.6 wks									◆	◇
Checkout of SLAM Boards Complete	10/6/05	9/28/05	1.2 wks									◆	◇
Finder Board Checkout Complete	11/16/05	9/29/05	6.7 wks									◆	◇
XFT Ready for Installation at CDF	11/16/05	9/29/05	6.7 wks									◆	◇
Finish Run 2b Trigger DAQ project	11/16/05	9/30/05	6.7 wks									◆	◇
Data Acquisition and Trigger Upgrades Ready to Install	11/16/05	1/17/06	-7.3 wks									◆	◇

Status Date: 5/31/05
Print Date: 6/9/05

Completed Milestone ★
Current Forecast ◇

Baseline Milestone ◆

IV. PROCUREMENT – P. Lukens

Several large procurements were placed for the production quantity components used for the Finder boards (a portion of the track trigger).

V. PROJECT HIGHLIGHTS

1.3 – Data Acquisition and Trigger

1.3.1 TDC (Time to Digital Converter) – Eric James

TDC modification continues at a rate of about 10 boards per week when boards are available. Due to a lack of access opportunities for removing boards from the detector, the rate of board modifications in May was lower than normal. A total of 126 boards out of 300 to be modified were completed by the end of the month. Modified boards have been installed in six of the twenty COT TDC crates. The newly installed boards have performed well and have not had a negative impact on normal detector operations. XTC II mezzanine cards (one component of the XFT upgrade) are now installed on the appropriate TDC boards in three of the COT crates containing modified boards. Installation of the XTC II cards will proceed in step with the installation of modified TDC boards in the remaining eleven COT crates. At the end of May, we were preparing to install three crates worth of TDC's during a scheduled shutdown in mid-June.

Month	Board Modification		Testing at Michigan		Detector Installation	
	Complete	Remaining	Complete	Remaining	Complete	Remaining
January	39	261	9	291	0	233
February	61	239	43	257	21	212
March	98 (33%)	202	65 (22%)	235	42 (18%)	191
April	116 (39%)	184	80 (27%)	220	69 (30%)	164
May	126 (42%)	174	109 (36%)	191	69 (30%)	164

1.3.11 XFT (eXtremely Fast Tracker) II – Richard Hughes, Brian Winer, Kevin Pitts

All components of the XFT II system underwent a production readiness review at the end of May. The review committee felt that all of the boards were ready to start production and recommended proceeding with production as fast as possible.

Stereo Linker Association Module (SLAM) Boards: A significant amount of work was done to speed up Linker board firmware timing, which is needed for the SLAM algorithm to complete on time. We managed to speed this up by ~300nsec, which is an increase of almost a factor of 2. This timing was tested using the OSU test stand.

Work began to synchronize Linker tracks with stereo finder pixels on the SLAM board (using a separate SLAM board to drive the Finder stereo pixels). We also worked on test stand software to drive the full set of SLAM test vectors (finer pixels mostly) through the SLAM board.

XTC: Production testing and burn-in continues in Urbana. Boards are then shipped to Fermilab to be tested on TDCs. On May 5, the first production XTC's were installed onto the CDF detector. These boards have been successfully read-out and calibrated. At the end of May, 3 of the 20 COT crates were fully instrumented with XTC boards. XTC checkout is easily able to keep up with TDC replacement. We anticipate having more than 50% of the detector instrumented with XTC boards by the end of June.

TDC Transition Module: Preproduction boards were received in mid-May and have been undergoing check-out. No problems have been found, and we have successfully captured XTC data via fiber optic in the prototype Finder board. Additional tests are ongoing to use a Pulsar board to receive data from the TDC TM. The order to fabricate the production quantity of boards was submitted.

Cabling: Evaluation of the first delivered fibers continued in May. The assembler identified some difficulties with putting the connectors on the fibers due to the mechanical characteristics of the fiber. All components are within specification and after thorough investigation and testing the sample cables it was determined that the fibers should perform to specification. At the end of the month, the assembler was released to assemble one half of the fibers. These will be tested before releasing the remaining production.

Stereo Finder: Testing of the Stereo Finder continued with emphasis on high statistics tests sending and capturing data. Most of the capture tests involve the Finder acting as both data source and receiver. Tests with up to 10^{11} bits sent and no errors detected were performed. Continuing data capture tests with the TDC transition card as source and more realistic timing structure revealed some data errors. Investigation of these errors points to some data synchronization problems with some firmware.

Other tests during May included: capturing data in the L2 buffers, turning on track segment patterns with input hit data and measurements of processing latency. The latency was measured for input from the TDC transition card (including fiber), data processing on the board and transmission to the SLAM board. All timing is within specifications.

While the first version Finder board was under test the design of the 2nd version was being completed. By the end of May the board layout was completed. Requisitions were written for all parts needed for full production of the Finder, Rx mezzanine cards, and Tx Mezzanine cards. The bid package and requisition for the Finder PCB fabrication and assembly were submitted. Following the production readiness review, orders were placed for the bulk of the components. It is anticipated that the remaining orders will be placed in early June.

1.3.4 Event Builder – Bruce Knuteson

A readiness review was held during May to understand how best to commission the Event Builder upgrade. All pieces are in place and regular tests are being conducted in the CDF control room. We will make use of end-of-store studies over the next few weeks to test increasingly large slices of the system. Our test of a low-cost D-link switch to handle the networking between the Level 3 converter nodes and the Level 3 processor nodes was successful. An order has been placed for 19 additional switches. The remaining VMIC boards, ordered for an anticipated expansion in the number of CDF DAQ VRB crates, have arrived at Fermilab.

1.3.5 Level 3 computers upgrade – Pat Lukens

The scope change proposed at the April PMG was approved, and the baseline has been changed to reflect this. Bid package documentation was developed during May for the procurement of Level 3 computers. Several meetings were held to accomplish this, both with computing experts within the experiment, and the Fermilab Procurement department.

1.3.6 SVT (Silicon Vertex Tracker) – Alberto Annovi

Software: All the work on simulation, SVTVME, and monitoring is going according to the plan. We will have to re-evaluate some parameters for the 128k pattern configuration for the AM++ in order to increase the efficiency a little bit. We have decided to write the "parasitic" track data from the vertical slice test in the SVDD bank so we are updating our offline monitor program to accommodate that.

AM++ and AMS/RW: Extensive tests have been run with a fully loaded AM++ board. A total of 16 AM++ and 24 LAMB boards have been produced and are ready to be assembled. The input and output spy buffers have been implemented in the AMS/RW and the DAQ buffers have been added. The truncated output has been implemented. A test run has been successfully executed taking data from the parallel vertical slice test. A copy of input data for one SVT wedge has been sent to and analyzed by the new boards. The results have been sent back to downstream electronics. Monitoring histograms have been produced.

Hit Buffer: Three groups working on HB implementation started to write and validate firmware with simulation and board tests. For the control chip (called HB0 in the RunIIb upgrade proposal) firmware, we finished writing the firmware implementing most of the functionality needed for data flowing including SPY buffers. We receive dummy road data from the P3 connector using an existing Merger board, and send the data to a downstream board. Within them, there are two FIFO's implemented in VHDL and Input/Output road SPY buffers. All of these functions work well. Two efforts for I/O chip (called HB1) are ongoing in parallel. One is to flow the data between the control chip and the I/O chip using VHDL FIFO's. For this, we are doing lots of simulation work now. This work also contains assignment of the data flow lines between two chips. The other effort involves the remaining functionality. We started examining mezzanine memory access via VME for the first step. We also completed writing the firmware for all of the read and write mode functionality of finite state mode, and are in the process of testing it.

Track Fitter: The remainder of the TF++ I/O firmware was finished up and tested on a few simple events, and cold-start (run initialization) routines for the new TF were written. After successfully cold-starting the TF++ in the test stand, we sent ~1000 events (~2-3k tracks) into the board, which still uses a 40 MHz clock. With the exception of some parity bits, the output matches simulation exactly. We upgraded the make-address lookup table (in firmware and simulation) to use long cluster bits to select which 4 layers to use when we have 5/5 roads, and the agreement with simulation still holds. In the next month, we plan to understand why one of the cold-start routines fails occasionally, and to continue more extensive tests before optimizing for faster clocks.

Mezzanines and Pulsars: All hardware for the SVT upgrade (Pulsar boards, large memory mezzanine cards, small memory mezzanine cards, and transition boards) has been received. All memory mezzanines, 75% of Pulsar boards, and all the transition boards have been tested. We are in the middle of converting the full board simulation (Pulsar plus mezzanines) to ModelSim, which can handle the SVT upgrade boards.

Integration: We have prepared a plan for the first two steps of the installation, which are AMSRW and AM++ installation and then TF++ installation. We are now integrating one AMSRW and one AM++ board with other svt boards in the vertical slice. The

vertical slice writes "parasitic" track data in the SVDD bank. In this way, we can run extensive tests to make sure that the new boards successfully find tracks working together with old boards.

VI. FINANCIAL STATUS (as of 31 May 2005)

The baseline cost of the Project is \$10,375K, consisting of Run IIb Project costs (\$9,034K) plus the closeout costs of the silicon detector upgrade (\$1,341K), which will no longer be constructed.

Current Financial Tracking Report - The table below contains current values for selected financial tracking quantities that do not appear in the standard Obligations or Cost Performance Reports. For the Silicon Detector portion of the project, we assume a BAC of \$1,341K and obtain the ACWP from the Obligations report. Remaining portions of the project have their costs listed in the Cost Performance Report.

	ACWP		BCWP		BAC		Cont.	EAC	ETC	Complete
	Silicon	Non-Sil	Silicon	Non-Sil	Silicon	Non-Sil				
CY 2004										
October	1342	1957	1342	2125	1673	5254	3448	6759	6908	50%
November	1357	2081	1357	2366	1673	5254	3448	6642	6652	54%
December	1341	2199	1341	2673	1673	5254	3448	6453	6361	58%
CY 2005										
January	1341	2277	1341	2909	1673	5254	3448	6295	6125	61%
February	1341	2396	1341	3095	1341	5531	3503	6173	5939	65%
March	1341	2866	1341	3361	1341	5531	3503	6377	5673	68%
April	1341	3028	1341	3378	1341	5945	3089	6936	5656	65%
May	1341	3274	1341	3850	1341	5945	3089	6710	5184	71%

CDF RunIIB Obligations Report - This report provides a Level 2 summary of outstanding Purchase Orders (PO) where money has been committed but for which the Project has not been invoiced. This does not include requisitions in the system where a Fermilab PO number has not yet been assigned. A brief description of the columns included in this report is given below:

- Current Month Total Cost – The cost charged to the project for the reporting month.
- Current Month Obligation – This is the total of the obligations made against the project for the reporting month.
- Year to Date Total Cost – This is the total cost charged to the project in this fiscal year.
- Year to Date Obligations with Indirect – This is the total of the obligations made against the project for this fiscal year.
- Current Purchase Orders Open Commitment – This is the total of the open commitments against the project. It includes open commitments from the current and all prior years.
- Prior Year Total Cost - This is the total cost charged to the project in all prior fiscal years.

The total project cost is simply the sum of the Year-to-Date costs and the Prior Year costs. The total committed and spent is the Total Project Cost plus the Open Commitment value.

**CDF Project Obligations Report
Through 31 May 2005**

CDF RIIb EQU - May FY05 IN \$K							
Task Number	Expenditure Category	Current Month Total Cost	Current Month Obligation	YTD Total Cost	YTD Obligations w/Indirect	Current PO Open Comm	Prior Yr Total Cost
Silicon	M&S	0.0	0.0	(0.3)	(103.7)	0.0	539.0
	SWF	0.0	0.0	(1.1)	(1.1)	0.0	571.1
	OH	0.0	0.0	(2.7)	(2.7)	0.0	230.9
	Total 1.1	0.0	0.0	(4.1)	(107.5)	0.0	1,341.0
Calorimeter	M&S	0.0	0.0	43.5	21.2	21.3	211.8
	SWF	0.0	0.0	0.0	0.0	0.0	139.1
	OH	0.0	0.0	0.9	0.9	0.0	51.5
	Total 1.2	0.0	0.0	44.3	22.1	21.3	402.3
Trigger/DAQ	M&S	168.7	276.9	870.3	1,415.0	602.3	708.2
	SWF	35.3	35.3	254.4	254.4	0.0	220.7
	OH	23.4	0.0	133.0	133.0	0.0	129.2
	Total 1.3	227.5	312.2	1,257.7	1,802.5	602.3	1,058.1
Administration	M&S	1.9	2.1	3.0	3.3	0.2	29.1
	SWF	12.1	12.1	96.9	96.9	0.0	268.2
	OH	4.0	0.0	29.8	29.8	0.0	84.4
	Total 1.4	18.0	14.2	129.8	130.0	0.2	381.7
Total Project	M&S	170.6	279.0	916.5	1,335.8	623.8	1,488.2
	SWF	47.4	47.4	350.2	350.2	0.0	1,199.0
	OH	27.4	0.0	161.0	161.0	0.0	495.9
Grand Total		245.4	326.4	1,427.7	1,847.0	623.8	3,183.1

Total Project Cost (Inception To Date): 4,610.9

CDF Project Cost Performance Report (CPR) – This report is generated from COBRA and provides a summary of the WBS 1.2-1.4 costs of the Project down to Level 3 of the Work Breakdown Structure. Silicon detector subproject closeout costs are not tracked here. Input data originates with the status (% Complete) of the Project schedules as reported by the Level 2 managers and actual costs extracted from the Fermilab accounting system. Where possible, costs are accrued for items that have been delivered, but not yet invoiced. This is only possible for a small fraction of our cost. Financial summaries are shown for this reporting period (columns 2-6) as well as the project to date (columns 7-11). Column 12 contains our baseline BAC, and will only be changed after the formal implementation of the Change Control process. Column 13 is the projected BAC, based on the current month's schedule. A number of specialized financial terms and abbreviations used in the CPR are defined here for convenience:

ACWP – Actual Cost of Work Performed. This is the actual cost of tasks that have been completed.

BAC – Budget at Completion. The BAC is the estimated total cost of the project when completed. It is equivalent to the BCWS at completion. The baseline value of the BCWS is contained in column 12 of the Cost Performance Report.

BCWP – Budgeted Cost of Work Performed. This is the scheduled cost profile of tasks that have been completed.

BCWS – Budgeted Cost of Work Scheduled. This is the sum of the budgets for all planned work to be accomplished within a given time period.

CV – Cost Variance. $CV = BCWP - ACWP$

EAC – Estimate At Completion. This is the ACWP to date, plus the BCWS (current scheduled estimate) of remaining tasks. $EAC = (BAC (current) - BCWP) + ACWP$

ETC – Estimate to Completion. $ETC = EAC - ACWP + Contingency$

Percent Complete - %Com = $\frac{BCWP}{BAC}$

SV – Schedule Variance. $SV = BCWP - BCWS$

**CDF Project
Cost Performance Report
Through 31 May 2005**

Cost Performance Report - Work Breakdown Structure													
Contractor: Location:					Contract Type/No:			Project Name/No: CDF RIIb Mstr Equ - D		Report Period: 4/30/2005 5/31/2005			
Quantity	Negotiated Cost		Est. Cost Authorized Unpriced Work		Tgt. Profit/ Fee %	Tgt. Price	Est Price	Share Ratio	Contract Ceiling	Estimated Contract Ceiling			
1	9,033,999		0		0	0.00	9,033,999	0	0	0			
Funding Type-CA WBS[2] WBS[3]	Current Period					Cumulative to Date					At Completion		
Item	Budgeted Cost		Actual Cost Work Performed	Variance		Budgeted Cost		Actual Cost Work Performed	Variance		Budgeted	Latest Revised Estimate	Variance
	Scheduled	Performed		Schedule	Cost	Scheduled	Performed		Schedule	Cost			
EQU Equipment													
1.2 Calorimeter Upgrades													
1.2.1 Central Preshower and Crack Detectors	0	0	0	0	0	444,504	444,504	422,928	0	21,576	444,504	444,504	0
1.2.2 Electromagnetic timing	0	0	0	0	0	23,403	23,403	23,403	0	1	23,403	23,403	0
WBS[2]Totals:	0	0	0	0	0	467,908	467,908	446,331	0	21,577	467,908	467,908	0
1.3 Run 2b DAQ and Trigger Project													
1.3.1 Run 2b TDC Project	39,655	11,206	4,754	-28,449	6,452	556,485	504,531	520,642	-51,955	-16,111	655,792	655,792	0
1.3.2 Run 2b Level 2 Project	15,446	12,462	16,049	-2,984	-3,587	410,991	410,197	402,864	-793	7,333	473,959	473,959	0
1.3.4 Event-Builder Upgrade	29,803	15,676	54,882	-14,127	-39,206	400,751	377,812	263,313	-22,939	114,498	435,363	435,363	0
1.3.5 Computer for Level3 PC Farm / DAQ	293,243	145,919	0	-147,324	145,919	471,844	324,520	237,044	-147,324	87,476	1,101,492	1,101,492	0
1.3.6 SVT upgrade	37,134	6,766	31,841	-30,368	-25,075	308,106	258,890	227,809	-49,216	31,081	362,407	362,407	0
1.3.11 Revised XFTH Project	296,761	263,725	119,943	-33,036	143,782	1,503,997	976,434	664,479	-527,563	311,955	1,703,357	1,697,256	-6,100
WBS[2]Totals:	712,042	455,753	227,468	-256,289	228,285	3,652,173	2,852,384	2,316,151	-799,790	536,233	4,732,369	4,726,268	-6,100
1.4 Administration													
1.4.3 Construction Phase	16,873	16,873	17,954	0	-1,081	530,083	530,083	511,509	0	18,573	744,322	744,322	0
WBS[2]Totals:	16,873	16,873	17,954	0	-1,081	530,083	530,083	511,509	0	18,573	744,322	744,322	0
Funding Type-CATotals:	728,916	472,627	245,423	-256,289	227,204	4,650,164	3,850,374	3,273,992	-799,790	576,383	5,944,598	5,938,498	-6,100
Sub Total	728,916	472,627	245,423	-256,289	227,204	4,650,164	3,850,374	3,273,992	-799,790	576,383	5,944,598	5,938,498	-6,100
Management Resrv.											3,089,401	3,095,502	6,101
Total	728,916	472,627	245,423	-256,289	227,204	4,650,164	3,850,374	3,273,992	-799,790	576,383	9,033,999	9,033,999	0

VII. VARIANCE ANALYSIS – P. Lukens

Subproject	Schedule Variance	Cost Variance
Run 2b TDC	Not significant. Limited by operations, and the availability of the detector.	None.
Run 2b XFTII	Due to delays in deliveries of the first board and associated testing, the production purchases for the SLAM and Finder did not start until May.	Actual costs have lagged the progress. Costs will be accrued next month.
Event Builder	None	Costs are low. Some engineering has been done with physicist (no cost) labor. Engineering costs from CD are expected to be transferred in June.
Computers for Level 3 and DAQ	None	A scheduling error resulted in an apparent variance. This will be resolved during June.
SVT Upgrade	None	Actual costs have lagged the progress. Costs will be accrued next month.
Administration	None	Costs for support and travel have been below estimates.

VIII. BASELINE CHANGES

There were several baseline changes made during May, 2005. The details were described in the April, 2005 monthly report. One additional change (Change Request #22) was made in May, which was done to synchronize our financial tracking with our most current resource loaded schedules. This action resulted in a small adjustment to our baseline track trigger cost.

IX. FUNDING PROFILES

The funding profile for the RunIIb CDF Detector Project is shown below. This profile has been updated to include additional Italian contributions to the Silicon Vertex Trigger subproject. These contributions are a result of the scope established in August, 2004.

	Funding Plan in Current Year \$K				
	FY02	FY03	FY04	FY05	Total
DOE MIE	\$ 3,460	\$ 3,509	\$ 1,673	\$ 1,732	\$ 10,375
DOE R&D	\$ 1,670	\$ 480	\$ -	\$ -	\$ 2,150
Foreign Contributions	\$ 39	\$ 518	\$ 234	\$ 404	\$ 1,195
U.S. Universities	\$ 24	\$ 225	\$ 103	\$ 26	\$ 378
Total	\$ 5,193	\$ 4,732	\$ 2,010	\$ 2,162	\$ 14,097