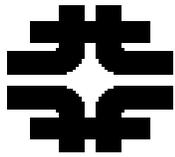


**ADMEM Checkout  
Phase 3**

Technician Name \_\_\_\_\_

ADMEM Serial Number \_\_\_\_\_



**Fermilab**

Particle Physics Division/CDF Upgrade Project

**ADMEM  
ADC/Memory Module**

**FINAL STOP –  
Supervisor  
CHECKOUT DOCUMENT**

Revised  
4/19/99  
Theresa M. Shaw  
Rodney Klein

**Checkout Sheet**

**Technician Name:** \_\_\_\_\_

**ADMEM #:** \_\_\_\_\_

**Note any test which initially fails and the action taken to repair it:**

**Name of Failing Test:** \_\_\_\_\_

**Repair Steps:** \_\_\_\_\_

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

**Name of Failing Test:** \_\_\_\_\_

**Repair Steps:** \_\_\_\_\_

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

**Name of Failing Test:** \_\_\_\_\_

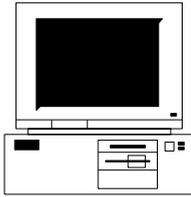
**Repair Steps:** \_\_\_\_\_

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

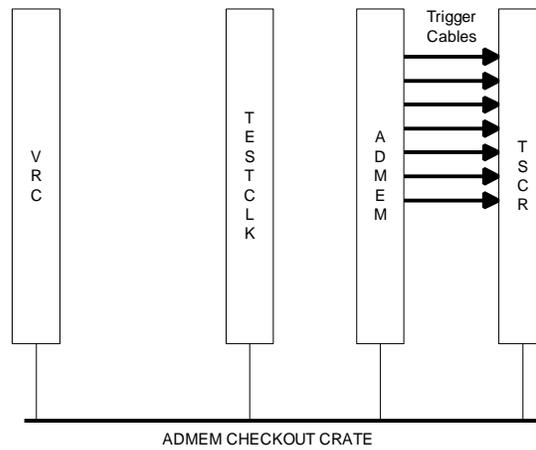
## TESTSTAND EQUIPMENT

Each Teststand should be equipped with the following Equipment:

- VIPA CDF Crate
- VME CPU on 9U adapter
- TSCR
- TESTCLK\_V7
- Short Trigger Cable
- Special Digital Paddle Card with Testpoints
- 20 Digital Paddle Cards
- Digital Multimeter
- Oscilloscope
- HP Logic Analyzer



PC



## Initial Checkout

\_\_\_\_\_ Verify that the module has been through initial checkout procedures.

### Looping Checkout

\_\_\_\_\_ In the Supervisor Teststand, set up as shown above, run the Supervisor Loop Test for at least 1 hour per board. This test will loop over the following test options.

**Please Note that all seven Trigger Cables must be attached.**

**The ADMEM must be configured as a Plug module.**

- Test Diagnostic Register
- Test Control Register
- Test Access Register for Flash RAM
- Test Flash RAM Access Register
- Test Pipeline Diagnostic Channels Enable Register
- Test Diagnostic Pipeline FIFO
- Test Transition Port Register
- Test Café Allocated Flash RAM
- Test Trigger Sum Flash RAM
- Test L2 Header Word
- Test Pipeline Length Register
- Test Pipeline Offset Register
- Test DAC Data Register
- Test DAC Control Register
- Test Café Control Register
- Test Café Delay Register
- Test Channels (0-3) Pedestal Subtraction Register
- Test Channels (4-7) Pedestal Subtraction Register
- Test Channels (8-11) Pedestal Subtraction Register
- Test Channels (12-15) Pedestal Subtraction Register
- Test Channels (16-19) Pedestal Subtraction Register
- Test Diagnostic Data Mode through Trigger Sums (should do all seven ports)
- Test Digital Pipeline thru L2 Buffers and L1 Pipeline
- Test Pipeline Trigger Sums (should do all seven ports with low and high order bits tested)

\_\_\_\_\_ An overnight test (>8hours running) should be set up with each days worth of checked out Boards. These Boards should have Pattern data ( 0x0000, 0xFFFF, 0xAAAA, 0x5555 ) loaded into digital Paddle cards.

**TAM** should then be run.