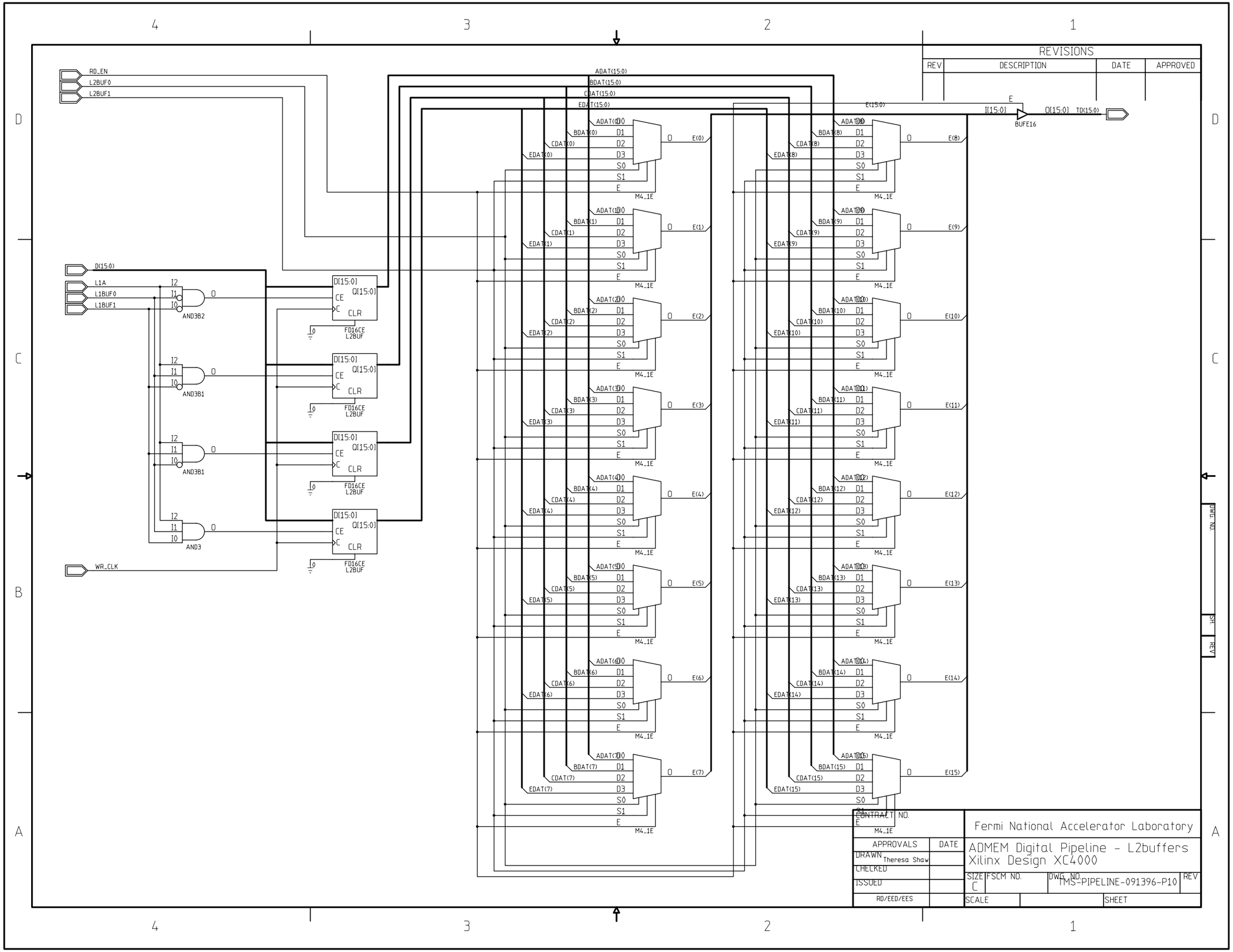
RD_EN
L2BUF0
L2BUF1
D(15:0)
L1A
L1BUF0
L1BUF1
WR_CLK
AND3B2
AND3B1
AND3B1
AND3
FD16CE
L2BUF
D(15:0)
Q(15:0)
CE
C
CLR
ADAT(15:0)
BDAT(15:0)
CDAT(15:0)
EDAT(15:0)
E(15:0)
I(15:0)
O(15:0)
TD(15:0)
BUFE16
M4_1E
D0
D1
D2
D3
S0
S1
E
O
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
DWG. NO.
SH.
REV
CONTRACT NO.
Fermi National Accelerator Laboratory
APPROVALS
DATE
DRAWN
Theresa Shaw
CHECKED
ISSUED
RD/EED/EES
ADMEM Digital Pipeline - L2buffers
Xilinx Design XC4000
SIZE
C
FSCM NO.
DWG. NO.
TMS-PIPELINE-091396-P10
REV
SCALE
SHEET