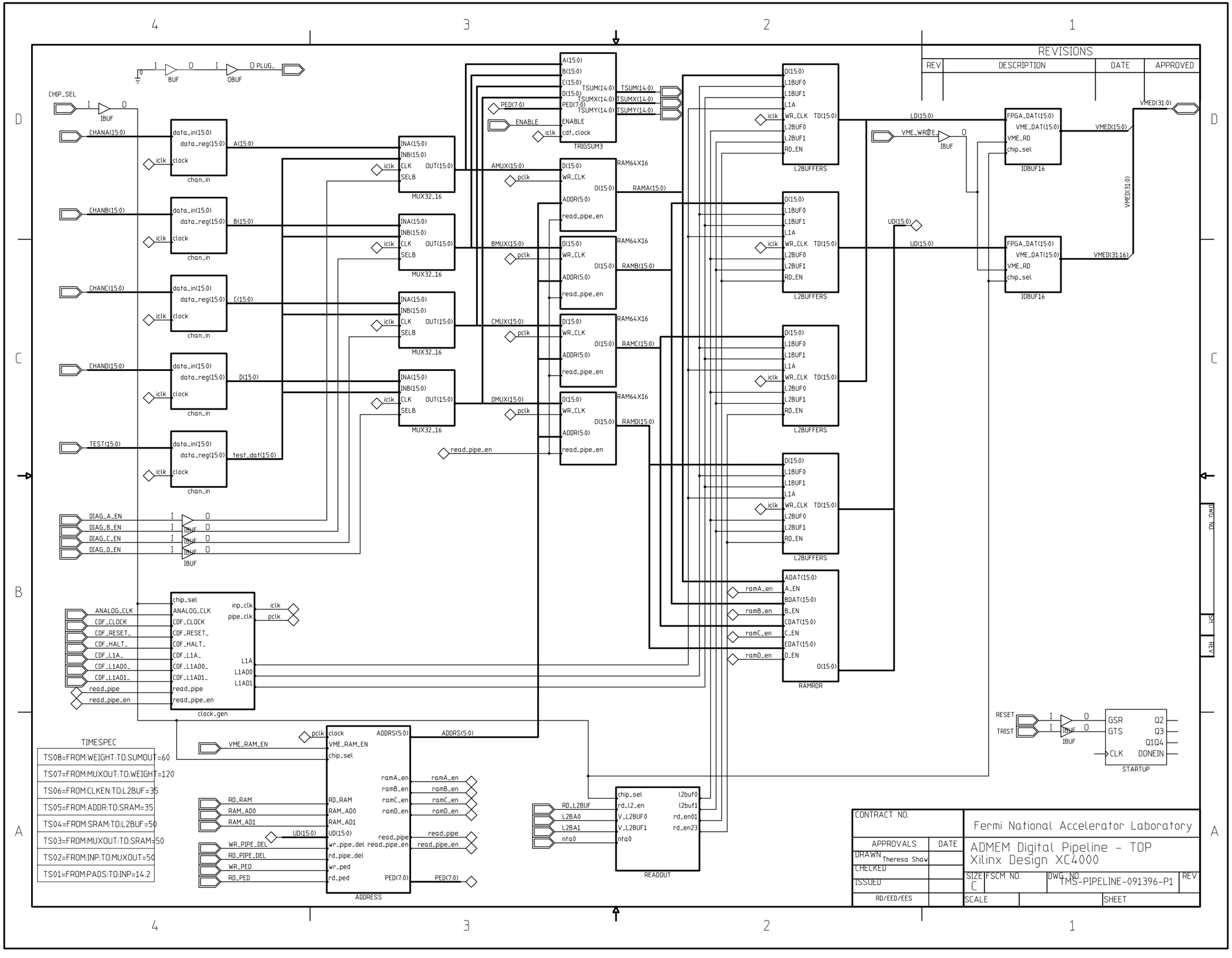
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
CHIP_SEL
IBUF
BUF
OBUF
PLUG_
CHANA(15:0)
CHANB(15:0)
CHANC(15:0)
CHAND(15:0)
TEST(15:0)
DIAG_A_EN
DIAG_B_EN
DIAG_C_EN
DIAG_D_EN
data_in(15:0)
data_reg(15:0)
clock
chan_in
A(15:0)
B(15:0)
C(15:0)
D(15:0)
test_dat(15:0)
INA(15:0)
INB(15:0)
CLK
SELB
OUT(15:0)
MUX32_16
AMUX(15:0)
BMUX(15:0)
CMUX(15:0)
DMUX(15:0)
iclk
pclk
A(15:0)
B(15:0)
C(15:0)
D(15:0)
TSUM(14:0)
TSUMX(14:0)
TSUMY(14:0)
PED(7:0)
ENABLE
cdf_clock
TRIGSUM3
RAM64X16
WR_CLK
ADDR(5:0)
read_pipe_en
RAMA(15:0)
RAMB(15:0)
RAMC(15:0)
RAMD(15:0)
L2BUFFERS
L1BUF0
L1BUF1
L1A
WR_CLK
TD(15:0)
L2BUF0
L2BUF1
RD_EN
LD(15:0)
VME_WRITE
FPGA_DAT(15:0)
VME_DAT(15:0)
VME_RD
chip_sel
IOBUF16
VMED(31:0)
VMED(15:0)
VMED(31:16)
UD(15:0)
ADAT(15:0)
A_EN
BDAT(15:0)
B_EN
CDAT(15:0)
C_EN
EDAT(15:0)
D_EN
ramA_en
ramB_en
ramC_en
ramD_en
RAMRDR
ANALOG_CLK
CDF_CLOCK
CDF_RESET_
CDF_HALT_
CDF_L1A_
CDF_L1AD0_
CDF_L1AD1_
read_pipe
read_pipe_en
inp_clk
pipe_clk
L1AD0
L1AD1
clock_gen
RESET
TRIST
GSR
GTS
CLK
Q2
Q3
Q1Q4
DONEIN
STARTUP
TIMESPEC
TS08=FROM:WEIGHT:TO:SUMOUT=60
TS07=FROM:MUXOUT:TO:WEIGHT=120
TS06=FROM:CLKEN:TO:L2BUF=35
TS05=FROM:ADDR:TO:SRAM=35
TS04=FROM:SRAM:TO:L2BUF=50
TS03=FROM:MUXOUT:TO:SRAM=50
TS02=FROM:INP:TO:MUXOUT=50
TS01=FROM:PADS:TO:INP=14.2
VME_RAM_EN
ADDRS(5:0)
RD_RAM
RAM_AD0
RAM_AD1
WR_PIPE_DEL
RD_PIPE_DEL
WR_PED
RD_PED
wr_pipe_del
rd_pipe_del
wr_ped
rd_ped
PED(7:0)
ADDRESS
RD_L2BUF
L2BA0
L2BA1
nta0
chip_sel
rd_l2_en
V_L2BUF0
V_L2BUF1
l2buf0
l2buf1
rd_en01
rd_en23
READOUT
CONTRACT NO.
APPROVALS
DATE
DRAWN
Theresa Shaw
CHECKED
ISSUED
RD/EED/EES
Fermi National Accelerator Laboratory
ADMEM Digital Pipeline - TOP
Xilinx Design XC4000
SIZE
C
FSCM NO.
DWG NO.
TMS-PIPELINE-091396-P1
REV
SCALE
SHEET
DWG NO.
SH
REV