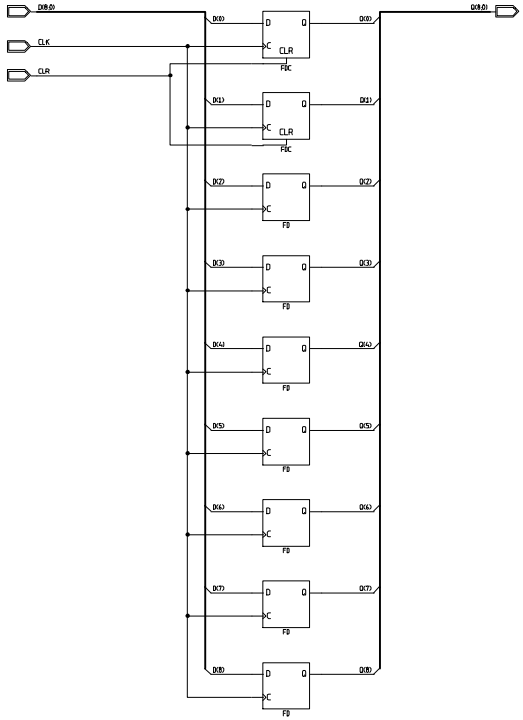
DWG. NO.	SH.	REV

REVISIONS

REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO. CDF UPGRADE ELECTRONICS		Fermi National Accelerator Lab		
APPROVALS	DATE	TRACER XILINX FPGA DESIGN TSI Interface - 9 bit register block CALIB Reg		
DRAWN Theresa M. Shaw				
CHECKED				
ISSUED		SIZE D	FSCM NO.	DWG. NO. TMS-TRAC-102496-1A	REV
		SCALE		SHEET 1 of 1