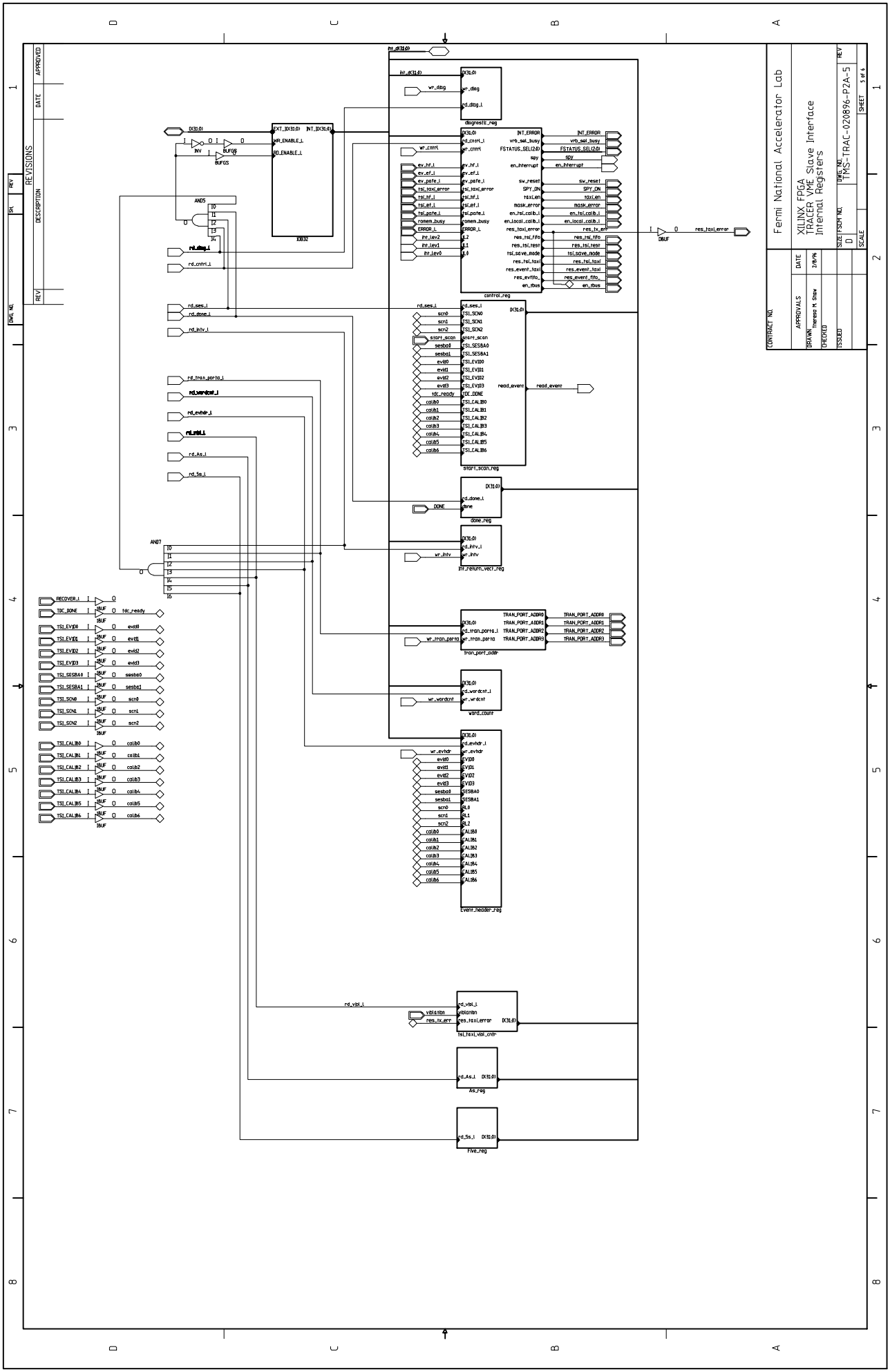
Fermi National Accelerator Lab
XILINX FPGA
TRACER VME Slave Interface
Internal Registers
TMS-TRAC-020896-P2A-5
SHEET 5 of 6
REVISIONS
DESCRIPTION
DATE
APPROVED
CONTRACT NO.
APPROVALS
DRAWN Theresa M. Shaw
CHECKED
ISSUED
SIZE D
SCALE
DWG. NO.
REV
diagnostic_reg
control_reg
start_scan_reg
done_reg
int_return_vect_reg
tran_port_addr
word_count
event_header_reg
tsi_taxi_viol_cntr
As_reg
Five_reg
IOB32
AND5
AND7
INV
BUFGS
DBUF
IBUF
OBUF
RECOVER_i
TDC_DONE
TSI_EVID0
TSI_EVID1
TSI_EVID2
TSI_EVID3
TSI_SESBA0
TSI_SESBA1
TSI_SCN0
TSI_SCN1
TSI_SCN2
TSI_CALIB0
TSI_CALIB1
TSI_CALIB2
TSI_CALIB3
TSI_CALIB4
TSI_CALIB5
TSI_CALIB6
DONE
INT_ERROR
FSTATUS_SEL(2:0)
sw_reset
SPY_ON
taxi_en
mask_error
en_tsi_calib_i
en_local_calib_i
res_taxi_error
res_tx_err
res_tsi_fifo
res_tsi_test
tsi_save_mode
res_tsi_taxi
res_event_taxi
res_event_fifo_
en_tbus
read_event
TRAN_PORT_ADDR0
TRAN_PORT_ADDR1
TRAN_PORT_ADDR2
TRAN_PORT_ADDR3
wr_diag
wr_cntrl
wr_intv
wr_tran_porta
wr_wordcnt
wr_evhdr
rd_vibl_i
rd_ses_i
rd_done_i
rd_intv_i
rd_tran_porta_i
rd_evhdr_i
rd_As_i
rd_5s_i
rd_cntrl_i
rd_diag_i
rd_vibl_i
vibl_tbn
res_tx_err