

Fermilab

Particle Physics Division/CDF Upgrade Project

**Specification for
TRigger And Clock + Event Readout Module
(TRACER)**

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Revision History

7/14/97	TMS	Addition of Flash RAM for Constant Storage Addition of TBUS (P0 Connector) Drivers
8/19/97	TMS	Fix type on TBUS Register Definition
3/16/98	TMS	Update TDC Calibration Pulse Width Register format, Update info on Front panel backplane spy ports
4/24/98	TMS	Update Control Register, Start Scan Register, Calibration Register Start Scan Register, and Event Header Registers. Calibration bits now accessible through Event Header and Start Scan Register. Readout List bits can now be controlled in Local Calibration Mode. Also, a logic change has been made in how the Busy signal to the Trigger System is derived.
6/2/98	TMS	Fix Error in Control Register Description
12/6/99	TMS	Fix Error in Control Register Description – bit 25
12/11/02	TMS	Fix Error in TBUS register address (address is 0x80 not 0x40)

1.0 Introduction

The *TR*igger *And* *C*lock + *E*vent *R*eadout Module (TRACER) performs the role of system interface for the front end crates to the rest of the upgraded CDF system. It will be assumed that the reader is familiar with the readout system described in CDF/DOC/TRIGGER/CDFR/2288 "A Standard Front-End and Trigger VMEbus Based Readout Crate for the CDF Upgrade - The CDF Readout Crate".

One of the TRACER's functions is to provide an interface to the Master Clock. The TRACER is used to fanout the precision 132ns clock and three clocking gates: Beam Zero, Beam Crossing, and Abort. The TRACER does this by driving the signals it receives from the Master Clock onto the CDF custom backplane where they are then readily available to all modules plugged into the crate. No timing adjustment is done to any signals from the Master Clock. Any custom tuning of the arrival of the signals will be done in the Clock Fanout Modules.

A second TRACER function is to provide an interface to the Trigger System Interface (TSI). The TRACER is used to fanout all trigger and control information received from the TSI. The TRACER receives encoded information from an optical link, decodes it and passes it onto the CDF custom backplane. These signals are used by the ADMEMs and other front-end modules to either pass an event fragment into one of four Level 2 readout buffers or to throw it away.

The TRACER also provides a path for sending the event data to the VMEbus Readout Boards (VRBs). Event data may be transmitted in two ways: the TRACER may act as a "spy" on the backplane and place backplane data into its Event FIFO, or it can receive data written directly into its Event FIFO from the VRC (VME Readout Controller). Once data exists in the Event FIFO, a sequencer onboard the TRACER will readout the event data, serialize it and then transmit the data to the VRB modules over fiber optic cables. The VRB will transmit the signal VRB_BUSY back to the TRACER if at any time it cannot accept the next event. If VRB_BUSY is detected by the TRACER, data transmission will be held off until the condition clears.

Finally, the TRACER provides a means by which to issue a crate reset. The VMEbus signal SYSRESET* will be pulsed low on the backplane if a reset pulse is detected from the CDF Reset Crate. An RS-422 signal is sent from the Reset Crate to a TRACER front panel connection if a crate reset is desired. A crate reset ability is required in the event of a CPU board hanging. NOTE that this reset ability is separate from the TSI CDF_RECOVER~ signal which serves to reset L1 pipeline pointers.

Figure 1 provides a system overview and shows where the TRACER fits in. Figure 2 provides a block diagram of the TRACER.

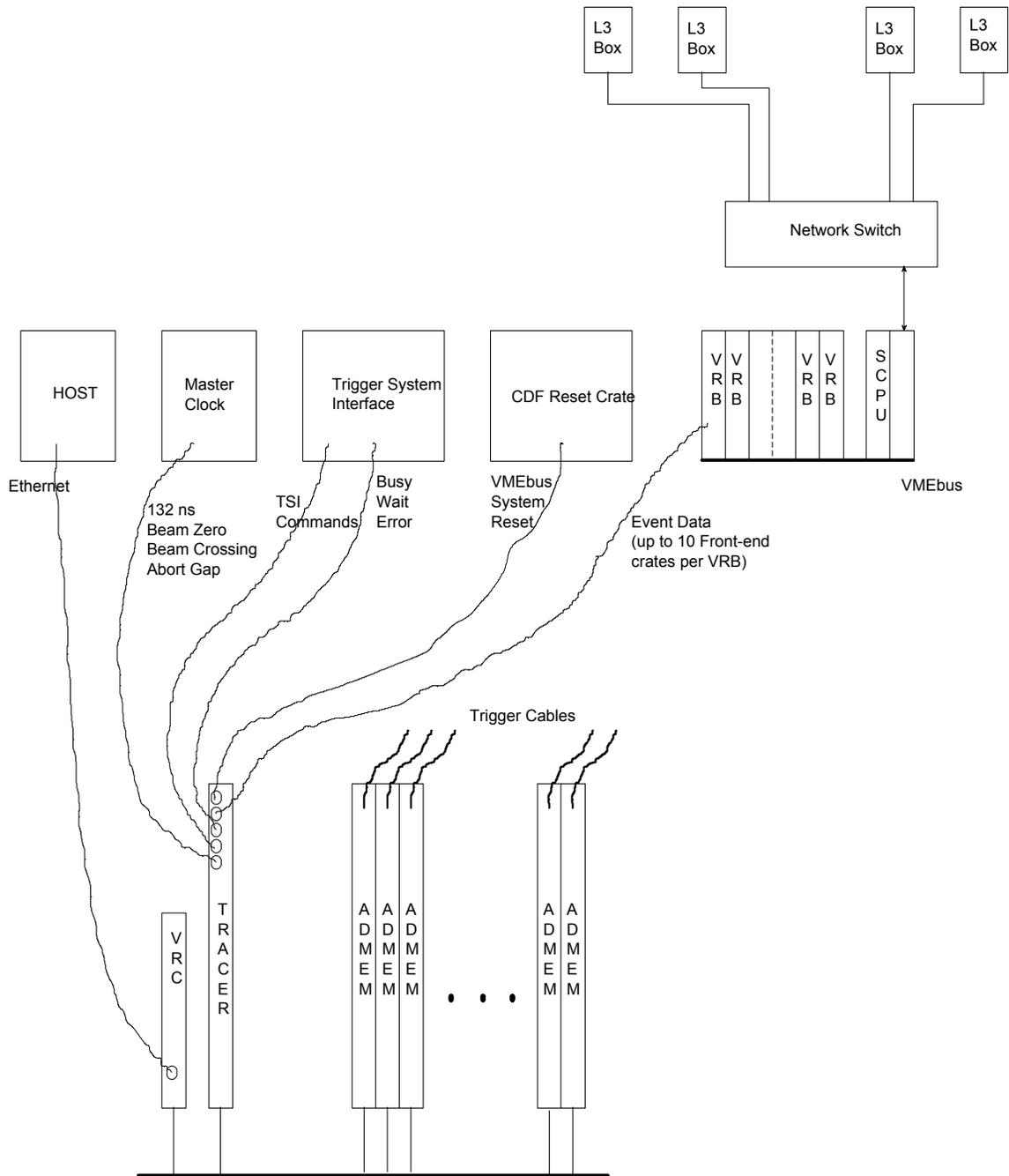


Figure 1. Block Diagram of Calorimetry DAQ System

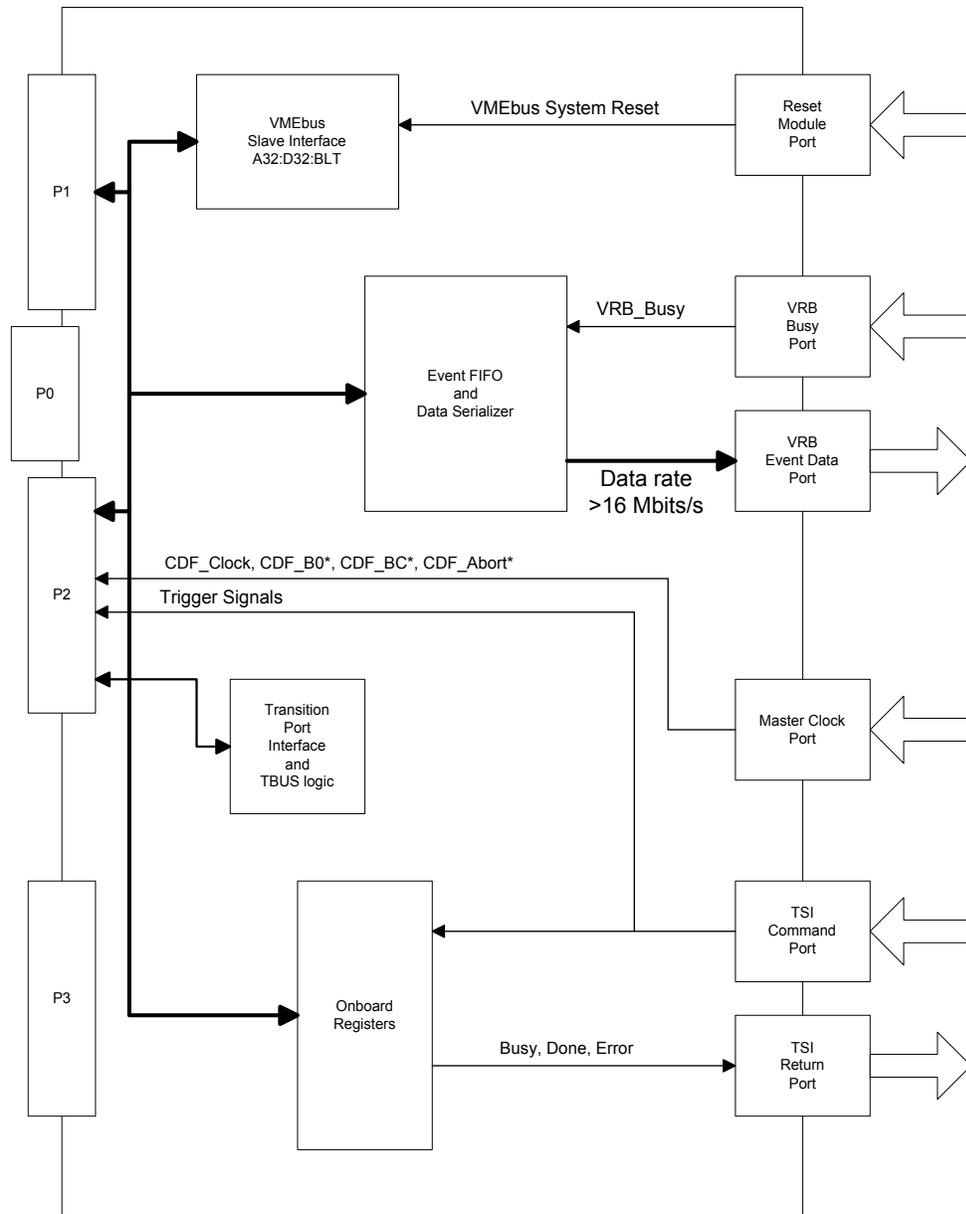


Figure 2 Block Diagram of Trigger Fanout/Crate Monitor/Spy Module

2.0 Interface to the Master Clock

The TRACER provides a front panel connection to receive a cable from the Master Clock. The Master Clock will provide the precisely timed 132 ns clock signal as well as gates which indicate the Beam Zero Crossing, Beam Crossing and Abort Gaps. The Master Clock signals are received as differential LVDS signals. The TRACER will provide a 100 ohm terminating input resistor for each of the signals. A 8-pin Shielded Data Link style connector will be provided to receive the cable from the Master Clock (see Appendix C). The shield of this connector will not be connected to the TRACER's digital ground. The front panel connector pinout will be as follows:

<u>Pin</u>	<u>Signal</u>	
1	Master_Clock	(132 ns clock)
2	Master_Clock*	
3	Beam_Crossing	
4	Beam_Crossing*	
5	Beam_Zero	(once around marker)
6	Beam_Zero*	
7	Abort_Gap	
8	Abort_Gap*	

The TRACER will receive these signals and drive the following backplane signals:

CDF_CLK	
CDF_CLK*	- 132 ns clock; accurately timed <i>differential PECL</i> signal delivered by the Master Clock. CDF_CLK is the only precisely timed signal. All other signals are considered gates to the rising edge of CDF_CLK. All CDF backplane signals are guaranteed to be valid for 10ns on either side of the rising edge of CDF_CLK.
CDF_BC*	- Beam Crossing (TTL)
CDF_B0*	- Bunch 0 (TTL)
CDF_ABORT*	- Abort Gap (TTL)

The TRACER will simply buffer these signals to the backplane - No timing adjustments will be done. CDF_B0~, CDF_BC~ and CDF_ABORT~ are active low gates to the rising edge of the CDF_CLK signal. They are guaranteed to have at least a 10 ns setup (see Figure 3) and hold time with respect to the clock edge.

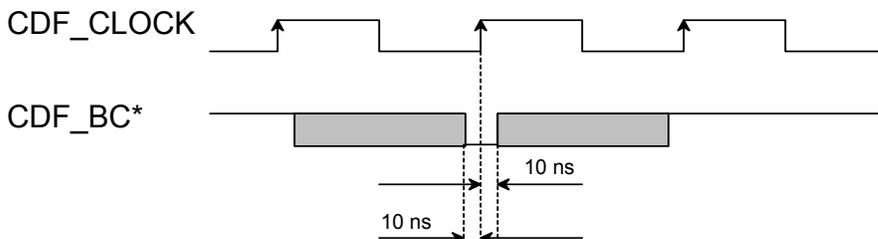


Figure 3. Backplane Timing Example of CDF_CLOCK and a Clock Gate

3.0 Interface to Trigger System Interface(TSI)

3.1 TSI <-> TRACER Optic Link

The TRACER will provide an interface to the TSI. An optical link using TAXIchip (AM7969-175JC) protocol, AMP optical receivers (AMP 269050-1), and operating at two times the CDF_CLK, provides the means for the TSI to issue commands. The TRACER will take the signals that it receives from the TSI, decode them and drive the appropriate trigger signals out onto the custom CDF VMEbus backplane. The TSI <-> TRACER protocol is described in the note "**Trigger Supervisor Protocols for Run II**" written by the CDF Group of Yale University.

The following backplane trigger signals will be driven by the TRACER as the result of TSI commands:

FROM TSI		Backplane Signal driven by TRACER	
L1 Word	bit 2	CDF_L1A*	- Level 1 Accept
	bit 3	CDF_L1R*	- Level 1 Reject
	bit 4	CDF_L2B0*	- Level 1 Accept Buffer Address 0
	bit 5	CDF_L2B1*	- Level 1 Accept Buffer Address 1
	bit 6	CDF_GLIVE*	- Level 1 Accept corresponds to live Beam Crossing
	bit 7	CDF_L1_CALIB*	- Indicates L1A event is from a Calibration
	bit 8	RSVD_L1W2*	- TSI reserved L1 word bit(8)
	L2 Word	bit 2	CDF_L2DB0*
bit 3		CDF_L2DB1*	- Level 2 Accept Decision Buffer Address 1
bit 4		CDF_L2A_EN*	- Level 2 Accept Enable signal
bit (8:5)		CDF_EVID(3:0)*	- Event Identifier(0)
Calib Word	bit (8:2)	CDF_CALIB(6:0)*	- Calibration bits which may be sent by TSI; these currently have no definition
Control Word	bit 2	CDF_STOP*	- Set Halt Condition
	bit 3	CDF_RECOVER*	- Reset FIFOs/pipelines
	bit 4	CDF_TEST*	- Diagnostic bit which will cause TRACER to capture TAXI link (TSI <-> TRACER)
	bit 5	CDF_RUN*	- Clear Halt Condition
	bit (8:6)	CDF_RL(2:0)*	- Readout List Identifier

(the following signals are generated by TRACER using above TSI info)

CDF_HALT*	- Halt filling L1 FIFO/pipelines - the HALT condition is set by CDF_STOP* and cleared by CDF_RUN*
CDF_CALEN*	- Calibration Enable - this is set whenever a TSI Calibration Word is received

CDF_L2A*	- Level 2 Accept - this is set whenever a TSI L2 Word is received and CDF_L2A_EN* is true
CDF_L2R*	- Level 2 Reject - this is set whenever a TSI L2 Word is received and CDF_L2A_EN* is false

All of the above signals are gates to the rising edge of the CDF_CLK signal. They are guaranteed to have at least a 10 ns setup and hold time with respect to the clock edge.

3.2 The Start Scan and Done Registers

The TRACER will also provide Start Scan and Done Registers which will be used in communications protocol with the TSI. When the TSI indicates it is time to read out an event (Start Event Scan), the “Start Scan” bit will be set in the TRACER’s Start Scan Register.

The VMEbus Readout Controller (VRC) can poll this register and begin readout when it sees the Start Scan bit set, or an interrupt mode may be enabled by setting the “Interrupt Mode Enable” bit of the TRACER’s Control Register. Interrupt mode causes the TRACER to initiate an Interrupt cycle upon the reception of Start Scan.

When the VRC has finished its readout cycle, it will write to the Done Register and set the “Done” bit. The “Done” bit is cleared upon the reception of the next Start Scan.

Start Scan Register

Description: Event tagging data for this register comes from the TSI “Level 2” word. The “Start Scan” bit is set when a L2 Accept is indicated, and cleared when the “Done” bit is set in the Done Register. Bit 16 reflects the state of the open-collector backplane signal CDF_TDC_DONE.

<u>Bit</u>	<u>Function</u>
0-15	Undefined
16	CDF_TDC_DONE
19-17	Undefined
20	Readout List 0
21	Readout List 1
22	Readout List 3
23	Undefined
24	Start Scan
25	L2 Decision Buffer Address 0
26	L2 Decision Buffer Address 1
27	Undefined
28	Event ID 0
29	Event ID 1
30	Event ID 2
31	Event ID 3

Done Register

Description: The Done bit can be set to a logic high by the VRC, over VMEbus, when readout is complete. The VMEbus path does not allow the bit to be set to a logic low. The Done bit will also be set to a logic high by the “recover” command in the event of a Halt-Recover-Run sequence.

The Done bit will be set to a logic low with the issuance of a new Start Event Scan command by the TSI.

The End of Block(EOB) marker may be written over VMEbus. When it is set, it will cause an EOB to be appended to the data in the Event FIFO. It is a self-clearing bit and cannot be read back. The EOB marker is an optional feature - its usage is optional.

Done and EOB have been placed in the same register in order to reduce the number of VMEbus cycles which the VRC must do at the end of a readout cycle. Typical usage would have the VRC set both Done and EOB at the end of a readout cycle. However, if an “early” done is sent to the TSI, the EOB marker could be sent later, after the data has been transferred to the Event FIFO.

<u>Bit</u>	<u>Function</u>
23-0	Undefined
24	Done (VMEbus can set DONE when bit 24 equals “1”, no reset capability over VMEbus)
30-25	Undefined
31	End of Block (EOB) (write only - self clearing bit)

3.3 DONE, ERROR and BUSY Signals

TSI <-> TRACER protocol also relies on a parallel copper link which will allow the TRACER to drive the signals DONE, ERROR and BUSY to the TSI.

The DONE signal is simply the buffered “Done” bit in the Done Register.

The ERROR signal will be asserted whenever some module in the CDF Crate is asserting CDF_ERROR~ on the open-collector backplane signal. The assertion of ERROR is meant to occur only in the case of a catastrophic error. It is possible to mask ERROR with a bit in the control register.

The BUSY signal can be asserted to two different ways. The default is to have the TRACER return BUSY to the TSI whenever the Event FIFO status flags indicate that the FIFO is greater than half full. It possible to reprogram which status flags are actually being compared to produce the TSI BUSY by writing to register bits (3:1) in the TRACER’s Control Register.

Alternatively, the BUSY signal can be asserted whenever the buffer space in the VRB (CDF's VMEbus Readout Board) becomes full by setting the Bit 0 of the Control Register. A direct optical link between the VRB and the TRACER, informs the TRACER when the higher level DAQ readout has become clogged.

This BUSY signal will not be cleared with a Halt-Recover-Run sequence. In order to clear BUSY, the problem with the status of the Event FIFOs or with the clogged VRB readout buffers must be fixed.

An eight pin Shielded Modular Data Link Connectors (see Appendix C) will be provided on the TRACER’s Front Panel. The shield of this connector will be connected to the TRACER’s digital ground. The connector has the following pinout:

<u>Pin</u>	<u>Signal</u>
1	DONE
2	DONE~
3	ERROR
4	ERROR~
5	BUSY
6	BUSY~
7	NC
8	NC

3.4 TEST Mode

It is possible for the TSI to turn on input to the TSI Diagnostic FIFO by sending the “TEST” bit in the TSI Control Word. When “TEST” is sent, the FIFO is flushed and the next 8K data words received from the TSI are clocked into a FIFO. In its this operating mode, once the FIFO is full, no further data recording will be done. In order to repeat the test, the original “TEST” state must be cleared by toggling the “Reset TSI Diagnostic FIFO TEST mode” bit in the Control Register.

A second diagnostic mode possible - it will, however, be overridden by any “TEST” message written from the TSI. In the second mode, it is possible to save the last ~8K of TSI commands by setting the “Enable TSI Diagnostic FIFO Save Mode” bit of the Control Register. When this bit is set the TSI Diagnostic FIFO will be filled by incoming TSI commands. As the FIFO limit is approached, automatic readout is begun to clear space for new commands. If at any time a CDF_ERROR* condition occurs, the state of the FIFO will be frozen. Hopefully, this will aid in determining what was going on in the crate at the time of the error.

4.0 Data Transmission

The TRACER has an optical data link to the VRB. This link uses the TAXIchip (AM7968-175JC) protocol and AMP optical driver (AMP 269049-1). It operates at two times the CDF_CLK.

An 8K by 32 bit Event FIFO feeds this data link. It is possible to fill this Event FIFO in two ways. One way is to simply do a VMEbus write into the FIFO. If the VRC is used to do zero suppression and data formatting, this method would be used. The VRC would first read in raw event data, do the formatting and then write the formatted data to the Event FIFO.

A second method for getting event data to the VRB would involve using the TRACER's Spy capability. The TRACER will have the capability to spy on the data as the VMEbus Readout Controller (VRC) reads it out. During event readout, the TRACER has the ability to clock data into the Event FIFO. The data which gets clocked into the event FIFO includes any VMEbus reads of data in the L2 Buffer Space (specified in CDF/DOC/TRIGGER/CDFR/2288), and any write to the TRACER's Done Register which sets the EOB marker. This Spy mode would be used only if there is no need for the VRC to do data formatting.

A sequencer on the TRACER will detect when data is present in the FIFO, serialize the data through the use of a TAXIchip, and transmit it upstairs to the Readout Memory (VRB) module via an optical link. The data can be transmitted to the VRB at a rate of up to one byte every 66 ns (twice the CDF clock). A Taxi Sync signal is sent up at least every 5 bytes; thus, a data rate of 4 Bytes/(5 x 66ns), or 12.1 MB/s is achievable out of the crate.

It is possible to append set an End of Block (EOB) marker on the transmitted data stream. This is done by writing to the EOB bit in the Done register. Whenever a logic high is written to this bit, the equivalent of a 33 bit word will be clocked into the Event FIFO. The most significant bit will be set high and will indicate the EOB. This EOB bit will be passed to the TaxiChip as the 9th data bit, which can then be decoded as EOB by the VRB.

5.0 Event Data Header Information

The TRACER will have registers to hold header information which should be applied to all event fragments which are transmitted to the VRB. The following header information should mark all events:

Word Count	(32 bits)	;downloaded from system or calculated by VRC
Partition ID	(3 bits)	;downloaded from system
Crate ID	(8 bits)	;downloaded from system
Event ID	(4 bits)	;obtained from TSI
L2 Buffer Address	(2 bits)	;obtained from TSI
Readout List #	(3 bits)	;obtained from TSI
Calibration Type #	(6 bits)	;obtained from TSI

The Word Count will be used by the VRB as a way of identifying Event fragments as they pass through it.

This header information can get into the Event FIFO in two ways. If the VRC is doing event formatting and transmitting the formatted event to the TRACER's Event FIFO, the VRC should apply the header to the formatted data. In this case, the VRC would need to be told the Partition ID and Crate ID at start-up. The rest of the header information would be available to the VRC through (1) reading the Start Scan register which is being polled in order to know when to initiate Event readout or (2) reading the Start Scan register upon receiving a Start Scan interrupt if interrupt mode is enabled.

In the case where the TRACER is in spy mode, and directly stores the raw event data into its Event FIFO, it is necessary to include the TRACER word count and header Registers in the beginning of the readout list. As they are read out, they will be written into the Event FIFO like all other Event data.

Word Count Register

Description: this register contains the number of 32 bit words (inclusive) which make up the event fragment. It must be downloaded if "Spy" mode is used.

<u>Bit</u>	<u>Function</u>
31-0	Word Count(31:0)

Event Header Register

Description: this register contains the minimum amount of information which must be applied as a header to all event fragments read out into L3.

<u>Bit</u>	<u>Function</u>
7-0	Crate ID(7:0) (r/w)
10-8	Partition ID(2:0) (r/w)
11-15	Undefined
19-16	Event ID(3:0) (r)
21-20	L2 Buffer Address(1:0) (r)
24-22	Scan List #(2:0) (r)
31-25	Calibration #(6:0) (r)

It may also be desirable to mark the end of an event. To do this we could repeat the Word Count and Event Header information. Two possible pattern words of A's and 5's will also be available as tags to be added to these words to aid in the descrambling of event blocks.

6.0 Reset Function

It is necessary to provide a remote reset capability for front end VMEbus crates. The main purpose of the reset will be to reboot a CPU which has hung. This will be done through the use of a dedicated reset line which will come in through a front panel connector and be driven by the CDF Reset Crate.

The reset signal will be driven and received as an RS-422 signal. When the reset line is pulsed low it will drive the SYSRESET* line low on the VMEbus backplane. This will cause all boards to do a reset.

7.0 TRACER TDC Calibration Features

Standard CDF Calibration Signals

The standard method of performing a calibration with the CDF system involves having the Trigger System Interface (TSI) send down a Calibration word which causes the CDF signal CDF_CALIBEN* to be asserted on the backplane. At some number of programmable (for example, 42) CDF clock cycles later, a L1 Accept will be issued. The data is then available in the L2 Decision Buffers for readout. A Start Event Scan message would be generated by the TSI to cause the event to be readout into the event stream.

Additional Features Required for TDC Calibration

Additional calibration signals are required for the TDCs. These signals consist of three backplane signals called CDF_TDC_CAL(2:0)*, as well as a precision differential PECL signal called CDF_TDC_CALIB*. All of these signals are active low.

CDF_TDC_CAL(2:0)* will be derived from the TSI Calibration word with the additional programmability that the pulses will not fire unless they have been enabled, and then not until two delay requirements are fulfilled. The TDC calibration pulses are enabled via the TDC Calibration Pulses Enable Register.

TDC Calibration Pulses Enable (r/w)

<u>Bit</u>	<u>Function</u>
28-0	Undefined
29	Enable CDF_TDC_CAL0*
30	Enable CDF_TDC_CAL1*
31	Enable CDF_TDC_CAL2*

The first programmable delay required is the number of CDF clock cycles which should occur prior to firing. This delay will range from 0-255. This delay will be set via a register on the Tracer and each of the four TDC calibration pulses will be independently programmable. Course delay values are set in the TDC Calibration Course Delay Register.

TDC Calibration Course Delay Register (r/w)

<u>Bit</u>	<u>Function</u>
7-0	Undefined
15-8	Delay for CDF_TDC_CAL0*
23-16	Delay for CDF_TDC_CAL1*
31-24	Delay for CDF_TDC_CAL2*

The second delay requirement will be a finer delay which will be set off the edge of CDF clock. This delay will be provided through an Analog Devices AD9501. The AD9501 can be set for a full scale range of 132ns with 255 delay steps for an adjustment step of ~.5 ns. Fine delay values are set in the TDC Calibration Fine Delay Register.

TDC Calibration Fine Delay Register (r/w)

<u>Bit</u>	<u>Function</u>
7-0	Delay for CDF_TDC_CAL0*
15-8	Delay for CDF_TDC_CAL1*
23-16	Delay for CDF_TDC_CAL2*
31-24	Undefined

There is an inherent propagation delay of 25-30 ns through the AD9501 - this will not be taken out, so it be necessary to have the ability to have L1 Accepts issued on up to two consecutive events to cover the full 132ns CDF cycle.

A final value of some concern is the pulse widths of CDF_TDC_CAL(2:0)*. The pulse width will be controlled via a programmable delay. The minimum pulse width will be 20ns and can grow in 5ns intervals up to 55ns. The pulse width will be controlled via the TDC Calibration Pulse Width Register. The pulse width will be 20ns + (5ns x value of Width Count).

TDC Calibration Pulse Width Register (r/w)

<u>Bit</u>	<u>Function</u>
21-0	Undefined
22-20	Width Count (2:0) for CDF_TDC_CAL0*
23	Undefined
26-24	Width Count (2:0) for CDF_TDC_CAL1*
24	Undefined
30-28	Width Count (2:0) for CDF_TDC_CAL2*
31	Undefined

Again, in normal operating mode, in order for any data to be included in the readout stream, the TSI must know to send a L1 Accept and a Start Event Scan. Therefore, any delays programmed into the first delay requirement would need to be communicated back to the TSI. Also, note that the TSI cannot change this number on the fly and it may/will conflict with other systems. This should not be a problem in a stand-alone TDC calibration run.

Front Panel Input

CDF_TDC_CALIB* can be driven through a twinax Front Panel bulkhead which expects differential PECL levels. It will be re-driven as a differential PECL signal to the backplane. Driver and Receiver chips will make use of ECLPS logic.

8.0 Local Test Stand Calibration

8.1 Introduction to test stand calibration

A need to perform in-crate calibration of the QIEs without control from the TSI exists. The timing and "quiet time" requirements make the calibrations difficult to fit into run-time protocol between the TSI and the TRACER. Calibration constants are most easily determined within the crate, using the local computing power of the VRC.

The VRC will determine the gains and offsets for each of the four QIE capacitors over ten QIE scales. This results in 80 constants to be determined. These constants will then be used by the VRC to calculate values for a lookup table which will linearize the raw QIE output.

Similarly, it will be possible to have the TRACER logic trigger the special TDC calibration signals which were described in the previous section.

8.2 The Calibration flow

8.2.1 Calorimetry Test Stand Flow

Calibration of the calorimetry is accomplished in the following manner:

- Set up the calibration reference by writing to a register on the ADMEM board.
- Set ADMEM look-up tables to pass-through mode (raw data will not be changed).
- Wait.
- Issue a Calibration command by writing to the TRACER Calibration Register.
- Tracer will wait programmed time, determined by the TRACER Start Delay Register.
- Tracer will issue Halt - Reset - Run sequence.
- Admem boards will begin filling pipeline with Beam Zero Crossing.
- Tracer will wait programmed time, determined by the TRACER Calibration Enable Delay Register.
- Tracer will issue Calibration Enable.
- Tracer will issue four successive L1 Accepts at a programmed number of crossings (set in the Calibration Delay Register) after calibration enable. The successive L1 Accepts will fill buffers 0, 1, 2 and 3 in that order.

- Tracer will wait a programmed delay, determined by the TRACER Halt Delay Register.
- Tracer will issue Halt (if halt mode enabled).
- Tracer will set a bit in a register to indicate process is done.

VRC will see calibration is complete, and will read out L2 buffer.

8.2.2 TDC Test Stand Flow

Calibration of the TDCs is accomplished in the following manner:

- Set up the TDC Calibration Control Registers described in the previous section.
- Issue a Calibration command by writing to the TRACER Calibration Register.
- Tracer will wait programmed time, determined by the TRACER Start Delay Register.
- Tracer will issue Halt - Recover - Run sequence.
- TDC boards will begin filling pipeline with Beam Zero Crossing.
- Tracer will wait programmed time, determined by the TRACER Calibration Enable Delay Register.
- Tracer will issue Calibration Enable.
- The Calibration Enable will trigger the TDC Calibration circuitry.
- TDC Calibration signals CDF_TDC_CAL(2:0)* will fire according to the constraints set in the TDC Calibration Pulses Enable Register, the TDC Calibration Course Delay Register and the TDC Calibration Fine Delay Register.
- Tracer will issue four successive L1 Accepts at a programmed number of crossings (set in the Calibration Delay Register) after calibration enable. The successive L1 Accepts will fill buffers 0, 1, 2 and 3 in that order.
- Tracer will wait a programmed delay, determined by the TRACER Halt Delay Register.

- Tracer will issue Halt (if halt mode enabled).
- Tracer will set a bit in a register to indicate process is done.

VRC will see calibration is complete, and will read out L2 buffer.

8.3 Setting up the Tracer

The Tracer must provide control over the following CDF backplane signals in order for the calibration to take place:

CDF_L1A~	(L1 Accept)
CDF_L1R~	(L1 Reject)
CDF_L2B0~	(L2 Buffer Address 0)
CDF_L2B1~	(L2 Buffer Address 1)
CDF_HALT~	(Halt L1 Buffer fill)
CDF_RESET~	(Reset all pipeline pointers)
CDF_RL0~	(Readout List bit 0)
CDF_RL1~	(Readout List bit 1)
CDF_RL2~	(Readout List bit 2)
CDF_CALIB0~	(Calibration bit 0)
CDF_CALIB1~	(Calibration bit 1)
CDF_CALIB2~	(Calibration bit 2)
CDF_CALIB3~	(Calibration bit 3)
CDF_CALIB4~	(Calibration bit 4)
CDF_CALIB5~	(Calibration bit 5)
CDF_CALIB6~	(Calibration bit 6)
CDF_CALEN~	(Calibration enable)
CDF_TDC_CAL(2:0)~	(TDC Calibration signals)

The timing of when these signals take place is critical to the calibration. The Tracer will provide a high degree of control over when these signals are asserted.

8.4 Tracer Calibration Registers

Calibration Register

Description: writing a one to the Local Calibration Enable bit, will automatically begin a teststand type calibration (assuming local teststand calibration mode has been previously enabled in general CSR register).

<u>Bit</u>	<u>Function</u>
15-0	Undefined
16	Local Calibration Enable
17	Readout List 0
18	Readout List 1
19	Readout List 2
23-20	Undefined
24	Calibrate 0
25	Calibrate 1
26	Calibrate 2
27	Calibrate 3
28	Calibrate 4
29	Calibrate 5
30	Calibrate 6
31	Enable Halt Mode ; this bit will cause the Tracer to issue a halt, a pre-programmed number of clock cycles after a L1 Accept

Start Delay Register

Description: this register will contain the value reflecting the number of 132ns clock cycles to wait before asserting the Halt - Reset - Run sequence following a write to the Calibration Register.

<u>Bit</u>	<u>Function</u>
15-0	Undefined
31-16	count of 132ns waiting periods

Calibration Delay Register

Description: this register contains the value, bits (15:0), reflecting the number of 132ns clock cycles to wait before asserting the Calibration Enable gate as well as the number of 132ns clock cycles, bits (31:16), to wait following the issuance of L1 Accept.

For a calorimetry local test stand run, the value of bits (31:16) would be set to 42, the pipeline depth. For a TDC calibration type, bits (31:16)

<u>Bit</u>	<u>Function</u>
15-0	Calen* Delay Value count of 132ns waiting periods, following the Halt-Recover-Run sequence, before issuing Calibration Enable
31-16	L1A* Delay Value count of 132ns waiting periods, after issuing Calibration Enable, before asserting L1A

Halt Delay Register

Description: this register will contain a value reflecting the number of 132ns clock cycles to wait following the issuance of a L1 Accept before asserting a CDF_HALT~. CDF_HALT~ will be asserted only if the Enable Halt Mode bit is set in the Calibration Register.

<u>Bit</u>	<u>Function</u>
15-0	Undefined
31-16	count of 132ns waiting periods

Calibration Done Register

Description: this is a read-only register which will contain a bit to indicate that the teststand calibration is done. It will be cleared with a write to the Calibration register and set at the end of the teststand calibration cycle.

<u>Bit</u>	<u>Function</u>
30-0	Undefined
31	Teststand Calibration Done

9.0 TRACER Interrupt Mode

The TRACER has an interrupt feature which may be used to indicate that a Start Event Scan message has been received. The enabling of this interrupt mode is controlled via the “Interrupt Mode Enable” bit of the TRACER’s Control Register. The interrupt feature is provided as an alternative method to the polling of the Start Event Scan Register.

The Interrupt Level is settable via switches on board, and the set level is readable through the Control Register.

A separate Interrupt Return Vector Register will allow the user to set the interrupt return vector.

10.0 TRACER Transition Module Port

A sixteen bit read/write port to a possible transition module has been included on the TRACER. The port is written to and read from via the Transition Port Read/Write Register on the TRACER. A four bit address to the port is set via the Transition Port Address Register. The port also receives positive logic read and write control signals.

The user defined pins of the P0 connector are used to implement the port, see Table 1.

PIN #	Row a	Row b	Row c	Row d	Row e
1	+5V	+5V	+5V	+5V	+5V
2	Ret_WX	Reserved	+5V	TBUS 1+	TBUS 1-
3	Ret_WX	Reserved	Reserved	TBUS 2+	TBUS 2-
4	Vw	Reserved	tran_port a(0)	tran_port d(0)	tran_port d(1)
5	Vw	Reserved	tran_port a(1)	tran_port d(2)	tran_port d(3)
6	Ret_WX	Reserved	tran_port a(2)	tran_port d(4)	tran_port d(5)
7	AREF_WX	Reserved	tran_port a(3)	tran_port d(6)	tran_port d(7)
8	Ret_WX	Reserved	tran_port read	tran_port d(8)	tran_port d(9)
9	Vx	Reserved	tran_port write	tran_port d(10)	tran_port d(11)
10	Vx	Reserved	USER I/O	tran_port d(12)	tran_port d(13)
11	Vy	Reserved	USER I/O	tran_port d(14)	tran_port d(15)
12	Vy	Reserved	USER I/O	USER I/O	USER I/O
13	Ret_YZ	Reserved	USER I/O	USER I/O	USER I/O
14	AREF_YZ	Reserved	USER I/O	USER I/O	USER I/O
15	Ret_YZ	Reserved	USER I/O	USER I/O	USER I/O
16	Vz	Reserved	USER I/O	USER I/O	USER I/O
17	Vz	Reserved	Reserved	TBUS 3+	TBUS 3-
18	Ret_YZ	Reserved	Reserved	TBUS 4+	TBUS 4-
19	Ret_YZ	Reserved	Reserved	TBUS OC1	TBUS OC2

Table 1. TRACER Transition Module Port - P0 Connector Pin Definition

11.0 TBUS Drivers and Receivers

The TRACER provides a means to use the TBUS lines of the P0 Connector. These lines are bussed and terminated on the J0 backplane and their usage can be defined on a system by system basis.

The TRACER will use PECL drivers to drive the TBUS(4:1) lines. They can be driven by writing to the TBUS Register and setting the “Enable TBUS Driver” bit in the Control Register.

The TBUS OC(2:1) lines are assumed to be open collector TTL and their status can be read through the TBUS Register.

12.0 Flash Memory Constant Storage

A 1 Megabit (131,072 x 8-Bit) AMD AM29F010 Flash Memory has been incorporated on the TRACER. The purpose of this Flash Memory is to serve as a storage device for any TRACER or crate level constants.

Like all Flash RAM, a specific algorithm must be used when erasing or programming the contents.

Two examples below describe how to set up the erase and the write algorithms to these devices. For additional information on these devices, please refer to AMD’s data sheet.

To erase the Flash RAM

```

write 0xAA00 0000 to addr 0xYY61 5554 (YY is Geo. Address)
write 0x5500 0000 to      0xYY60 AAA8
write 0x8000 0000 to      0xYY61 5554
write 0xAA00 0000 to      0xYY61 5554
write 0x5500 0000 to      0xYY60 AAA8
write 0x1000 0000 to      0xYY61 5554

```

To write the Flash RAM

```

write 0xAA00 0000 to addr 0xYY61 5554
write 0x5500 0000 to      0xYY60 AAA8
write 0xA000 0000 to      0xYY61 5554
write desired data to    desired address

```

13.0 TRACER Front Panel

The TRACER Front Panel will contain the following LED indicators:

+5V	;LED (red) on when module is powered
Module Select	;LED (green) on during VMEbus access
TSI_DONE	;LED (green) on when DONE is being returned to TSI
TSI_ERROR	;LED (red) on when ERROR is being returned to TSI
TSI_BUSY	;LED (yellow) on when BUSY is being returned to TSI

The TRACER Front Panel will also hold

8-pin Shielded Data Link connector for TSI return signals

Connector Ground Shield connected to Board Ground

8-pin Shielded Data Link connector to receive Master Clock Signals

Connector Ground Shield not connected to Board Ground

An optical cable receiver for TSI TAXI-protocol data

An optical cable driver for data link to VRB

An optical cable receiver for the Busy signal from the VRB

An 8-pin module jack to receive a reset signal from the CDF RESET Crate

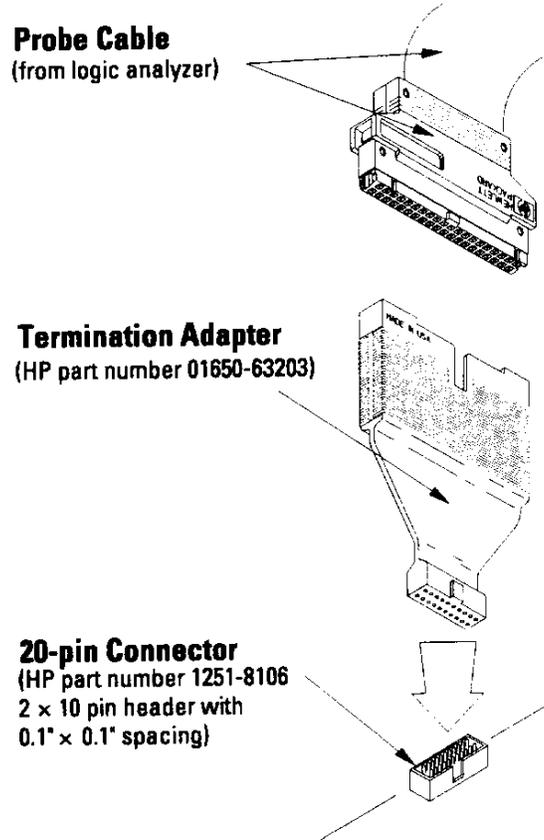
No ground shield

Two 34 pin headers to spy on the special CDF backplane signals (see Table2)

TDC calibration Twinax Bulkhead; LVDS input

Logic Analyzer Port - On the TRACER

Tracer Front Panel Ports J will provide ports for easy access to the CDF backplane trigger and clock signals. These ports will bring TTL level signals to four 20 pin right angle box headers on the front panel. The ports can be used by a wide range of oscilloscopes or logic analyzers, but are specifically designed for ease of use with HP logic analyzers and the HP Terminator Adapter.



Hewlett Packard Pinout on Terminator Adapter (HP part number 01650-63203)

Pin	Signal	Pin	Signal
20	GND	19	D0
18	D1	17	D2
16	D3	15	D4
14	D5	13	D6
12	D7	11	D8
10	D9	9	D10
8	D11	7	D12
6	D13	5	D14
4	D15	3	CLK1
2	CLK2	1	+5V

CDF Signals are connected to the Port as follows:

Port J7 - POD 1

Pin	Signal	Pin	Signal
20	GND	19	<i>CDF_TDC_CAL0*</i>
18	CDF_RowA1	17	<i>CDF_TDC_CAL1*</i>
16	CDF_RowA2	15	<i>CDF_TDC_CAL2*</i>
14	CDF_RowA3	13	<i>CDF_TDC_CALIB</i>
12	CDF_RowA4	11	No Connect
10	CDF_RowA5	9	<i>CDF_TDC_DONE</i>
8	<i>CDF_CLOCK</i>	7	CDF_RowC7
6	No Connect	5	CDF_RowC8
4	CDF_RowA8	3	CDF_CLOCK
2	No Connect	1	No Connect

Port J8 - POD 2

Pin	Signal	Pin	Signal
20	GND	19	CDF_RowC9
18	<i>CDF_BC*</i>	17	CDF_RowC10
16	<i>CDF_B0*</i>	15	CDF_RowC11
14	CDF_RowA11	13	<i>CDF_GLIVE*</i>
12	<i>CDF_L1A*</i>	11	<i>RSVD_L1W1*</i>
10	<i>CDF_L1R*</i>	9	<i>RSVD_L1W2*</i>
8	<i>CDF_L2B0*</i>	7	<i>CDF_STOP*</i>
6	<i>CDF_L2B1*</i>	5	<i>CDF_TEST*</i>
4	<i>CDF_HALT*</i>	3	CDF_CLOCK
2	No Connect	1	No Connect

Port J9 - POD 3

Pin	Signal	Pin	Signal
20	GND	19	<i>CDF_RUN*</i>
18	CDF_RowA17	17	<i>CDF_RL0*</i>
16	<i>CDF_RECOVER*</i>	15	<i>CDF_RL1*</i>
14	CDF_RowA19	13	<i>CDF_RL2*</i>
12	<i>CDF_ABORT*</i>	11	<i>CDF_CALIB3*</i>
10	<i>CDF_CALIB0*</i>	9	<i>CDF_CALIB4*</i>
8	CDF_RowA22	7	<i>CDF_CALIB5*</i>
6	<i>CDF_CALIB1*</i>	5	<i>CDF_CALIB6*</i>
4	<i>CDF_CALIB2*</i>	3	CDF_CLOCK
2	No Connect	1	No Connect

Port J10 - POD 4

Pin	Signal	Pin	Signal
20	GND	19	<i>CDF_CALEN*</i>
18	CDF_RowA25	17	CDF_RowC26
16	<i>CDF_ERROR*</i>	15	<i>CDF_L2R*</i>
14	<i>CDF_L2A*</i>	13	<i>CDF_L2A_EN*</i>
12	<i>CDF_L2BD0*</i>	11	<i>CDF_EVID0*</i>
10	CDF_RowA29	9	<i>CDF_EVID1*</i>
8	<i>CDF_L2BD1*</i>	7	<i>CDF_EVID2*</i>
6	<i>CDF_RSVD0*</i>	5	<i>CDF_EVID3*</i>
4	<i>CDF_RSVD1*</i>	3	CDF_CLOCK
2	No Connect	1	No Connect

Table 2. Front Panel Pinout of Backplane Monitoring

14.0 Power Requirements

The TRACER uses approximately 5Amps @ 5V for a power consumption of 25 Watts.

15.0 VMEbus Slave Interface

The TRACER will implement a modified version of a VMEbus slave interface. Only 32 bit aligned data transfers will be supported; these may be either single word transfers or block transfers. Only extended (32-bit) addressing modes will be supported. All boards will be assigned a unique geographical address through use of backplane pins on the CDF Custom J2 backplane. The TRACER will respond to all address spaces. Therefore, TRACER modules will respond to the following address modifier codes: 09, and 0B.

Memory Map

YY00 0000 Diagnostic Register (32 bit Read/Write) (r/w)
 YY00 0004 Control Register

Please Note all reset lines must be toggled by the user - they are not self-clearing.

<u>Bit</u>	<u>Function</u>
0	Select VRB busy as Trigger System Return Busy source (r/w) default state - low 0 - TS Busy will be derived from Event FIFO status 1 - TS Busy will be derived from VRB busy
1	Event Status Busy Return - Select HF* status default state - low <i>Bits (3:1) provide the user with control over when the TS Busy return bit turns on with respect to the Event FIFO status flags</i>
2	Event Status Busy Return - Select E/F* status default state - hi
3	Event Status Busy Return - Select PAFE* status default state - hi
6-4	Interrupt Level (2:0) (r) <i>allows readback of the Jumper settings of the interrupt level</i>
7	Error (r) <i>reflects the active state (inverted) of CDF_ERROR* on the backplane</i>
8	VRB Busy (r) <i>reflects the state of VRB_Busy signal coming from the VRB</i>

- 9 TSI Diagnostic FIFO PAFE~ (r)
- 10 TSI Diagnostic FIFO E/F~ (r)
- 11 TSI Diagnostic FIFO HF~ (r)

HF*	E/F*	PAFE*	State
1	0	0	Empty
1	1	0	Almost Empty (<P*) P is a Programmable depth P(default is 256)
1	1	1	Less Than Half Full
0	1	1	Greater Than Half Full
0	1	0	Almost Full (> 8K-P)
0	0	0	Full

* To change the value of **P**, issue a reset pulse to the Event FIFO. Then hold the Reset signal to the Event FIFO high, while writing a value to the Event FIFO. Release the Event FIFO reset signal. **P** will be the value of bits (31:24) during the Event FIFO write.

- 12 TSI Taxi Error (r)
TaxiChip violation has been detected
- 13 Event FIFO PAFE~ (r)
- 14 Event FIFO E/F~ (r)
- 15 Event FIFO HF~ (r)
- 16 Undefined
- 17 Enable TBUS Divers (r/w)
default state - low
set high to drive output of TBUS Register onto Backplane (P0) TBUS lines
- 18 Reset the Event FIFO (r/w)
default state - low
toggle hi-lo to clear the Event FIFO
- 19 Reset the TSI TaxiChip Receiver (r/w)
default state - low
toggle hi-lo to reset TaxiChip
- 20 Reset the Event Data TaxiChip Transmitter (r/w)
default state - low
toggle hi-lo to reset TaxiChip
- 21 Enable TSI Diagnostic FIFO Save Mode (r/w)
default state - high
when set, TSI Diagnostic FIFO will save last 8K TSI commands
- 22 Reset TSI Diagnostic FIFO "TEST" mode (r/w)
default state - low
toggle hi-lo to reset "TEST" message from TSI
- 23 Reset TSI Diagnostic FIFO (r/w)
default state - low
toggle hi-lo to reset the TSI Diagnostic FIFO

- 24 Reset TSI Taxi Error (r/w)
 default state - low
 *toggle hi-lo to clear TSI Taxi violation error state, and reset the
 TSI TAXI Violation Counter Register*
- 25 Enable Trigger Signals to backplane
 default state – high
 0 – Tracer will not drive trigger signals to backplane
 1 – Tracer will drive trigger signals to backplane
- 26 Select CDF Trigger Signal source (r/w)
 default state - low
 0 - TSI Interface
 1 - Local Calibration Sequencer
- 27 Interrupt Mode Enable (r/w)
 default state - low
 *when set, enables interrupts when Start Event Scan received from
 TSI*
- 28 Mask CDF_ERROR (r/w)
 default state - low
 when set, will mask out any errors being sent to the TSI
- 29 Event Data Taxi Enable (r/w)
 default state - high
 *when set, the onboard sequencer will begin reading out the Event
 FIFO and streaming the data to the VRB*
- 30 Spy Mode Enable (r/w)
 default state - low
 *when set, L2 buffer space data will be captured from the backplane
 and put into the Event FIFO*
- 31 Software Reset (r/w)
 default state - low
 resets TSI interface registers

YY00 0008 Start Scan Register (r)

<u>Bit</u>	<u>Function</u>
0	Calibration 0
1	Calibration 1
2	Calibration 2
3	Calibration 3
4	Calibration 4
5	Calibration 5
6	Calibration 6
15-7	Undefined
16	CDF_TDC_DONE
19-17	Undefined
20	Readout List 0
21	Readout List 1
22	Readout List 3
23	Undefined
24	Start Scan
25	L2 Decision Buffer Address 0
26	L2 Decision Buffer Address 1
27	Undefined
28	Event ID 0
29	Event ID 1
30	Event ID 2
31	Event ID 3

YY00 000C Done Register (r/w)

<u>Bit</u>	<u>Function</u>
23-0	Undefined
24	Done (VMEbus can set DONE when bit 24 equals "1", no reset capability over VMEbus)
30-25	Undefined
31	End of Block (EOB) (write only - self clearing bit)

- YY00 0010 Calibration Register (r/w)
- | <u>Bit</u> | <u>Function</u> |
|-------------------|--|
| 15-0 | Undefined |
| 16 | Local Calibration Enable |
| 17 | Readout List 0 |
| 18 | Readout List 1 |
| 19 | Readout List 2 |
| 23-20 | Undefined |
| 24 | Calibrate 0 |
| 25 | Calibrate 1 |
| 26 | Calibrate 2 |
| 27 | Calibrate 3 |
| 28 | Calibrate 4 |
| 29 | Calibrate 5 |
| 30 | Calibrate 6 |
| 31 | Enable Halt Mode ; this bit will cause the Tracer to issue a halt, a pre-programmed number of clock cycles after a L1 Accept |
- YY00 0014 Start Delay Register (r/w)
- | <u>Bit</u> | <u>Function</u> |
|-------------------|--------------------------------|
| 15-0 | Undefined |
| 31-16 | count of 132ns waiting periods |
- YY00 0018 Calibration Delay Register (r/w)
- | <u>Bit</u> | <u>Function</u> |
|-------------------|--|
| 15-0 | count of 132ns waiting periods, following the Halt-Recover-Run sequence, before issuing Calibration Enable |
| 31-16 | count of 132ns waiting periods, after issuing Calibration Enable, before asserting L1A |
- YY00 001C Halt Delay Register (r/w)
- | <u>Bit</u> | <u>Function</u> |
|-------------------|--------------------------------|
| 23-0 | Undefined |
| 31-24 | count of 132ns waiting periods |
- YY00 0020 Calibration Done Register (r)
(cleared with any write to the Calibration Register)
- | <u>Bit</u> | <u>Function</u> |
|-------------------|----------------------------|
| 30-0 | Undefined |
| 31 | Teststand Calibration Done |
- YY00 0024 Interrupt Return Vector Register (32 bit Read/Write) (r/w)

YY00 0028 TDC Calibration Pulses Enable (r/w)

<u>Bit</u>	<u>Function</u>
28-0	Undefined
29	Enable CDF_TDC_CAL0*
30	Enable CDF_TDC_CAL1*
31	Enable CDF_TDC_CAL2*

YY00 002C TDC Calibration Course Delay Register (r/w)

<u>Bit</u>	<u>Function</u>
7-0	Undefined
15-8	Delay for CDF_TDC_CAL0*
23-16	Delay for CDF_TDC_CAL1*
31-24	Delay for CDF_TDC_CAL2*

YY00 0030 TDC Calibration Fine Delay Register (r/w)

<u>Bit</u>	<u>Function</u>
7-0	Delay for CDF_TDC_CAL0*
15-8	Delay for CDF_TDC_CAL1*
23-16	Delay for CDF_TDC_CAL2*
31-24	Undefined

YY00 0034 TDC Calibration Pulse Width Register (r/w)

<u>Bit</u>	<u>Function</u>
7-0	Width Count (7:0) for CDF_TDC_CAL0*
15-8	Width Count (7:0) for CDF_TDC_CAL1*
24-16	Width Count (7:0) for CDF_TDC_CAL2*
31-25	Undefined

NOTE: The original five TRACERS' TDC Calibration Width Register had the following format

<u>Bit</u>	<u>Function</u>
21-0	Undefined
22-20	Width Count (2:0) for CDF_TDC_CAL0*
23	Undefined
26-24	Width Count (2:0) for CDF_TDC_CAL1*
24	Undefined
30-28	Width Count (2:0) for CDF_TDC_CAL2*
31	Undefined

YY00 0038 Transition Port Read/Write Register (r/w)

<u>Bit</u>	<u>Function</u>
15-0	Undefined
31-16	Data(15:0)

YY00 003C Transition Port Address Register (r/w)

Bit	Function
27-0	Undefined
31-28	Address(3:0)

YY00 0080 TBUS Register (r/w)

Bit	Function
0	State of TBUS OC1 (read only)
1	State of TBUS OC2 (read only)
2-23	Undefined
24	TBUS1 (r/w)
25	TBUS2 (r/w)
26	TBUS3 (r/w)
27	TBUS4 (r/w)
31-28	Undefined

NOTE: Blue wire modification to TRACER (12/11/02) will allow TBUS1 line to be driven out through an inverting open collector gate unto P2-C26. This mod was made to produce a reset signal for use by the SMXR boards.

YY10 0000 - YY10 007C ID PROM (upper 8 bits) (r)

YY40 XXXX TSI_Diagnostic FIFO (r)
bits (31:23) represent Taxi bits (8:0)
(holds first 8K data words sent down TSI optic link after the receipt of the TEST signal)

YY50 XXXX Event Data FIFO (r/w)

YY6X XXXX Flash RAM Constant Storage (upper 8 bits) (r/w)

YY80 0000	Word Count Register (r/w)
	<u>Bit</u> <u>Function</u>
	31-0 Count of 32 bit Words in Event Record
YY80 0004	Event Header Register
	<u>Bit</u> <u>Function</u>
	7-0 Crate ID(7:0) (r/w)
	10-8 Partition ID(2:0) (r/w)
	11-15 Undefined
	19-16 Event ID(3:0) (r)
	21-20 L2 Buffer Address(1:0) (r)
	24-22 Scan List #(2:0) (r)
	31-25 Calibration #(6:0) (r)
YY80 0008	TSI TAXI Violation Counter Register
YY80 000C	A's Pattern Register (r) This word will contain (hex)AAAAAAAA
YY80 0010	5's Pattern Register (r) This word will contain (hex)55555555

APPENDIX A

Bill Of Materials

<<<From Job: E:\JOBS_TRACER\TRACER_PROD_V2\vbdc\tracer_prod.prj>>>

Fermi National Accelerator
Particle Physics Division
ET&T - CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF DESG
1	3	AD9501JP	Dig Prog Delay Gen, JP pkg	20.00	U56-U58
2	1	AMP 1-520459-3	AMP Modular Jack Connector 8 Pos	2.25	J1
3	1	AMP 3-520459-3	AMP Modular Jack Connector 8 Pos	2.25	J2
4	1	AMP 226968-1 DIGI A1126-ND	Twinax Bulkhead	24.58	J6
5	1	AMP 269050-1	AMP Optronic Data Link - RCVR 200Mb/s	76.47	U15
6	1	AMP 352009-1 PLUS SHIELDS .	AMP 5x19 Z-PACK 2mm Female Conn w/gnd sh	25.00	P0
7	1	AMP269049-1	200 Mb/s 1300 nm optical transmitter.	20.00	D6
8	1	AM27S19SAPC	32x8 PROM	1.25	U35
9	1	AM29F010-45JC	No PDB description available	10.45	U11
10	1	AM7968-175JC	Taxi xmtr	20.00	U22
11	1	AM7969-175JC	TAXI RCVR	25.00	U16
12	1	BOT d_strip	Bottom Discharge strip	.01	X2
13	1	C&K P8121 1160-1890	Mom. Push button Panel mnt	2.48	S4 - Do not stuff
14	3	CAP_CER_SMT_SPARE_1206	SMT CAP SPARE	0.168	C147,C149,C151
15	1	CY7B991-7JC	ROBOCLOCK	21.85	U42
16	5	CY7C470-15JC	Cypress 8K x 9 FIFO	22.00	U17,U28,U38,U44
*					U49
17	5	CY74FCT16500TTSSOP	18-bit Registered Transceivers	5.78	U23,U29,U30,U32
*					U39
18	1	CY74FCT16543CTPAC	No PDB description available		U31
19	5	CY74FCT162244TTSSOP	16-Bit Buffers/Line Drivers	3.95	U18,U27,U37,U43
*					U48
20	1	DS26C32ATN RS-422 recvr National	Diff Line RCVR	3.50	U52
21	1	DS90C031 National	Differential Line Driver	2.23	U9
22	1	DS90C032 National	Differential Line Receiver	2.23	U41
23	3	DS1020	Programmable 8-bit Silicon delay line 1n	22.00	U61-U63
24	2	ERIE 8131-100-651-104M 1415-3140	Bypass Cap .1UF	0.05	C17,C25
25	1	ERIE 8131-100-651-153M 1415-3090	Bypass Cap .015UF	0.07	C1
26	4	ERJ-6ENF19.1 Digi P19.1CBK-ND	1/10W 1% 19.1 ohm	0.061	R40,R43,R51,R54
27	8	ERJ-6ENF51.1 Digi P51.1CBK-ND	1/10W 1% 51.1 ohm	0.061	R41,R42,R44,R45
*					R52,R53,R55,R56
28	1	ERJ-8ENF1.00K Digi P1.00KFBK-ND	1/8W 1% 1.0K ohm	0.0542	R37
29	3	ERJ-8ENF8.0K Digi P8.0KFBK	1/8W 1% 1.0K ohm	0.0542	R78-R80
30	7	ERJ-8ENF66.5 Digi P66.5FBK-ND	1/8W 1% 66.5 ohm	0.0542	R26,R32,R35,R39
*					R46,R65,R68

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Electronics Design System
Bill of Materials

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<<<From Job: E:\JOBS_TRACER\TRACER_PROD_V2\vbdc\tracer_prod.prj>>>

Fermi National Accelerator
Particle Physics Division
ET&T - CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF	DESG
31	2	ERJ-8ENF82.5 Digi P82.5FBK-ND	1/8W 1% 82.5 ohm	0.0542	R70,R71	
32	2	ERJ-8ENF100 Digi P100FBK-ND	1/8W 1% 100 ohm	0.0542	R48,R72	
33	2	ERJ-8ENF121 Digi P121FBK-ND	1/8W 1% 121 ohm	0.0542	R73,R74	
34	2	ERJ-8ENF158 Digi P158FBK-ND	1/8W 1% 158 ohm	0.0542	R29,R30	
35	2	ERJ-8ENF169 Digi P169FBK-ND	1/8W 1% 169 ohm	0.0542	R17,R25	
36	2	ERJ-8ENF249 Digi P249FBK-ND	1/8W 1% 249 ohm	0.0542	R23,R24	
37	2	ERJ-8ENF267 Digi P267FBK-ND	1/8W 1% 267 ohm	0.0542	R28,R34	
38	2	ERJ-8ENF394 Digi P394FBK-ND	1/8W 1% 394 ohm	0.0542	R49,R50	
39	75	Ground Via	Ground-Via	.00	VG1-VG7, VG18, VG19	
*					VG20-VG85	
40	3	HARTING-male	VME64 Card Connector	25.00	P1-P3	
41	1	HIROSE TM5RJ1-66 DIG H9083-ND	Modular Jack 6pos 6contact	2.30	J3	
42	1	HP HFBR-2412	Fiber Optic RCVR	18.15	U26	
43	4	HP HLMP-1301 1445-0475	Red LED	0.24	D1,D3-D5	
44	1	HP HLMP-1401 1445-0495	Yellow LED	0.24	D2	
45	1	IDT 74FCT244DTP	8 bit Tri-state buffer	3.40	U50	
46	17	KEMET T340B106K015AS	10UF 15V Bullet	.80	C56,C57,C59,C61	
*					C104,C132,C137	
*					C157,C161,C167	
*					C181-C183,C206	
*					C208,C211,C212	
47	3	KEMET T354H336K016AS	33UF 16V RADIAL Dip	.85	C18,C26,C53	
48	2	LITTLEFUSE 251010 Newark 20F604	10 AMP PCB Fuse	0.74	F1,F2	
49	1	MACH 110-12JC	AMD PLD 44 Pin PLCC	7.00	U25	
50	2	MC10E116	QUINT differential Line Receiver	10.00	U40,U76	
51	1	MC10H350	PECL Receiver	10.00	U51	
52	2	MOTOROLA 1N5908	Transient Suppressor 6.0V	1.24	D7,D8	
53	3	PALCE22V10H-7PC	Programmable Logic Device	5.00	U10,U34,U47	
54	15	PAN ECS-H1CC106R DIG PCT3106	SMT CAP 10.0UF	0.9765	C2,C5,C6,C11,C13	
*					C14,C15,C24,C28	
*					C30,C31,C36,C37	
*					C41,C52	
55	1	PAN ECS-H1CY105R DIG PCT3105	SMT CAP 1.0UF	0.3955	C48	
56	11	PAN ECU-V1H103KBG DIG PCC103BN	SMT CAP 0.01UF	0.168	C7,C9,C29,C32,C39	
*					C46,C90,C101,C102	

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Fermi National Accelerator
Particle Physics Division
ET&T - CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF DESG
*					C119,C205
57	5	PAN ECU-V1H103KBM DIG PCC103BCT	SMT CAP 0.01UF	0.168	C19,C50,C51,C92
*					C93
58	152	PAN ECU-V1H104KBW DIG PCC104B	SMT CAP 0.1UF	0.5914	C3,C4,C12,C16,C21
*					C23,C27,C33,C34
*					C35,C38,C42,C43
*					C44,C45,C49,C54
*					C55,C58,C60,C62
*					C63-C89,C91,C94
*					C95-C100,C103
*					C105-C118,C120
*					C121-C131,C133
*					C134-C136,C138
*					C139-C146,C148
*					C150,C152,C153
*					C154-C156,C158
*					C159,C160,C162
*					C163-C166,C168
*					C169-C180,C184
*					C185-C204,C207
*					C209,C210,C213
*					C214,C215,C245
59	6	PAN ECU-V1H561JCX DIG PCC561CGCT	SMT CAP 560pF	0.125	C8,C10,C20,C22
*					C40,C47
60	40	PN32	test point		GP1-GP18,TP18
*					TP23,TP24,TP31
*					TP32,TP33,TP40
*					TP44-TP58
61	5	RC05-270 1487-0290	270 ohm 1/8W 5%	0.19	R1,R3,R4,R6,R7
62	1	RC05-820K 1487-0497	1/8W 820Kohm 5%	0.18	R5
63	3	RC05-1000 1487-0325	1000 ohm	0.18	R14-R16
64	1	RC07-1.5M 1487-1125	1/4W, 5PCT, THRU	0.14	R76
65	2	RC07-1M 1487-1105	1/4W, 5PCT, THRU	0.19	R2,R77
66	1	RC07-5.6 Digi 5.6QBK-ND	1/4W, 5PCT, THRU	0.06	R75
67	5	RC07-4700 1487-0825	1/4W, 5PCT, THRU	0.08	R10-R13,R36

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Fermi National Accelerator
Particle Physics Division
ET&T - CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF DESG
68	1	RN55C-13K	1/8W 1PCT Thru	0.04	R19
69	3	RN55C-27K	1/8W 1PCT Thru	0.04	R20-R22
70	2	RN55C-84.5	1/8W 1PCT Thru 249 Ohm	.04	R62,R63
71	1	RN55C-100K	1/8W 1PCT Thru	0.04	R18
72	1	RN55C-249 1487-4365	1/8W 1PCT Thru 249 Ohm	.04	R61
73	13	SN74ABTE16245SSOP	16 Bit Incident Transceiver	5.60	U1,U7,U8,U21,U33
*					U45,U46,U54,U59
*					U60,U65,U66,U75
74	1	SN74ABTE16246SSOP	11 Bit Incident Transceiver	7.50	U14
75	3	Samtec TSW-12-07-L-D 2pin sip	2 pin jumper - mates with SNT-100-BK-G \$	0.16	S1-S3
76	8	Spare-IC 24DIP3	Spare 24 pin DIP	0.00	U67-U74
77	36	TEST_PIN	.025 x .025 square post.	.01	TP1-TP17,TP19
*					TP20-TP22,TP25
*					TP26-TP30,TP34
*					TP35-TP39,TP41
*					TP42,TP43
78	1	TIBPAL16L8-5C	Programmable Logic Device	5.00	U13
79	1	TOP d strip	Top Discharge strip	.01	X1
80	43	VCC Via	VCC-Via	.00	VP1-VP25,VP51
*					VP52,VP54,VP55
*					VP56-VP61,VP66
*					VP67-VP73
81	1	XC3130A-1PQ100C	Xilinx XC3130A Logic Cell Array	35.00	U4
82	1	XC4005EPQ100-3	Xilinx FPGA	60.00	U19
83	1	XC4013E-3PQ240C	Xilinx FPGA	250.00	U6
84	1	XC17128-PD8C	XILINX PROM	13.00	U20
85	2	XC17256-PD8C	XILINX PROM	13.00	U3,U12
86	2	mc10h3511	Quad TTL to PECL translator.	10.00	U36,U55
87	15	res_spare1206	1/8W 1% 1.0K ohm	0.00	R8,R9,R27,R31,R33
*					R38,R47,R57,R58
*					R59,R60,R64,R66
*					R67,R69
88	1	1N5817	Scottky Diode	.80	D9
89	1	3 pin jump 3SIP60 TSW-12-07-L-D	3 pin jumper	0.30	U24
90	1	10x-2-102	10 pin 1K SIP, pin 1 common	1.50	RP1

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Fermi National Accelerator
Particle Physics Division
ET&T - CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF DESG
91	1	74F04N	hex inverter	0.53	U53
92	2	74F38N	Open collector nand	0.53	U5,U64
93	1	74LS14N 1455-8014	schmitt trigger inverter	0.31	U77
94	1	74LS123N 1455-8123	Multivibrator	0.35	U2
95	4	2503-5020-UG 3M 20pin Rt Ang HDR	3M 20 pin right angle header		J7-J10
96	6	2743021446 PSC ELECTRONICS	SMT FERRITE BEAD 10UH	1.30	L1-L6

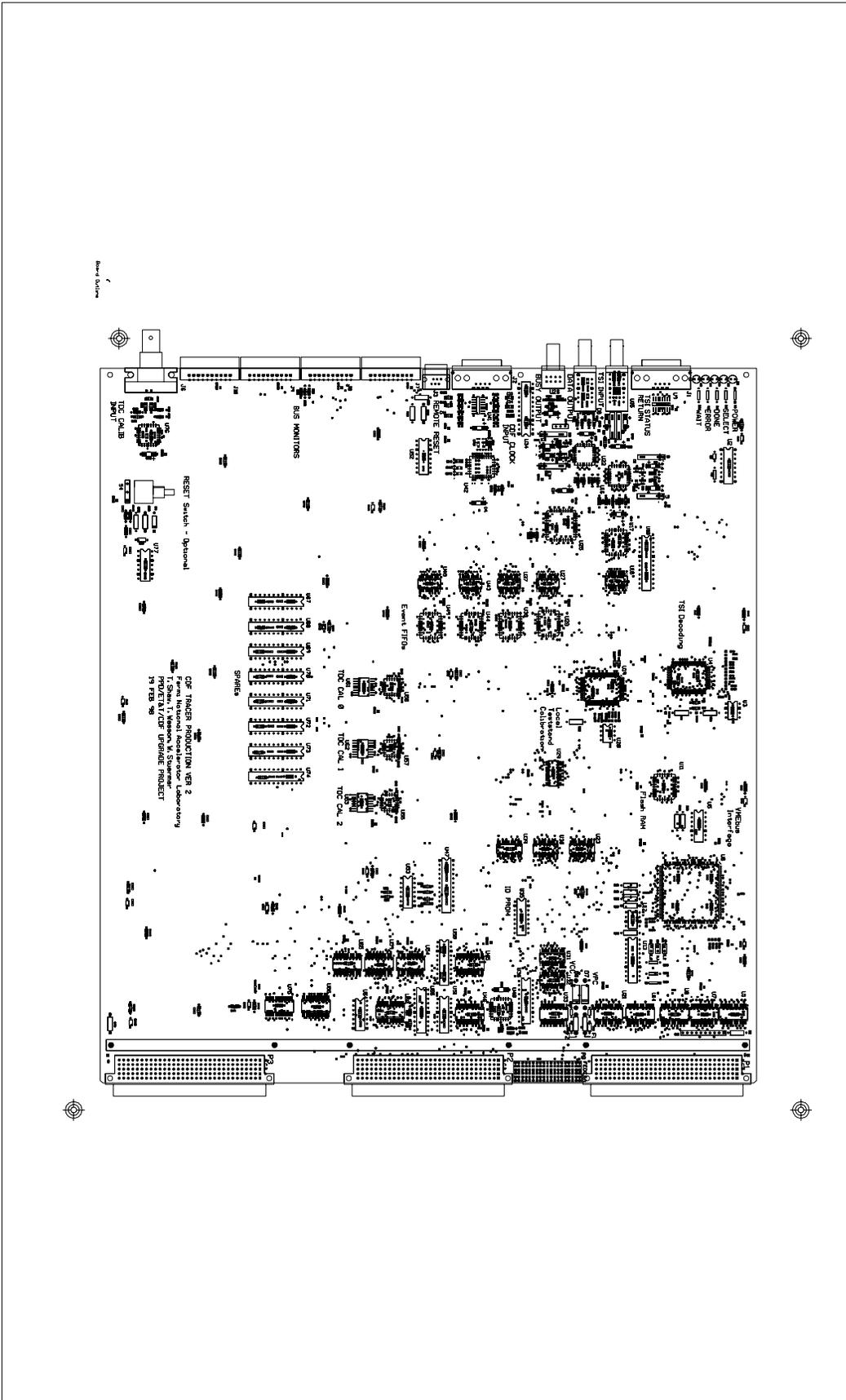
Total Parts Used: 603
Total Parts Cost: 1313.37
Board Cost ~ \$300
Board Assemble ~\$150

TOTAL ~ \$1770

APPENDIX B

TRACER PCB VIEW

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APPENDIX C

Master Clock and TSI Cabling Note

T_M_SHAW 060396

Revised 6/14/96

Proposal for Master Clock Fanout Cable and TSI Return Cable

A set of proposals were made at the end of the CDF infrastructure meeting on May 22, 1996 on how to cable the TSI return signals and the Master Clock. What follows is the result after feedback from all (we hope) systems.

Master Clock Fanout Cabling

- Assume the use of National's LVDS differential line drivers and receivers. P/Ns are DS90C032 and DS90C32. Testing done by Steve Chappa has verified that there are no problems with these devices.
- Cable Termination at the Receiver end should consist of a SMT resistor (100 ohms) across the differential inputs which matches the cable impedance.
- While most systems require 4 signals, at least one system (SVX) has identified the need for five signals. It was decided at the clock meeting on 6/13/96 to simply run an additional "CABLE B" to such systems. CABLE B will contain the 53Mhz clock required by SVX.

This decision allows us to continue to use the high quality Category 5 cable we have tested (4 pair limit), as well as the connectors. CABLE A and CABLE B will have different keys to prevent them from being switched at front panels.

CABLE PINOUT for CDF Readout Crate with TRACER

CABLE A

<u>Pin</u>	<u>Signal</u>	
1	Master_Clock	(132 ns clock)
2	Master_Clock*	
3	Beam_Crossing	
4	Beam_Crossing*	
5	Beam_Zero	(once around marker)
6	Beam_Zero*	
7	Abort_Gap	
8	Abort_Gap*	

CABLE B

Not Required

CABLE PINOUT for “SVX-like” Readout Crate**CABLE A**

<u>Pin</u>	<u>Signal</u>	
1	Sync	(one tick every 132 ns clock)
2	Sync*	
3	Beam_Crossing	
4	Beam_Crossing*	
5	Beam_Zero	(once around marker)
6	Beam_Zero*	
7	Abort_Gap	
8	Abort_Gap*	

CABLE B

<u>Pin</u>	<u>Signal</u>	
1	53MHz_Beam_Clk	(one tick every 132 ns clock)
2	53MHz_Beam_Clk*	
3	N/C	
4	N/C	
5	N/C	
6	N/C	
7	N/C	
8	N/C	

BOARD MOUNT CONNECTORS

(AMP Catalog 82101)

CABLE A

AMP Shielded Data Link Connectors, 8 Conductor, Side Entry Panel and PCB Ground

Part # 3-520459-3

(Note: this part uses the “C” key to distinguish it from the TSI return cable)

CABLE B

AMP Shielded Data Link Connectors, 8 Conductor, Side Entry Panel and PCB Ground

Part # 5-520459-3

(Note: this part uses the “E” key to distinguish it from the TSI return cable)

CABLE CONNECTORS

Cable - Plug Assemblies for Round Cable (order 1 part each per cable end)

Sub- assembly	Part # 3-520424-3	“C” key
Sub- assembly	Part # 5-520424-3	“E” key
Top Shield	Part # 520464-1	
Bottom Shield	Part # 520465-1	
Ferrule	Part # 520437-1	
Boot	Part # 520853-1	

Trigger System Interface - DONE, BUSY, ERROR cable

- The proposal is to use the same differential line drivers, National's LVDS DS90C032 and DS90C32 as we are using for the clock fanout.
- The same PCB board mount and cable connectors will be used, with the exception that these will have "A" key coding. This is being done to prevent someone from mixing the TSI return cables with the clock fanout cables.

Board Mount Connectors:

AMP Shielded Data Link Connectors, 8 Conductor, Side Entry PCB Ground
Part # 1-520459-3 "A" Key

Cable - Plug Assemblies for Round Cable (order 1 part each per cable end)

Sub- assembly	Part # 1-520424-3 "A" Key
Top Shield	Part # 520464-1
Bottom Shield	Part # 520465-1
Ferrule	Part # 520437-1
Boot	Part # 520853-1

PINOUT

<u>Pin</u>	<u>Signal</u>
1	DONE
2	DONE*
3	ERROR
4	ERROR*
5	BUSY
6	BUSY*
7	L1_DONE (This signal is unique to SVX)
8	L1_DONE*

Other Useful Part Numbers

Hand Tools required for Cable assembly

Connector Hand Tool Frame	Part # 58194-1
Die Sets for Connectors	Part # 58195-3
Ferrule Hand Tool Frame	Part # 69710-1
Die Sets for Ferrules	Part # 1-58166-2

Cable

Teststand use:

Category 5, PVC jacketed Cables/overall Bedfoil Shield, 4 Pair Part # 1633A
Available Now

Category 5, Plenum-Paired Cables/overall Bedfoil Shield, 4 Pair Part # 1646A
Available 1/97
(Beldon Wire and Cable Catalog)