



Cable Tests

XFT Project

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Introduction

The XFT project will need a method of transporting data from the TDC modules up to the FINDER modules and the FINDER modules need a method for transporting data to the LINKER modules. We constructed the following test stand shown in the block diagram below to validate a few methods that may be incorporated into the XFT project. The test stand allows us to verify the ability of two logic families: LVDS and ECL to drive and receive data over a 200' ANSLEY cable and also over a 200' ANSLEY cable with a 10' piece of twist-n-flat cable attached to the receiver end of the ANSLEY cable. Tests that are performed will tell us: 1. Skew between channels on the cable, 2. Width of valid data that is available after a 200' transmission. 3. Pulse shape and crosstalk that can be expected at the receiver end of the cable.

The FINDER to LINKER connection may use the National Semiconductor's Channel Link driver and receiver pair. This test setup allows us to verify the data rate and cable length that can be implemented in the FINDER to LINKER connection.

The test setups and descriptions are listed on the next 8 pages with the findings from the tests following them. There are lots of pictures that have been incorporated into this document, most of these pictures originated in .TIF or .BMP format. Information on the Driver board and Receiver board along with information on the instruments used can be obtained from the authors.

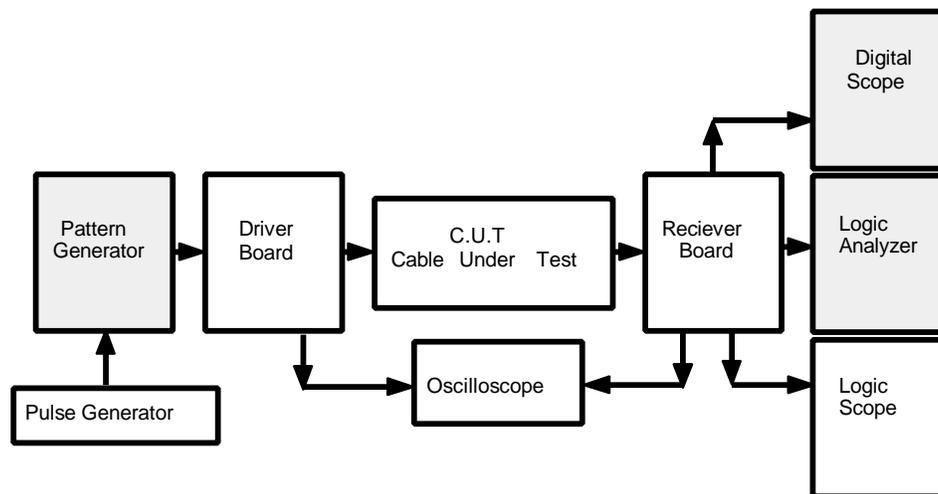


Figure 1. Block Diagram

The following 3 modules are housed in the HP 16500A Logic Analysis System.

Pattern Generator: HP 16522A 200M Hz. Pattern Generator Module. This module is capable of being loaded with a random pattern that is 24 bits wide and 500 deep. The Generator connects to the system with the use of HP 10461A TTL Data Pod or HP 10464A ECL Data Pod(terminated). TTL Clock signals use the TTL HP 10460A clock pod.

Logic Analyzer: HP 16510B 100M Hz./500M Hz.

Digital Scope: HP 16532A 1 GSa/s Digitizing Oscilloscope.

Scope Probe(1): HP 10433A 10:1 probe, 10M/10pf.

Differential Scope probe(1): TEK P6046 Differential probe and Amplifier.

When using the Differential Probe and Amplifier set the Digitizing Scope to 10mv/div, 50 ohm DC input, 1:1 scope probe. The setting on the Amplifier sets the horizontal scale per division seen on the screen of the scope.

Logic Scope: TEK TLS 216 Logic Scope 2 GSa/s.

Scope Probe(15): TEK P6240 10:1 probe, 1M/2.5pf. The 15 individual probes were calibrated to the scope channels that they plugged into.

Oscilloscope: TEK 2467B 400M Hz.

Scope Probe(2): TEK P6137 10:1, 10M/10.8pf, 1.5M

Pulse Generator: HP 8130A 300M Hz. Pulse Generator.

Driver Board: FERMILAB design, this 4 layer board is a 9U VME based board that contains a ground and power plane. IC Components on the board consist of the following three types: 24 - ECL Drivers(six 10H101 ICs), LVDS Drivers(six National Semiconductor DS90C031 ICs) and a National Semiconductor DS90CR211 Parallel to Serial Channel Link driver(1 IC). The board receives its power from the VMEBUS backplane, the -5.2v required by the ECL drivers is generated through the use of a linear regulator which receives an input of -12v which is supplied on the backplane of the crate. The three output connectors on the front of the board are respectively connected to the three different types of drivers. The LED's on the front show the presence of the supply voltages on the board.

C.U.T. :

ANSLEY cables(4) that are 200.0 +/- .1 ft long with 24 differential signal channels with a ground between adjacent differential pairs for a total of 76 wires, 28 awg. solid.

AMPHENOL SPECTRA STRIP twist-n-flat cable #132-2801-050 28 awg. stranded.

BELDEN - M DATATWIST(R) 1633A - CATEGORY 5 cable, 4pr. twisted 24 awg. solid cu. wires with shield and drain wire.

Receiver Board: FERMILAB design, this 6 layer board is physically similar to Driver board with the exception of two additional signal layers, the ground and power plane layers are the inner two layers. IC Components on the board consist of the following three types: 24 - ECL Receivers/Translators(six 10H125 ICs), LVDS Receivers(six National Semiconductor DS90C032 ICs) and a National Semiconductor DS90CR212 Serial to Parallel Channel Link Receiver(1 IC).

ECL Logic

TEST A1 - STEP TEST

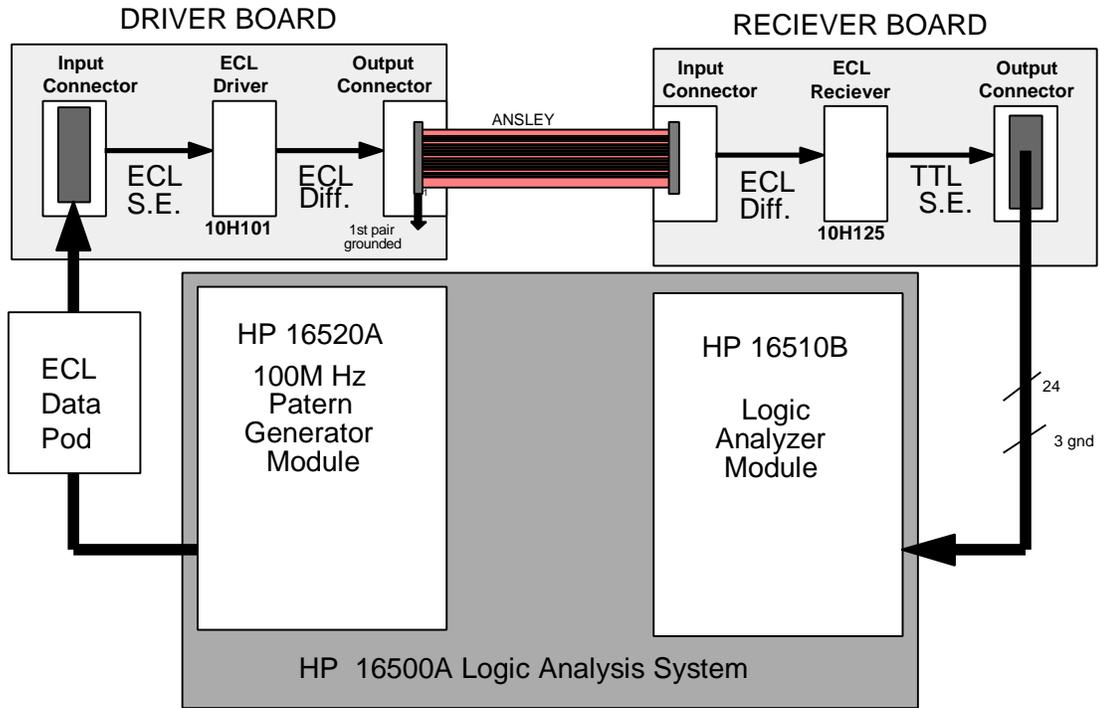


Figure 2. Test setup #1.

Function: To validate the connection and operation of the drivers, receivers and four cables operating at 50M Hz .

Procedure: Setup test as shown in figure 2. The pattern generated for this test should be a stepping pattern as shown in figure 3.

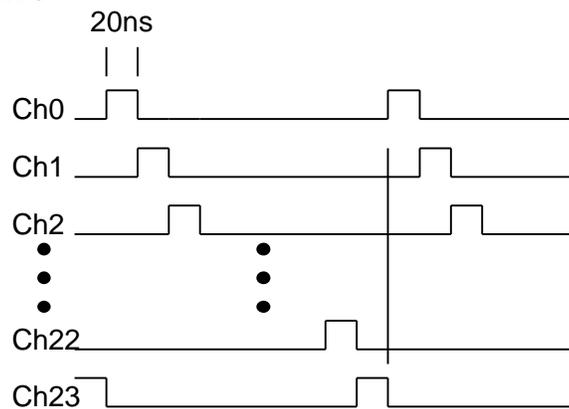


Figure 3. Stepping pattern.

Results: Record waveform of the Logic Analyzer input, verify that the inputs match the pattern generated.

TEST A2 - SKEW TEST

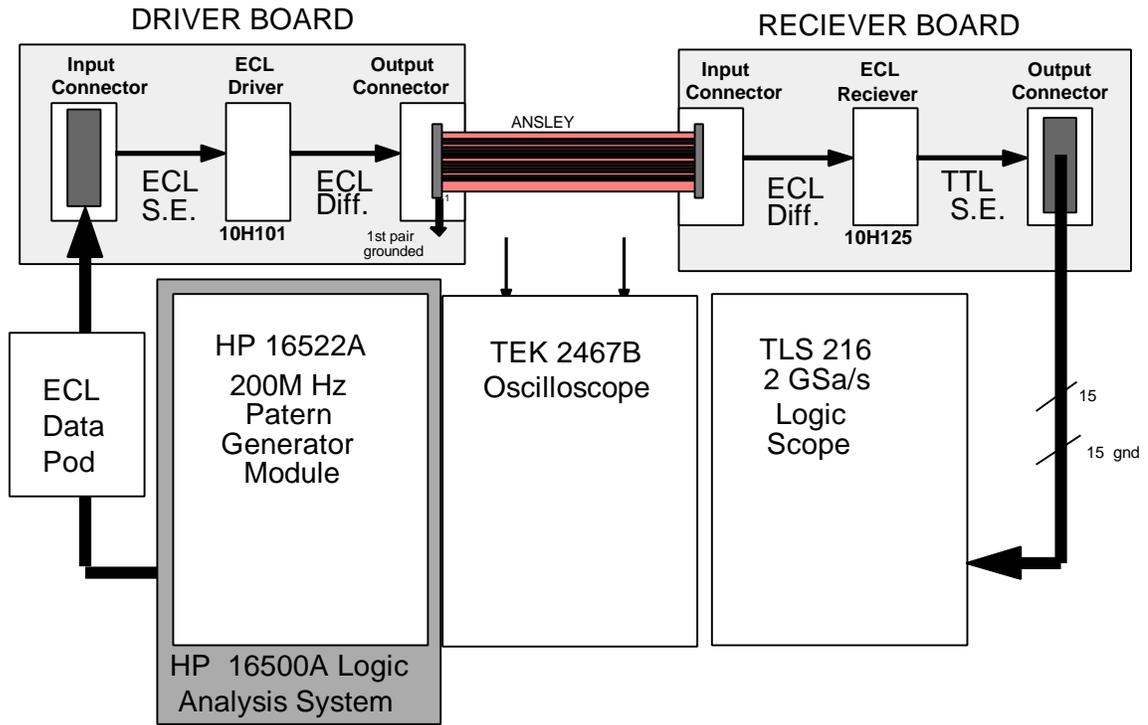


Figure 4. Test Setup #2.

Function: To determine the maximum skew across the channels.

Procedure: Use setup shown in figure 4. The pattern generated for this test is as shown in figure 5.

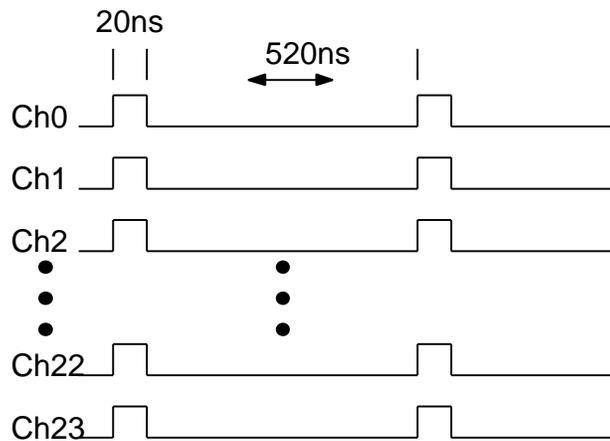


Figure 5. Skew test pattern.

Results: Using the Logic Scope record the skew between the 24 channels. The Logic Scope has 15 channels and there are 24 outputs so save the first 9 channels with waveform save option and then move the probes to the next 9 channels and recall the first 9 waveforms that were saved. The screen will now contain 24 waveforms, use the measure function to record the worst case skew shown between the channels(The trigger will need to come from one of the channels that is not moved).

Using a TEK 2467B Oscilloscope trigger off of one of the inputs to the drivers with one channel and using the other channel record the skew between all channels at the inputs to the drivers (this skew is a function of the HP16522A and the data pods). Subtract the skew found with the TEK 2467B Oscilloscope from the skew found with the Logic Scope, the result is the maximum skew between channels.

TEST A3 - EYE TESTS

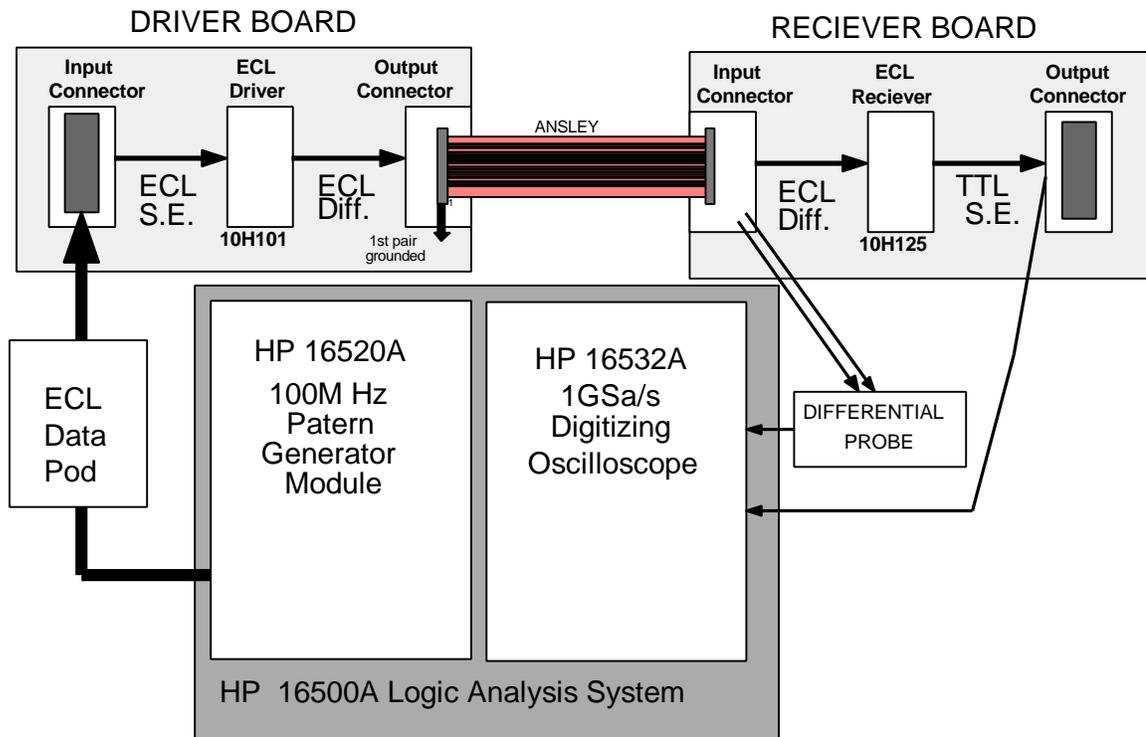


Figure 6. Test Setup #3.

Function: To reveal the width of valid data available at the receiver after being transmitted across 200' of cable.

Procedure: Use setup shown in figure 6. Load the Pattern Generator with 500 random patterns and set to repetitive run. Trigger the Digitizing Oscilloscope on the clock coming out of Pattern Generator's clock pod output.

Results: Record measurement of eye opening of all channels going into receivers using Digitizing Oscilloscope and Differential probe.

TEST A4 - STEADY STATE HIGH TEST

Function: To reveal pulse shape on cable after being in a high steady state.

Procedure: Use setup shown in figure 6. Set the Pattern Generator to pulse low for 20ns on one channel with all other channels remaining in a high steady state, repeat test with all channels pulsing low at the same time.

Results: Trigger Digitizing Oscilloscope on channel being pulsed and record pulse at receiver input with the Differential probe and also at the receiver output. View all channels noting the pulse shape, record observations of pulse shape on channels located on the end and middle of the cable.

TEST A5 - STEADY STATE LOW TEST

Repeat above test with a pulse going high for 20ns and then returning to a low steady state.

TEST A6 - CROSSTALK TEST

Function: To show the crosstalk between pairs of wires in the cable.

Procedure: Use the setup shown in figure 6. Disconnect a cable pair from the middle of the cable at the driver end of the cable using a switch block (INTRASWITCH 922578-50) that plugs into the connector on the Driver board with the cable plugging in to the other side of the switch block. Setup the Pattern Generator to provide a pattern as shown in figure 7, the pattern on the channels other than Ch9, Ch10 and Ch11 should be random if possible.

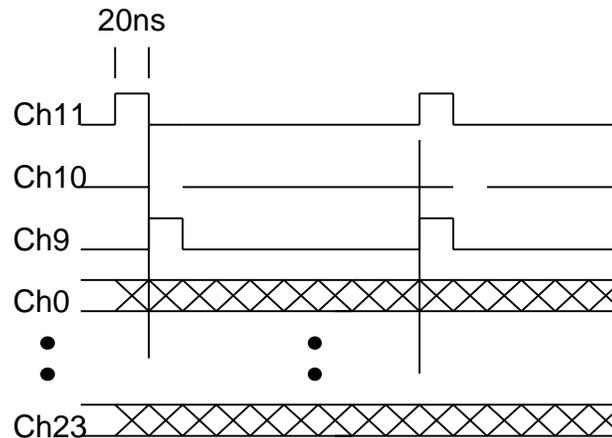


Figure 7. Crosstalk Pattern.

Results: Using the Differential probe of the Digitizing Oscilloscope record the crosstalk present on the floating cable pair at the input to the receivers and also the adjacent channels being pulsed at the output of the receiver.

TEST B1-B6

- Repeat TEST A1 -A6 with a 10 foot twist and flat tail on the receiving end.

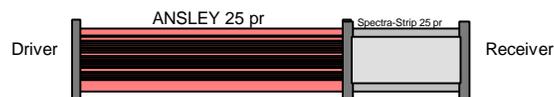


Figure 8. Ansley Cable with 10' Twist-n-Flat attached.

LVDS Logic

- Repeat TESTS A1- A6 and B1-B6 which were done for the ECL drivers and receivers using the LVDS drivers and receivers.

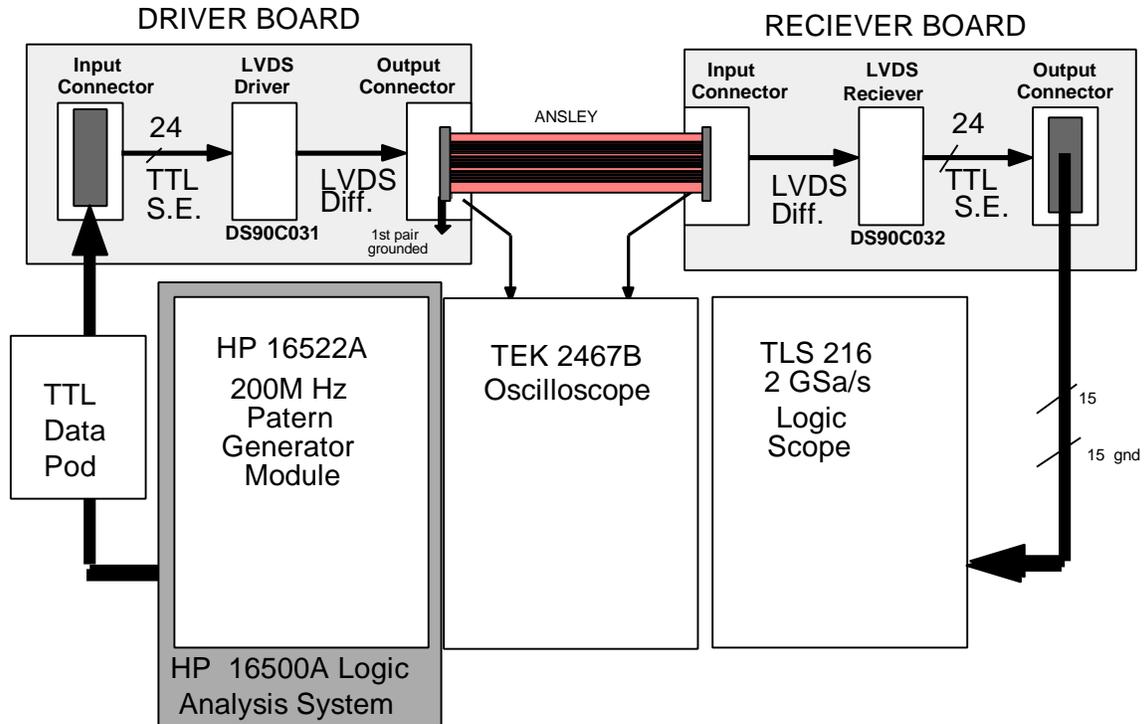


Figure 9. Test Setup For LVDS Driver/Receiver..

National Channel Link

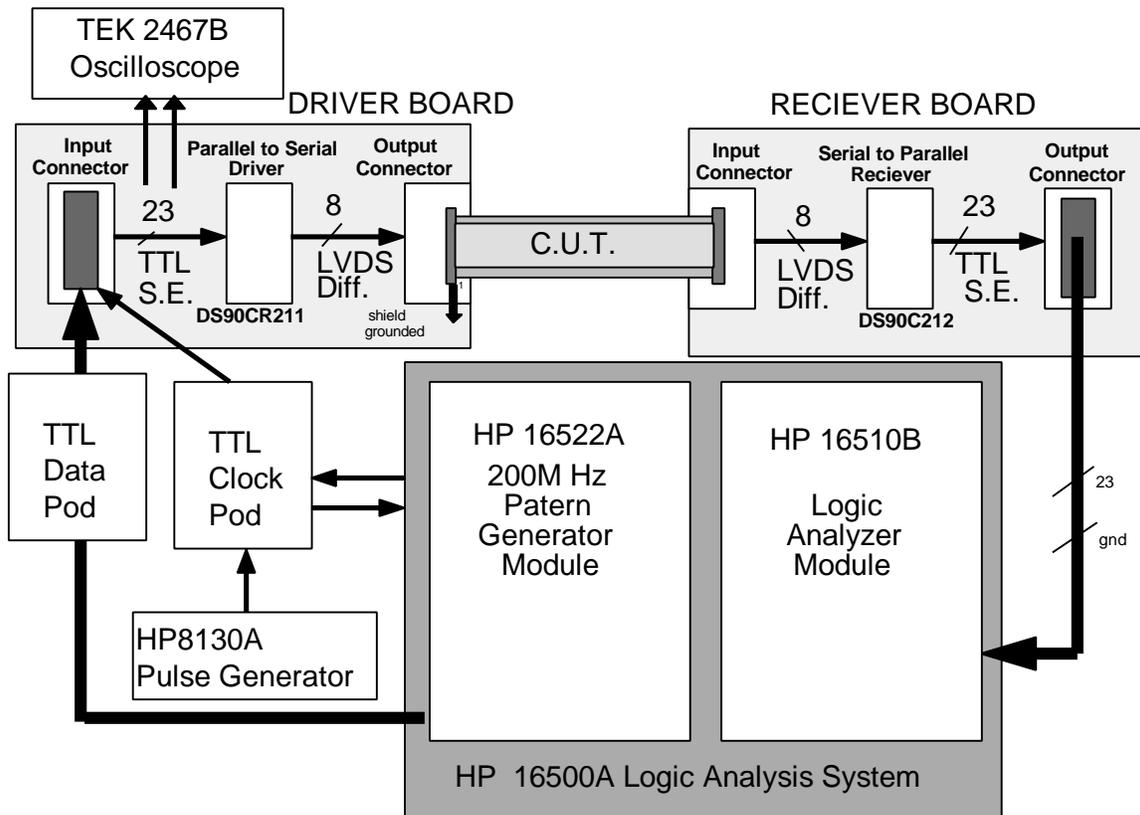


Figure 10. Test Setup for Channel Link Driver/Receiver.

TEST C1 - CHANNEL LINK - TWIST-N-FLAT CABLE

Function: Find out how far we can drive data over a twist and flat cable using the National Semiconductor DS90CR211/212 Channel Link Parallel to Serial Driver and Receiver. (The recommended length is no more than 10 meters on a high quality cable). Test at speeds 25M Hz, 30M Hz, and 40M Hz.

Procedure: Use test setup shown in figure 6. Use the stair step pattern generated illustrated in figure 3 as an input to the driver, the clock will come from the Pattern Generator through the TTL Clock Pod. The HP 16522A will not supply a 30M Hz. clock so use the external clock option and connect the HP8130A to the TTL Clock Pod Input when testing at 30M Hz.(use a 50 ohm termination at the clock pod input). The Pattern Generator has a method of delaying the clock signal out with respect to the data out. Use the TEK 2467B scope to record the delay between the clock signal and the data for all 10 clock delay settings at the input to the driver.

Connect a 30ft. twist-n-flat cable between the driver and receiver board. Set the Pattern Generator to run at 25M Hz. and view the data coming from the receiver board with the Logic Analyzer set to accumulate mode. If the pattern viewed at the Logic Analyzer is corrupted adjust the clock delay until the pattern is correct or if needed reduce the length of the cable in 20"(spacing of flat areas) increments until the data is correct.

Result: Record the cable length and clock delay settings that produced the correct pattern. Repeat with the Pattern Generator running at 30M Hz. and then again at 40M Hz.

TEST C2 - CHANNEL LINK - CATEGORY 5 CABLE

Function: Find out how far we can drive data over a Category 5 cable using the National Semiconductor DS90CR211/212 Channel Link Parallel to Serial Driver and Receiver. (The recommended length is no more than 10 meters on a high quality cable). Test at speeds 25M Hz, 30M Hz, and 40M Hz.

Procedure: Replace the twist-n-flat cable with the BELDEN 1633A Category 5 cable. Solder the 4 pairs of wires to the appropriate pins on a 50 pin ribbon cable connector so that it will plug into the 50 pin header on the boards. On the Driver board side of the cable connect the drain wire to pin 1 of the connector which will connect the shield to ground of the Driver board. Start with a 30 ft. length of cable and the Pattern Generator running at 25M Hz. reduce the cable in 5 ft. increments until the pattern viewed with the Logic Analyzer is not corrupted.

Result: Record the cable length and clock delay settings that produced the correct pattern. Repeat with the Pattern Generator running at 30M Hz. and then again at 40M Hz.

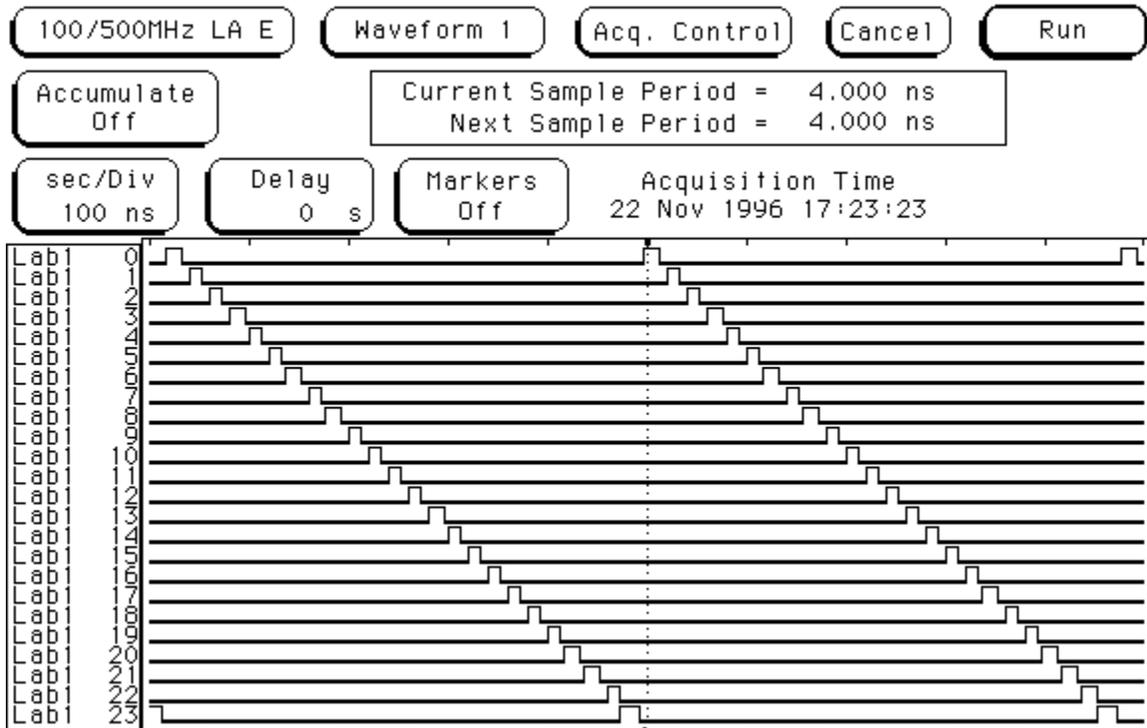
TEST RESULTS

LVDS Logic with ANSLEY CABLE TEST RESULTS

The first tests performed were done with the LVDS driver sending data across ANSLEY cable #4. The recorded waveforms were stored in files with a .TIF or .BMP format.

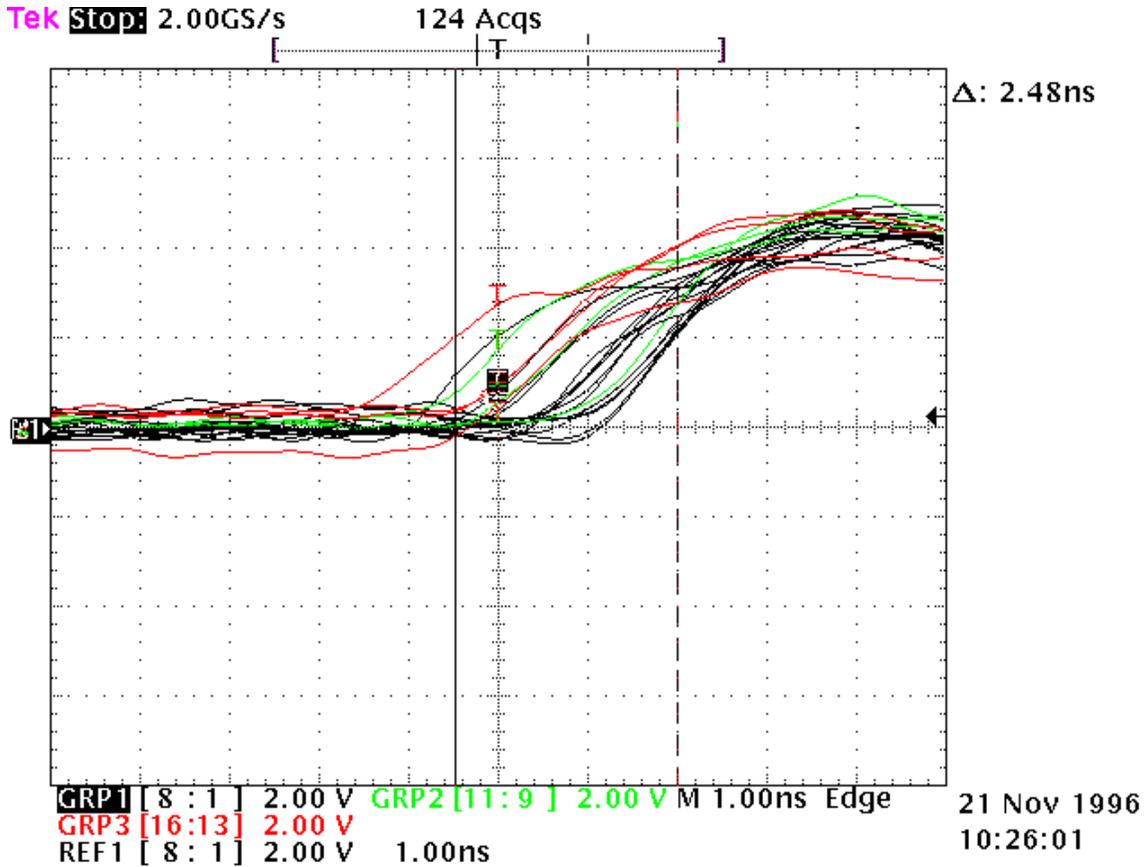
TEST A1: LVDS - Cable #4 Step Test

The following picture shows the output of the LVDS Receiver, the waveform was observed with the Logic Analyzer. The input pulse width was set to 20ns. This resultant waveform verifies the connection and functionality of the drivers, receivers and cable under test.



TEST A2: LVDS - Cable #4 Skew Test

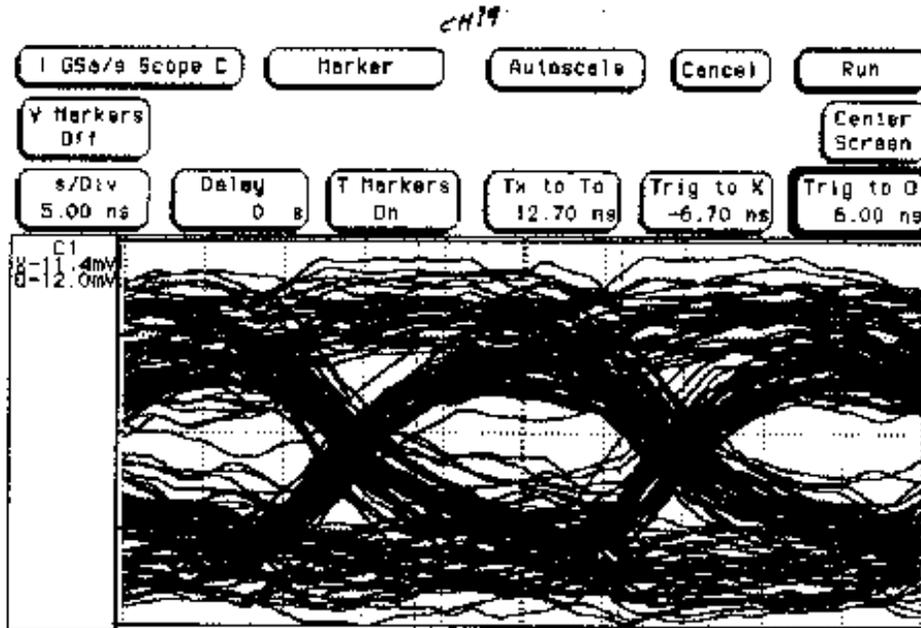
The following picture shows the skew between outputs of the 24 LVDS Receivers, the waveform was observed with Tektronix TLS 216 Logic Scope. The total skew for the system was as shown: 2.48ns and occurred between channel 5 and channel 16. The skew measured between the inputs of the drivers was found to be 1.26ns. The skew measured between the outputs of the receivers and the input to the Logic Scope was found to be 0.1ns. The skew through the cable and drivers was then found by subtracting: $2.48\text{ns} - 1.26\text{ns} - 0.1\text{ns} = 1.12\text{ns}$.

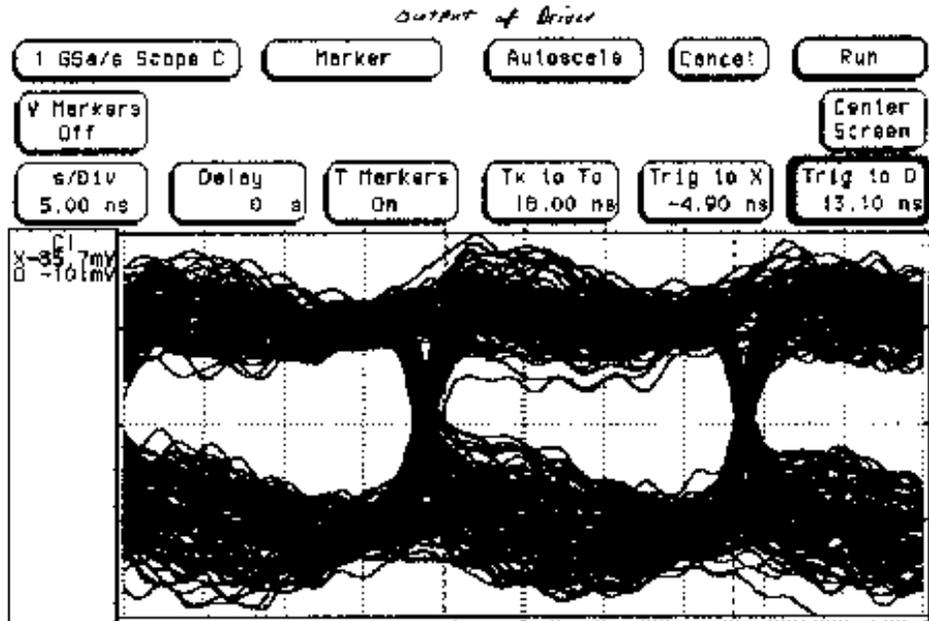
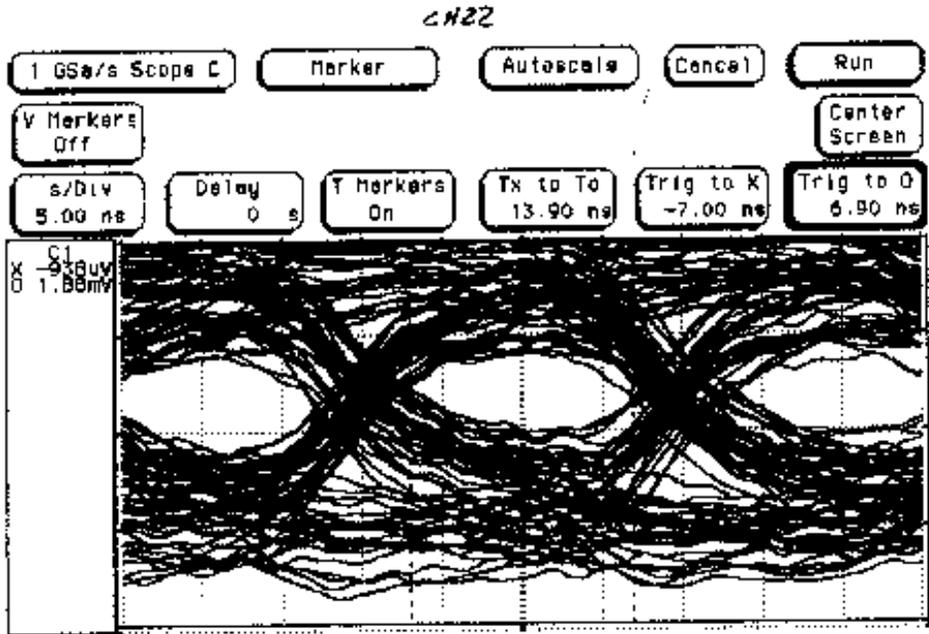


TEST A3: LVDS - Cable #4 I-Test

The following three pictures shows the differential inputs of channel 19 and 22 and channel 0's drivers output as observed with the differential probe. The measured width of the eye opening for all the channels is shown in the following chart.

CHANNEL NUMBER	WIDTH OF EYE OPENING
0	13.4ns
1	12.3ns
2	12.1ns
3	13.4ns
4	12.0ns
5	13.7ns
6	13.0ns
7	12.1ns
8	14.0ns
9	14.0ns
10	12.5ns
11	12.2ns
12	12.6ns
13	12.6ns
14	12.4ns
15	13.3ns
16	12.0ns
17	11.2ns
18	11.2ns
19	11.1ns *worst
20	11.9ns
21	13.8ns
22	14.6ns *best
23	14.2ns

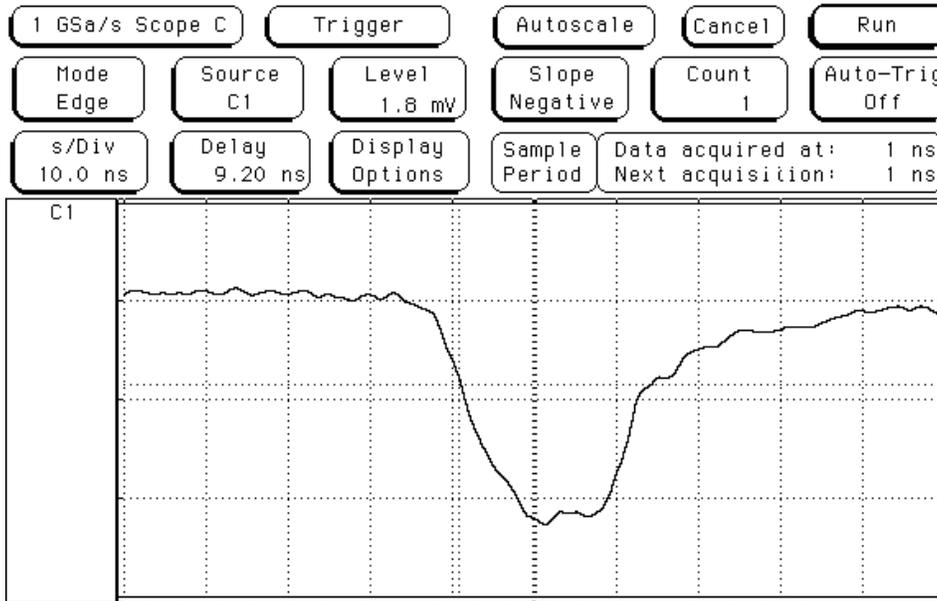
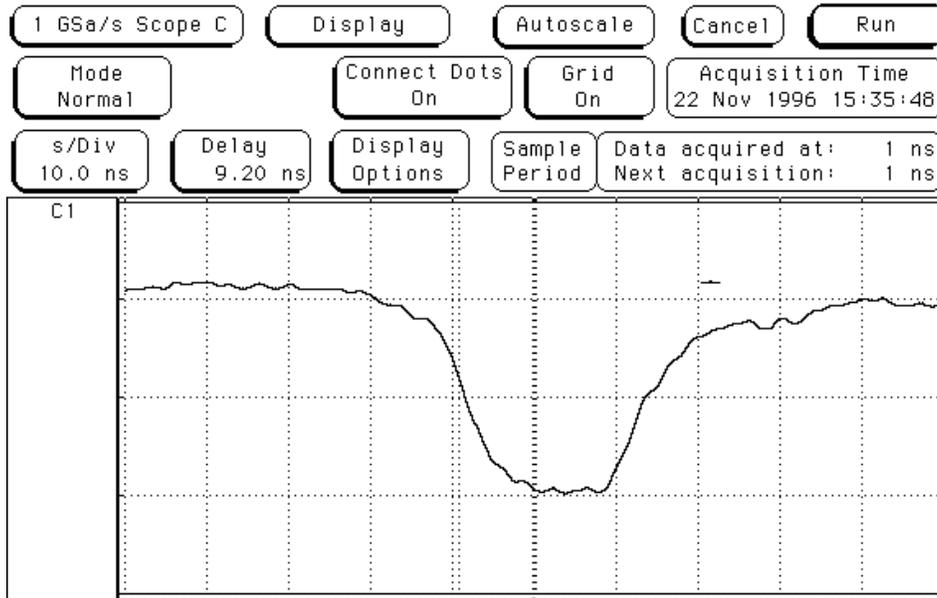


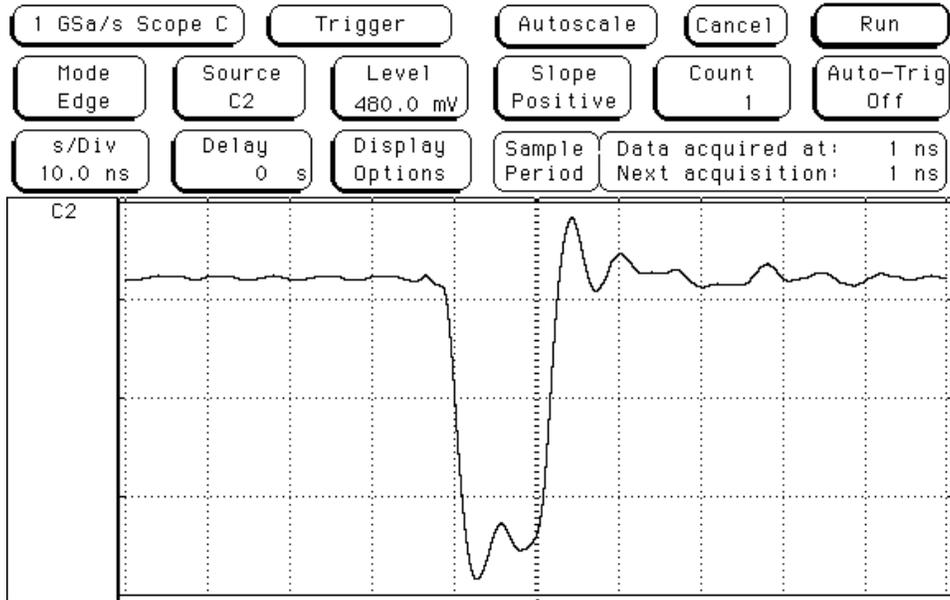
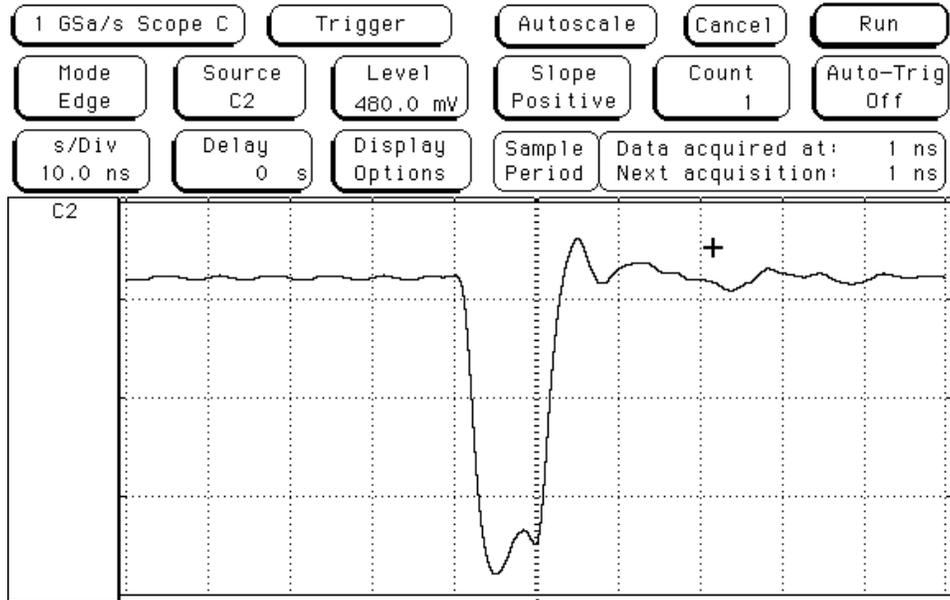


TEST A4: LVDS - Cable #4 Steady State - High Test

The 1st picture below shows the differential input of channel 0 receiver as measured with the differential probe. The single low going pulse provided to only the channel 0 driver was 20ns wide. The Horizontal scale per division is 200mv/div.

The channel being driven(viewed) was incremented so that the differential pulse shape present on all of the inputs to the receivers could be observed, there was only a minimal amount of pulse shape changes between channels. The 2nd picture is also of channel 0 at the differential input to the receiver, this picture shows the pulse shape when all the channels are being driven with one low going 20ns pulse at the same time. The 3rd and 4th picture are of the output of the channel 0 receiver and correspond to the 1st and 2nd pictures, these pictures depict the width of the data pulse the receiver will produce in the two cases. The horizontal scale per division in these last two pictures are 2v/div.

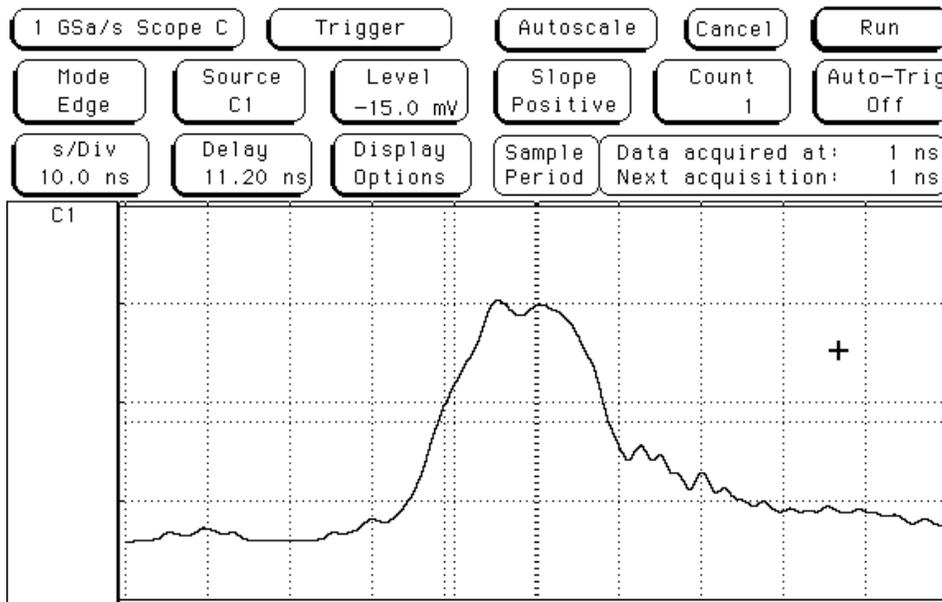
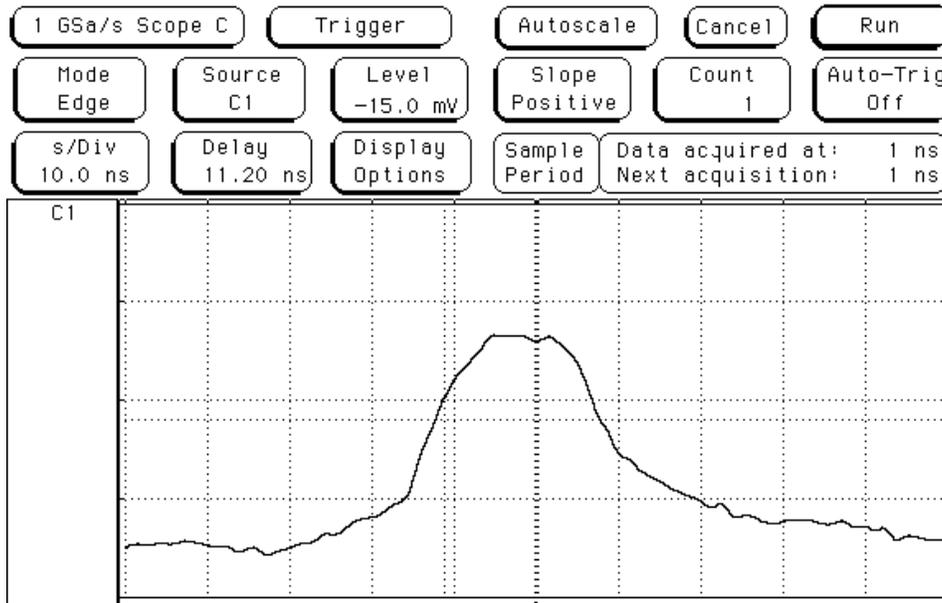


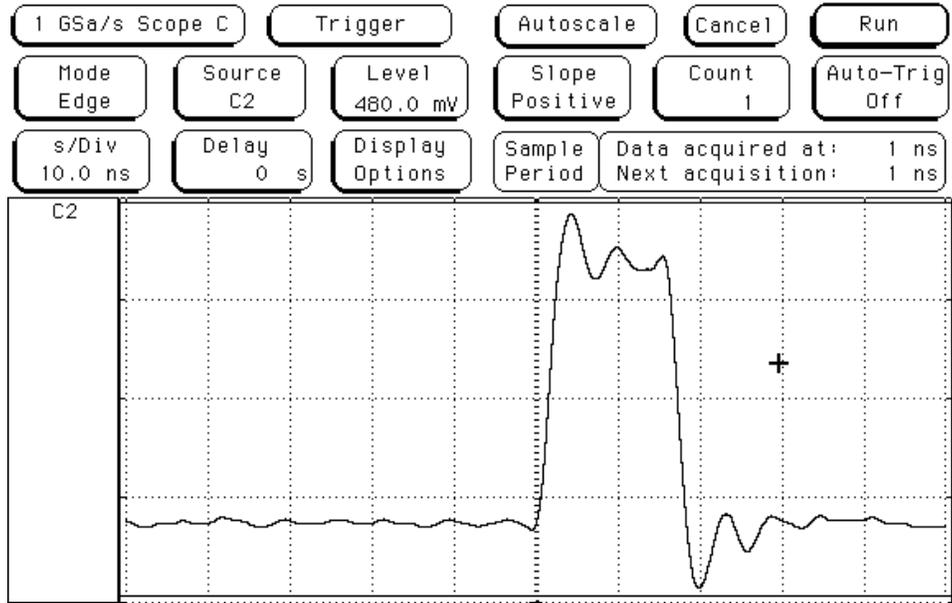
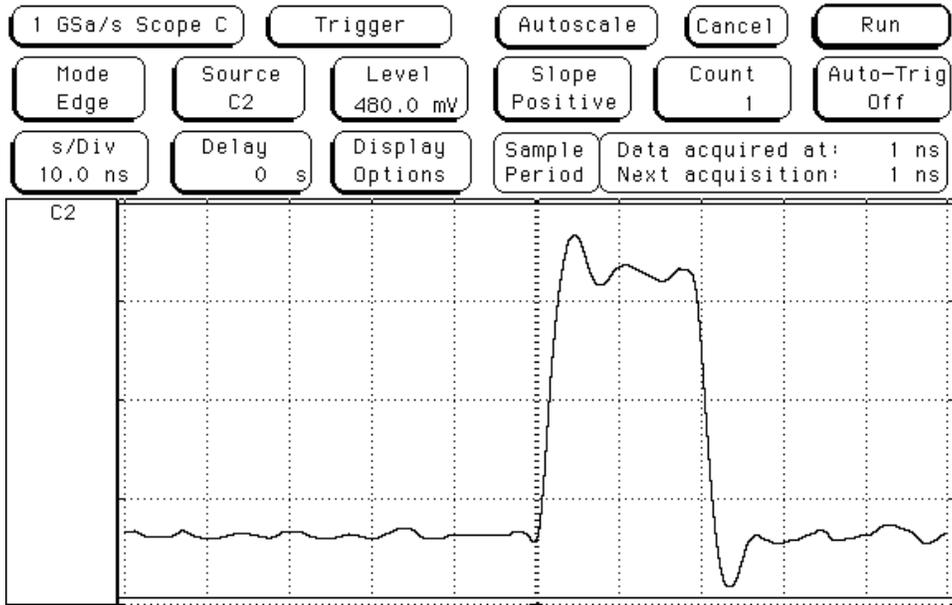


TEST A5: LVDS - Cable #4 Steady State - Low Test

The 1st picture below shows the differential input of channel 0 receiver as measured with the differential probe. The single high going pulse provided to only the channel 0 driver was 20ns wide. The Horizontal scale per division is 200mv/div.

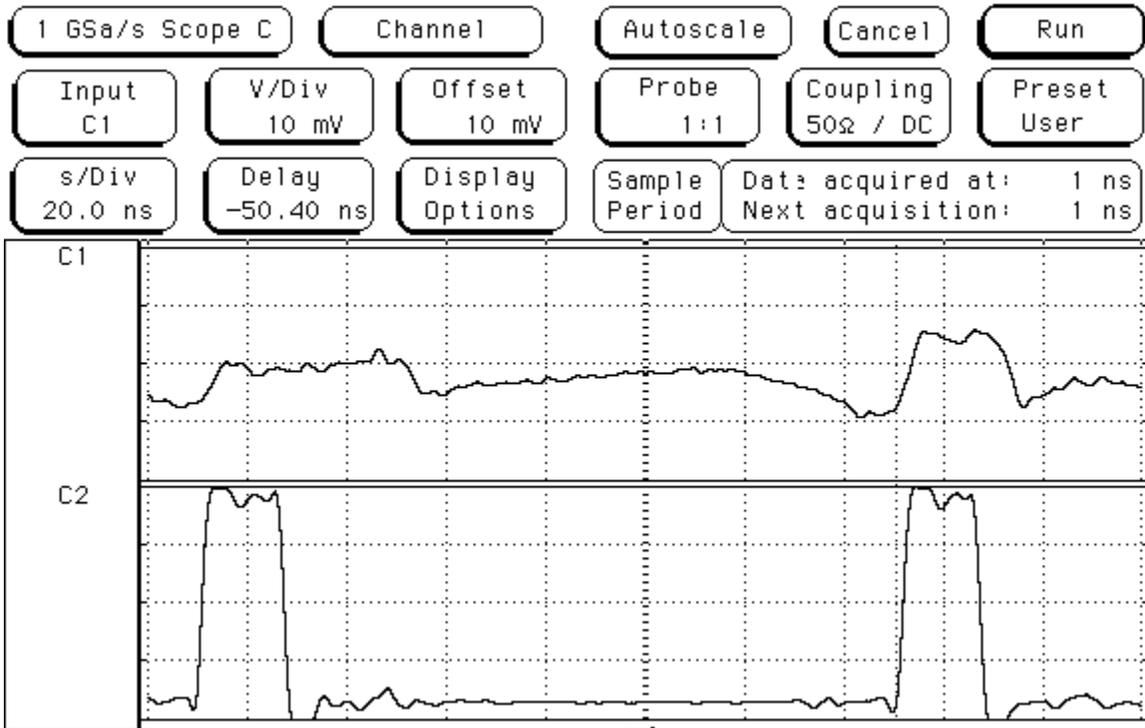
The channel being driven(viewed) was incremented so that the differential pulse shape present on all of the inputs to the receivers could be observed, there was only a minimal amount of pulse shape changes between channels. The 2nd picture is also of channel 0 at the differential input to the receiver, this picture shows the pulse shape when all the channels are being driven with one high going 20ns pulse at the same time. The 3rd and 4th picture are of the output of the channel 0 receiver and correspond to the 1st and 2nd pictures, these pictures depict the width of the data pulse the receiver will produce in the two cases. The horizontal scale per division in these last two pictures are 2v/div.





TEST A6: LVDS - Cable #4 Crosstalk Test

The following picture shows the results of the crosstalk test. The differential probe(C1) was placed across the differential input of the channel 10 receiver and another probe(C2) was placed at the output of the channel 9 receiver. The crosstalk from the adjacent channels can be observed at the differential input(C1) of the non-driven channel's receiver. The horizontal scale per division is 100mv/div for C1 and 1v/div for C2. The output of the channel 10 receiver never went to a high state. The picture below was taken with only channel 9 and channel 11 being driven, we also observed the crosstalk when all 23 channels were being driven and the changes were minimal

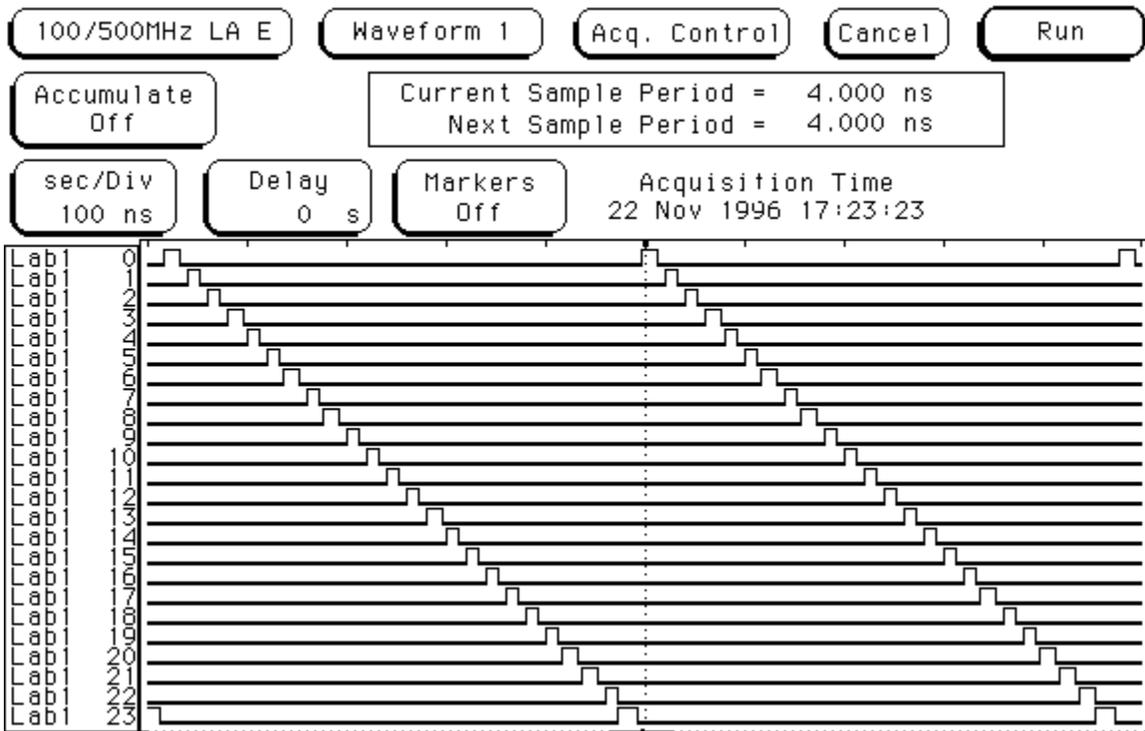


LVDS Logic with ANSLEY cable and 10' Twist-N-Flat cable added at Receiver end.

The same tests were repeated with the LVDS driver/receivers and ANSLEY cable #4 with a 10 ft. length of twist-n-flat cable added to the receiver end of the ANSLEY cable. The changes were minimal, the resulting pictures are shown below.

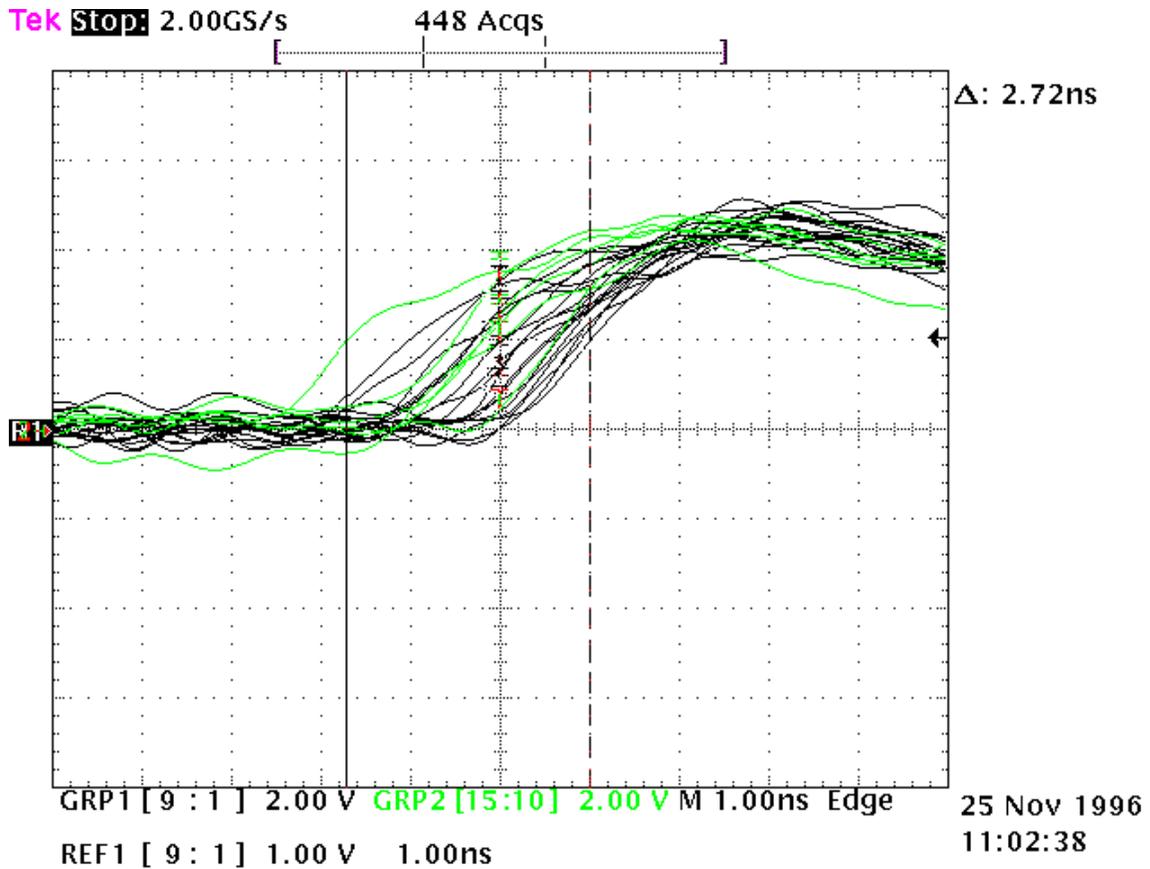
TEST B1: LVDS - Step Test

The following picture shows the output of the LVDS Receiver. The waveform was observed with the Logic Analyzer. The input pulse width was set to 20ns. This resultant waveform verifies the connection and functionality of the drivers, receivers and cable under test.



TEST B2: LVDS - Skew Test

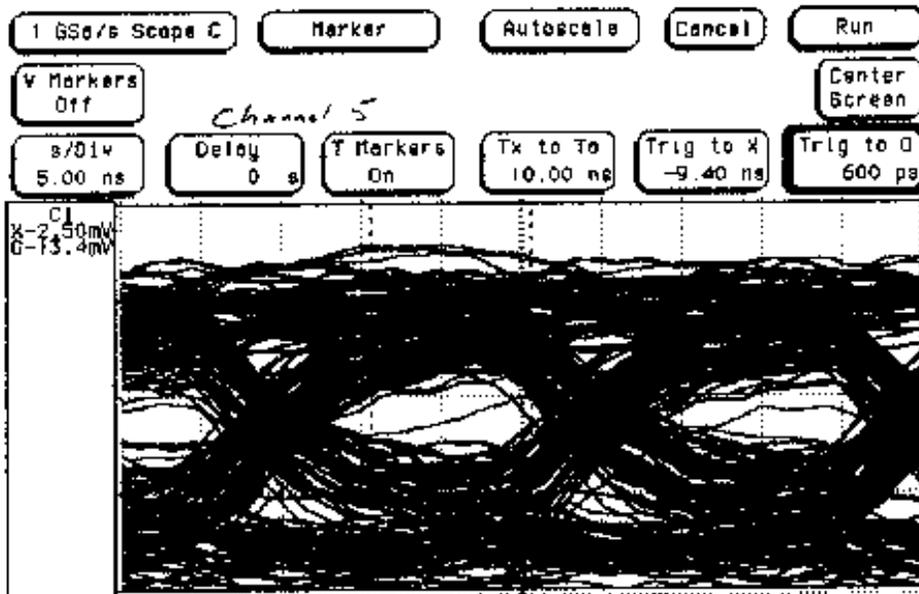
The following picture shows the skew between outputs of the 24 LVDS Receivers, the waveform was observed with Tektronix TLS 216 Logic Scope. The total skew for the system was as shown: 2.72ns and occurred between channel 5 and channel 16. The skew measured between the inputs of the drivers was found to be 1.26ns. The skew measured between the outputs of the receivers and the input to the Logic Scope was found to be 0.1ns. The skew through the cable and drivers was then found by subtracting: $2.72\text{ns} - 1.26\text{ns} - 0.1\text{ns} = 1.36\text{ns}$.



TEST B3: LVDS - EYE Test

The following picture shows the differential inputs of channel 5 as observed with the differential probe. The measured width of the eye opening for all the channels is shown in the following chart.

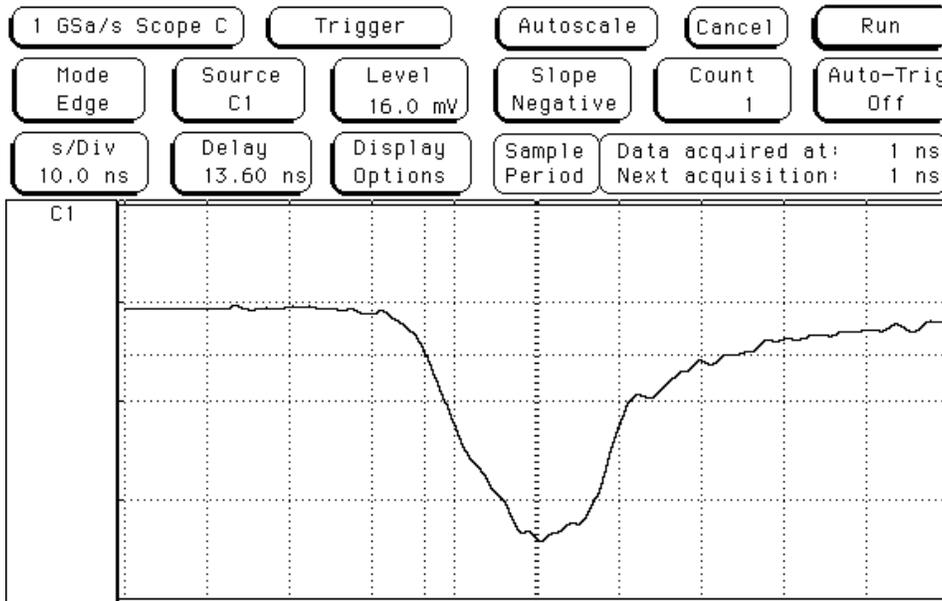
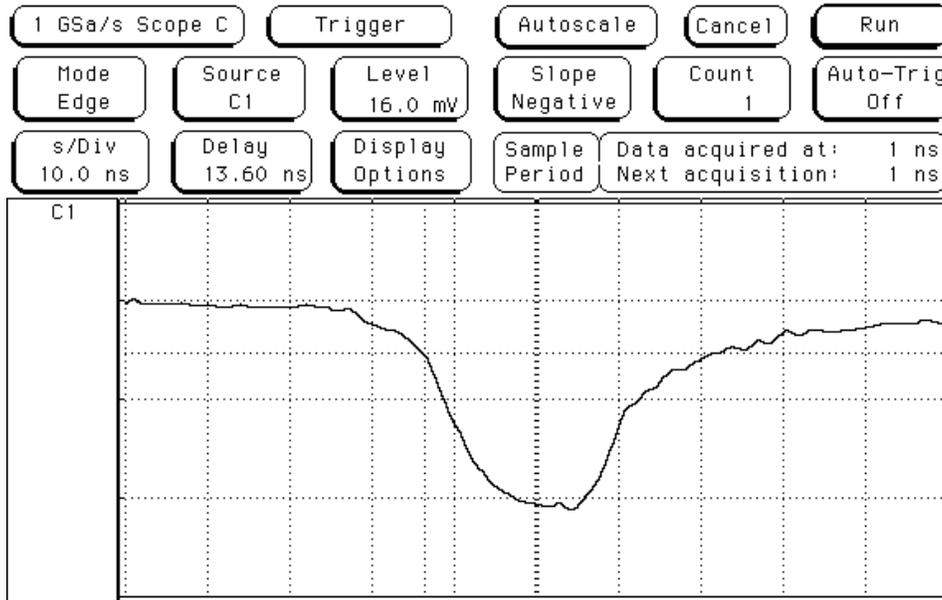
CHANNEL NUMBER	WIDTH OF EYE OPENING
0	12.4ns
1	11.6ns
2	13.2ns
3	11.1ns
4	10.2ns
5	9.9ns *worst
6	12.3ns
7	11.4ns
8	12.2ns
9	11.3ns
10	12.9ns
11	12.3ns
12	14.2ns *best
13	12.3ns
14	12.1ns
15	11.7ns
16	14.1ns
17	12.6ns
18	13.2ns
19	14.1ns
20	11.9ns
21	12.5ns
22	12.1ns
23	14.1ns

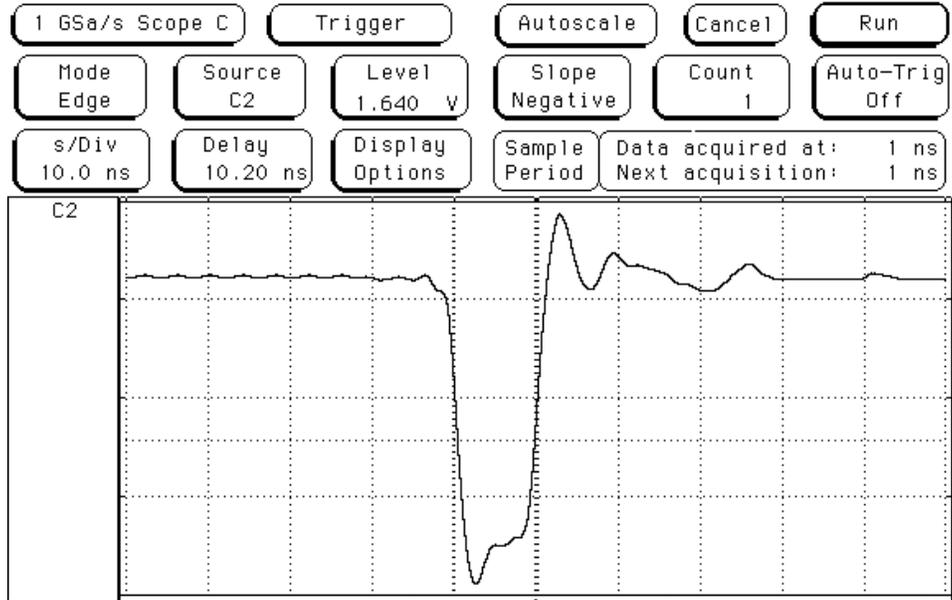
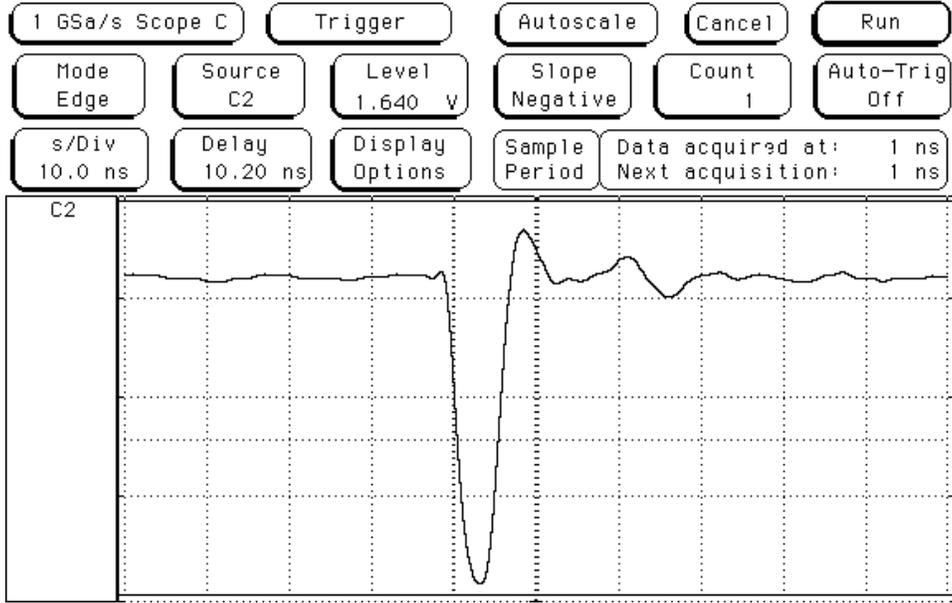


TEST B4: LVDS Steady State - High Test

The 1st picture below shows the differential input of channel 0 receiver as measured with the differential probe. The single low going pulse provided to only the channel 0 driver was 20ns wide. The Horizontal scale per division is 200mv/div.

The channel being driven(viewed) was incremented so that the differential pulse shape present on all of the inputs to the receivers could be observed, there was only a minimal amount of pulse shape changes between channels. The 2nd picture is also of channel 0 at the differential input to the receiver, this picture shows the pulse shape when all the channels are being driven with one low going 20ns pulse at the same time. The 3rd and 4th picture are of the output of the channel 0 receiver and correspond to the 1st and 2nd pictures, these pictures depict the width of the data pulse the receiver will produce in the two cases. The horizontal scale per division in these last two pictures are 2v/div.



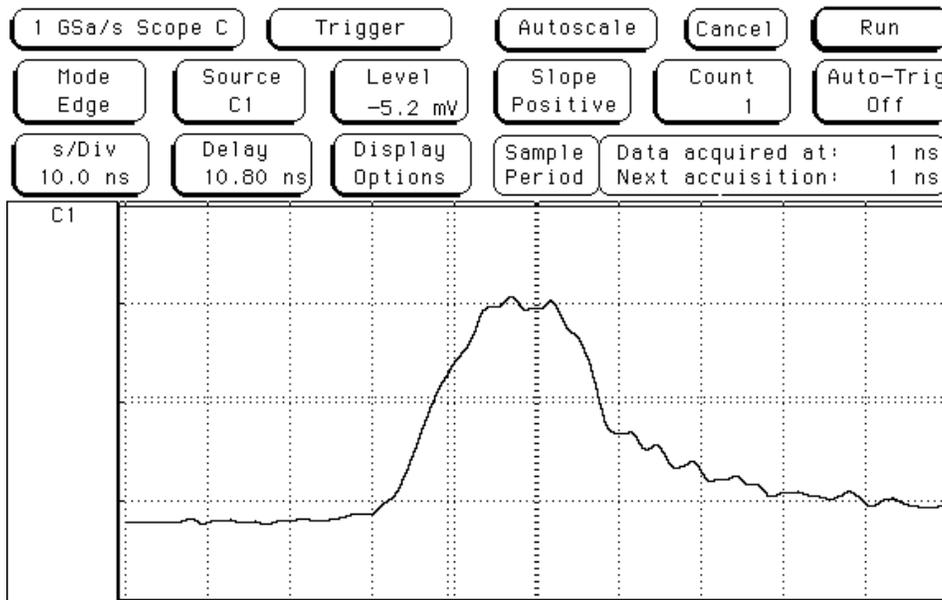
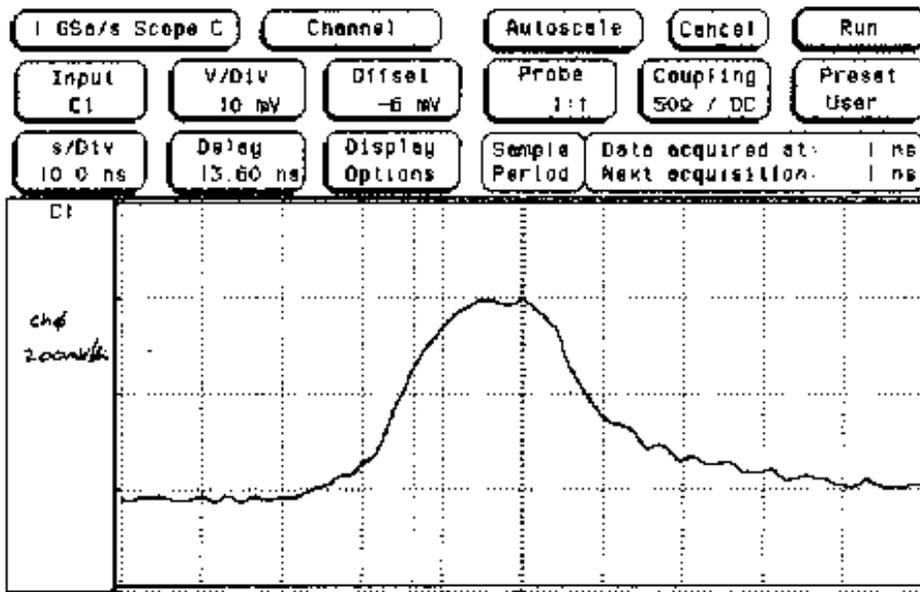


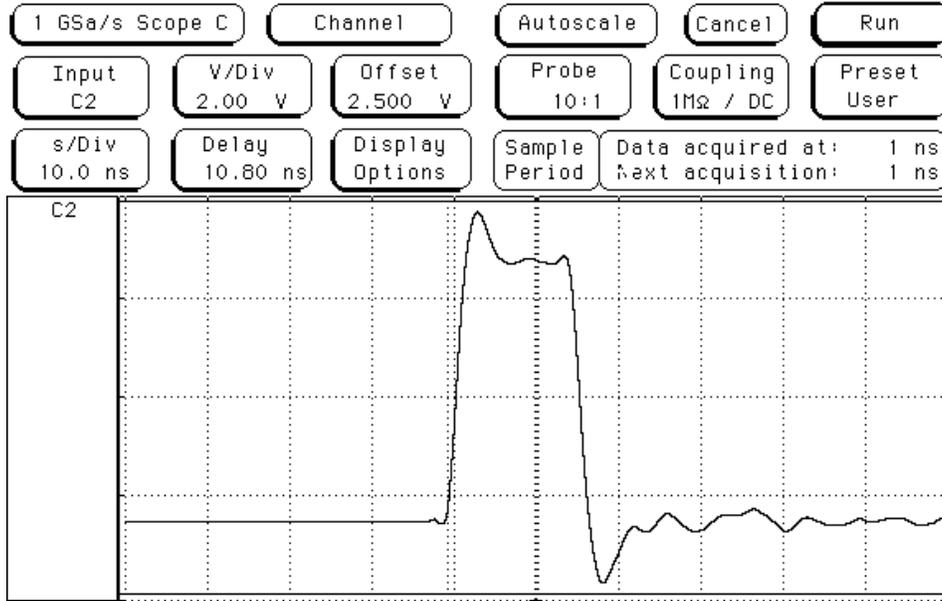
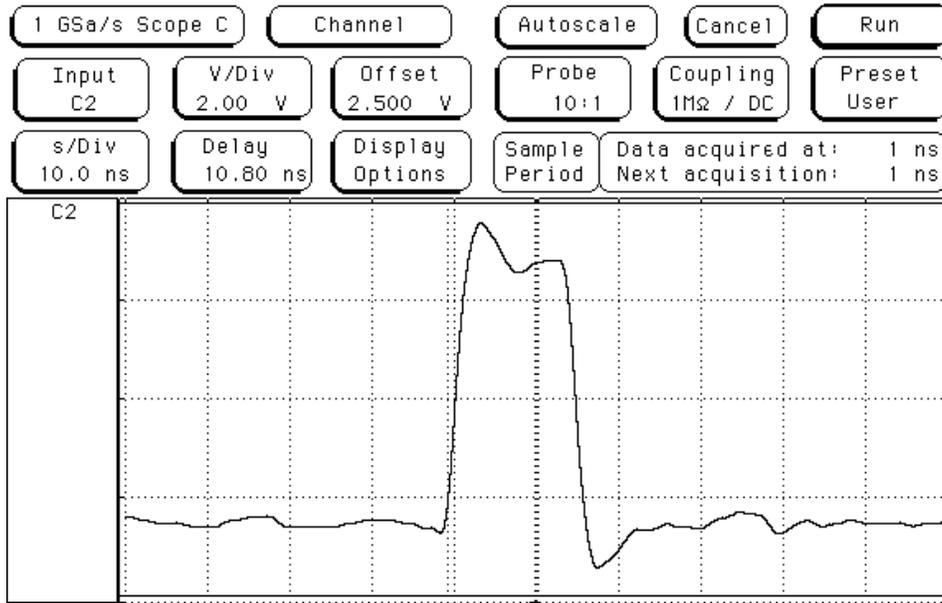
TEST B5: LVDS Steady State - Low Test

The 1st picture below shows the differential input of channel 0 receiver as measured with the differential probe. The single high going pulse provided to only the channel 0 driver was 20ns wide. The Horizontal scale per division is 200mv/div.

The channel being driven(viewed) was incremented so that the differential pulse shape present on all of the inputs to the receivers could be observed, there was only a minimal amount of pulse shape changes between channels. The 2nd picture is also of channel 0 at the differential input to the receiver, this picture shows the pulse shape when all the channels are being driven with one high going 20ns pulse at the same time. The 3rd and 4th picture are of the output of the channel 0 receiver and correspond to the 1st and 2nd pictures, these pictures depict the width of the data pulse the receiver will produce in the two cases. The horizontal scale per division in these last two pictures are 2v/div.

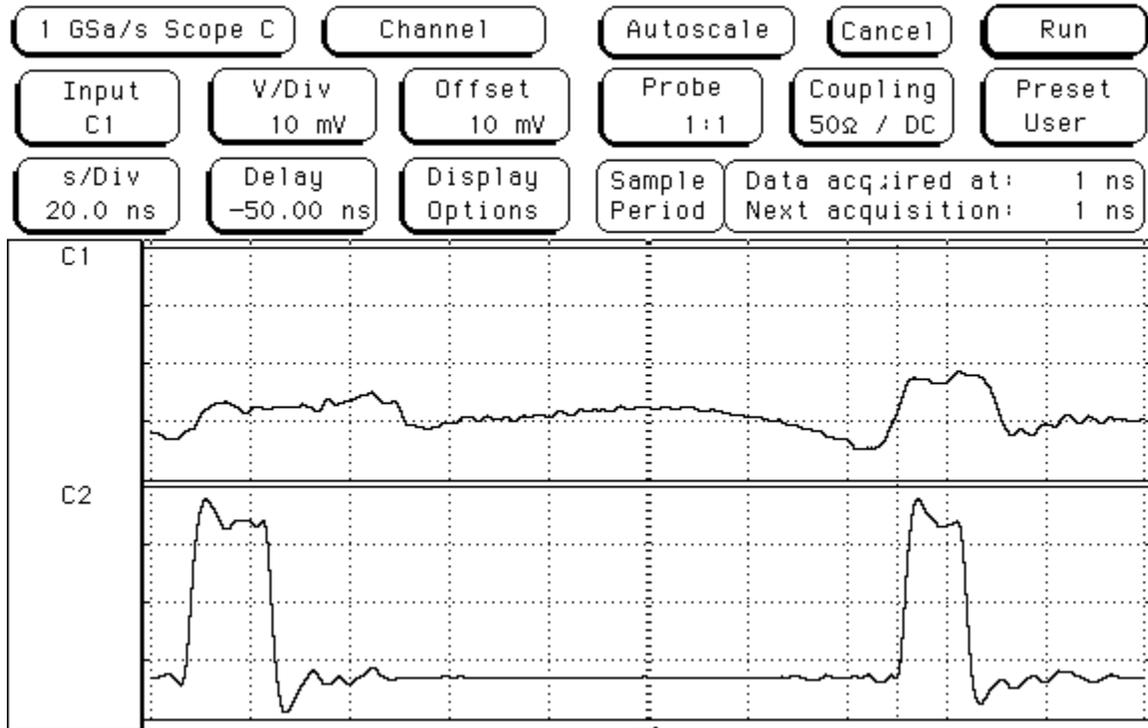
LV85C9





TEST B6: LVDS Crosstalk Test

The following picture shows the results of the crosstalk test. The differential probe(C1) was placed across the differential input of the channel 10 receiver and another probe(C2) was placed at the output of the channel 9 receiver. The crosstalk from the adjacent channels can be observed at the differential input(C1) of the non-driven channel's receiver. The horizontal scale per division is 100mv/div for C1 and 1v/div for C2. The output of the channel 10 receiver never went to a high state. The picture below was taken with only channel 9 and channel 11 being driven, we also observed the crosstalk when all 23 channels were being driven and the changes were minimal



Changed termination resistors on Receiver board at LVDS inputs from 100 ohms to 121 ohms and repeated the Skew and Eye tests. The Skew test produced a maximum skew of 1.14ns for both the ANSLEY only cable and for the ANSLEY and 10' Twist-N-Flat cable. The EYE tests were similar to the EYE tests with the 100 ohm resistors with opening varying from 10ns to 14ns. The other three 200' ANSLEY cables were given tests A2 & B2 "LVDS SKEW TEST" and A3 & B3 "LVDS EYE TEST".

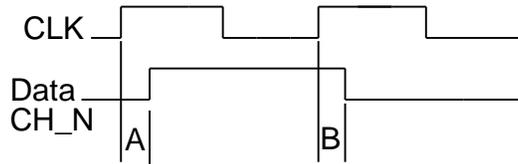
The results of the skew tests are as follows:

ANSLEY #1	ANSLEY #2	ANSLEY #3	ANSLEY #4
1.15ns	1.35ns	1.17ns	1.21ns
ANSLEY #1 w/10' twist-n-flat	ANSLEY #2 w/10' twist-n-flat	ANSLEY #3 w/10' twist-n-flat	ANSLEY #4 w/10' twist-n-flat
1.15ns	1.37ns	1.17ns	1.45ns

The EYE tests of all 4 cables with or without the 10' twist-n-flat attached showed a minimum opening of 10.2ns.

CHANNEL LINK TEST RESULTS

The following chart shows the affect of the clock delay setting of the Pattern Generator on the clock to data relationship at the drivers inputs. For the A measurement if the positive edge of the clock is ahead of the positive edge of the data then the number is negative. For the B measurement if the positive edge of the clock is after the falling edge of the data the number is negative. As can be seen in the results that for a clock delay of 0 the second clock pulse will clock in the data.



Clk Delay #	25M Hz. Clk A	25M Hz. Clk B	30M Hz. Clk A	30M Hz. Clk B	40M Hz. Clk A	40M Hz. Clk B
0	-3.0ns	2.4ns	-2.4ns	2.0ns	-2.5ns	1.8ns
1	-2.2ns	0.9ns	-0.9ns	0.3ns	-1.8ns	0
2	0	-1.6ns	1.3ns	-1.8ns	-1.5ns	-1.0ns
3	2.5ns	-2.2ns	2.2ns	-2.5ns	0	-1.8ns
4	3.4ns	-3.3ns	3.9ns	-3.7ns	2.5ns	-2.8ns
5	4.7ns	-4.4ns	5.7ns	-4.9ns	4.4ns	-4.4ns
6	5.9ns	-6.4ns	6.9ns	-6.9ns	5.5ns	-6.1ns
7	6.6ns	-7.6ns	7.6ns	-8.4ns	6.8ns	-7.6ns
8	8.4ns	-9.6ns	8.8ns	-9.9ns	7.5ns	-8.9ns
9	9.6ns	-10.6ns	9.7ns	-10.1ns	9.2ns	-10.3ns

TEST C1: CHANNEL LINK - Twist-n-Flat Cable Test

At a 140" cable length and the 25M Hz. data rate the data was valid at clock delays of 0 and 6-9, at clock delays of 1-5 the data was corrupted.

At a 120" cable length and the 30M Hz. data rate the data was valid at clock delays of 0 and 6-9, at clock delays of 1-5 the data was corrupted.

At a 80" cable length and the 40M Hz. data rate the data was valid at clock delays of 0 and 6-9, at clock delays of 1-5 the data was corrupted.

TEST C2: CHANNEL LINK - Category 5 Cable Test

At a 25' cable length and the 25M Hz. data rate the data was valid at clock delays of 0 and 6-9, at clock delays of 1-5 the data was corrupted.

At a 20' cable length and the 30M Hz. data rate the data was valid at clock delays of 0 and 6-9, at clock delays of 1-5 the data was corrupted.

At a 10' cable length and the 40M Hz. data rate the data was valid at clock delays of 0 and 6-9, at clock delays of 1-5 the data was corrupted.

MAXIMUM CABLE LENGTH VS. FREQUENCY

Twist-N-Flat			Category 5		
25M Hz.	30M Hz.	40M Hz.	25M Hz.	30M Hz.	40M Hz.
140"	120"	80"	25'	20'	10'

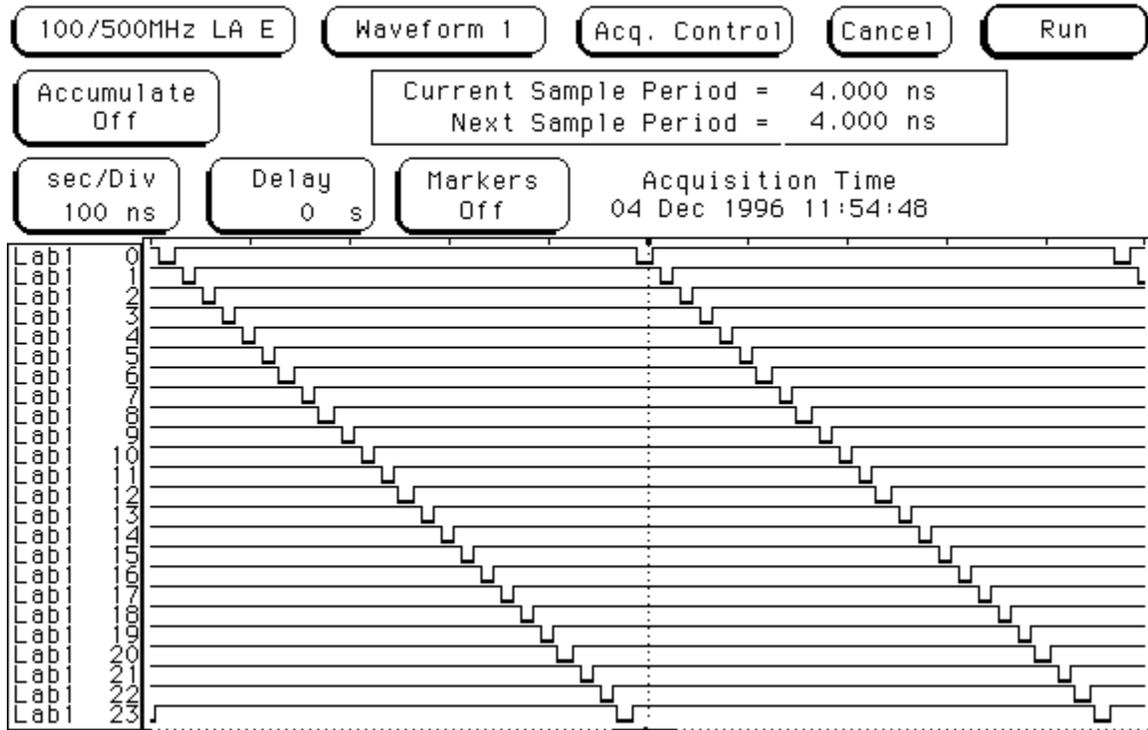
The maximum length of the cable may be some what longer in the Category 5 cable because we reduced the cable in 5' increments. At 30M Hz. and a 25' length there were only a few errors and at 40M Hz. and a 15' length there were only a few errors.

ECL Logic ANSLEY CABLE TEST RESULTS

The receiver outputs of the ECL logic are reversed resulting in inverted outputs at the receiver end.

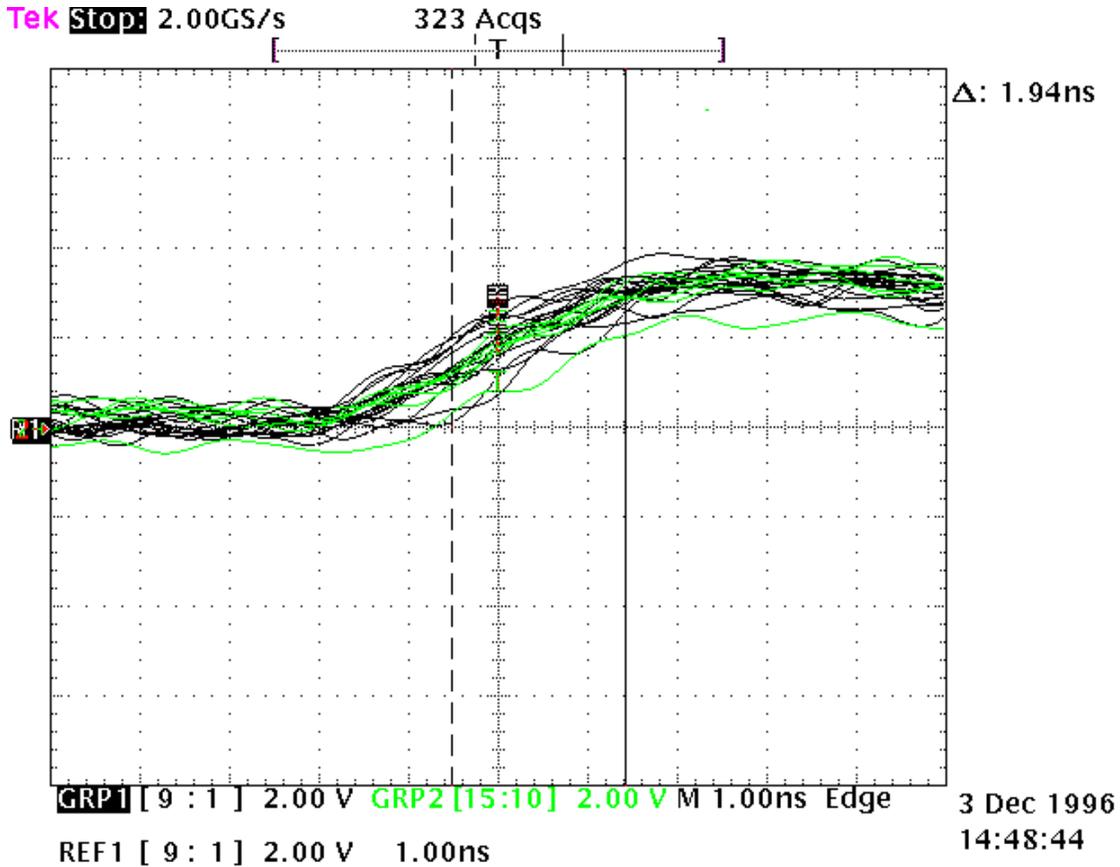
TEST A1: ECL - Cable #4 Step Test

The following picture shows the output of the LVDS Receiver, the waveform was observed with the Logic Analyzer. The input pulse width was set to 20ns. This resultant waveform verifies the connection and functionality of the drivers, receivers and cable under test.



TEST A2: ECL - Cable #4 Skew Test

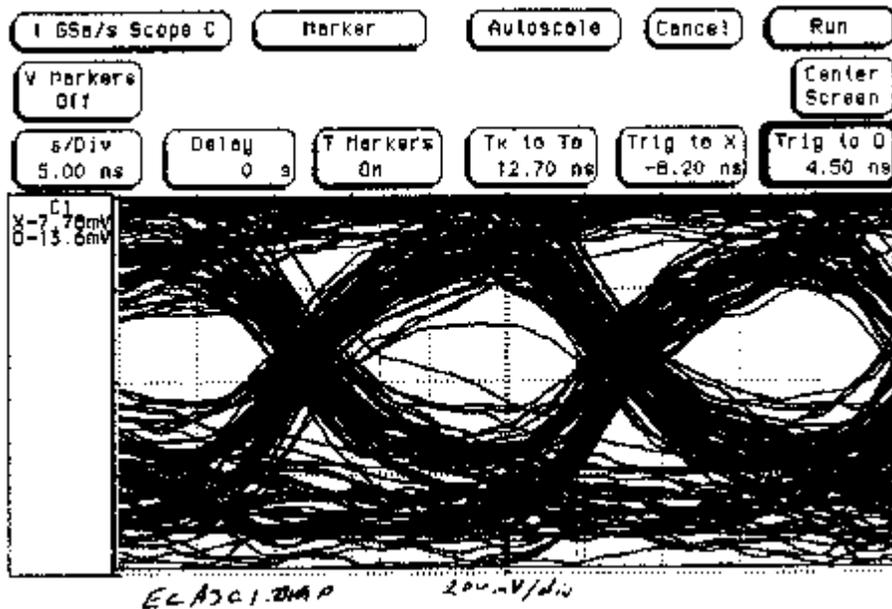
The following picture shows the skew between outputs of the 24 LVDS Receivers, the waveform was observed with Tektronix TLS 216 Logic Scope. The total skew for the system was as shown: 2.48ns and occurred between channel 5 and channel 16. The skew measured between the inputs of the drivers was found to be 1.26ns. The skew measured between the outputs of the receivers and the input to the Logic Scope was found to be 0.1ns. The skew through the cable and drivers was then found by subtracting: $2.48\text{ns} - 1.26\text{ns} - 0.1\text{ns} = 1.12\text{ns}$.

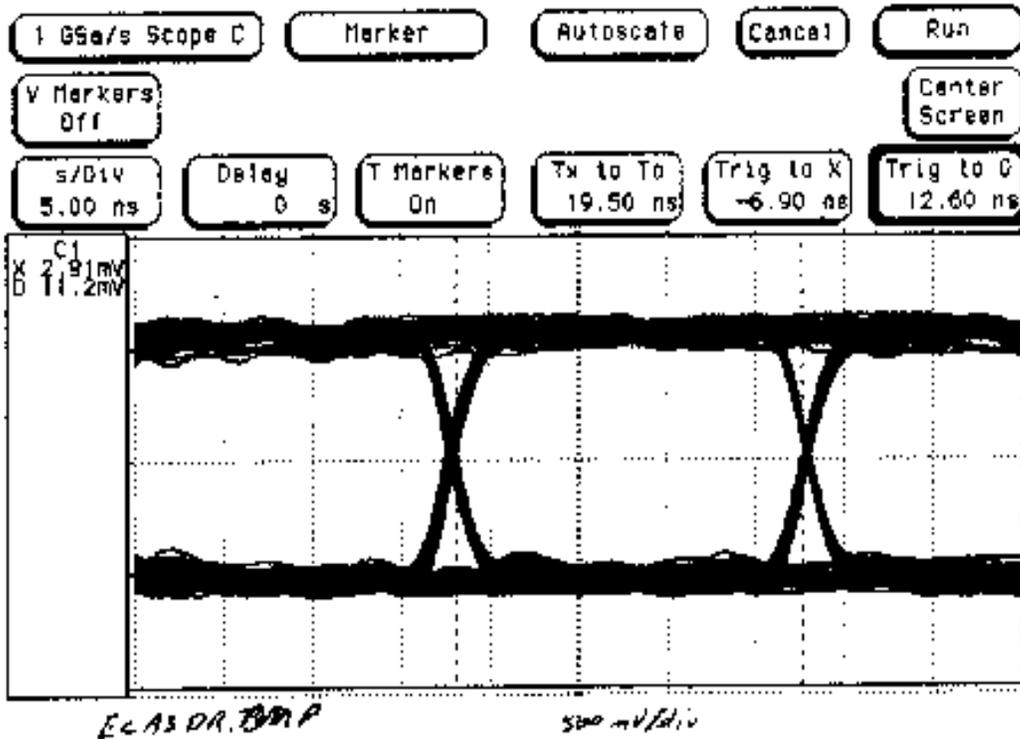
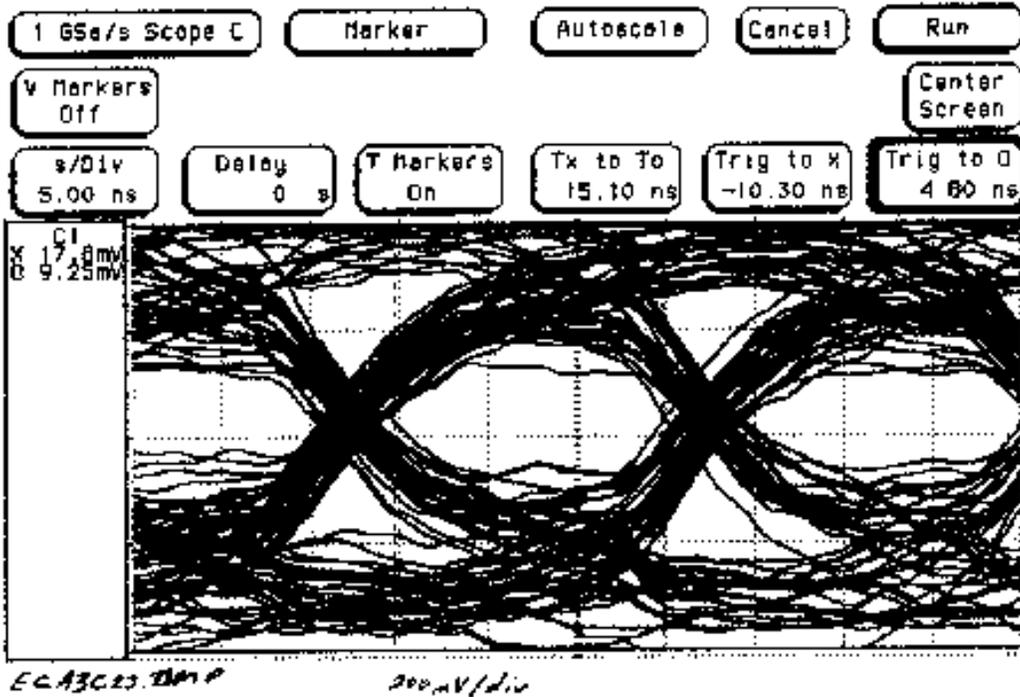


TEST A3: ECL - Cable #4 I-Test

The following three pictures shows the differential inputs of channel 1 and 23 and channel 0's drivers output as observed with the differential probe. The measured width of the eye opening for all the channels is shown in the following chart.

CHANNEL NUMBER	WIDTH OF EYE OPENING
0	14.8ns
1	12.7ns
2	13.7ns
3	14.5ns
4	13.7ns
5	13.5ns
6	14.4ns
7	14.1ns
8	14.1ns
9	13.1ns
10	13.3ns
11	13.8ns
12	14.0ns
13	13.8ns
14	13.0ns
15	13.1ns
16	13.0ns
17	12.7ns
18	13.8ns
19	14.4ns
20	12.6ns
21	13.5ns
22	13.3ns
23	15.1ns

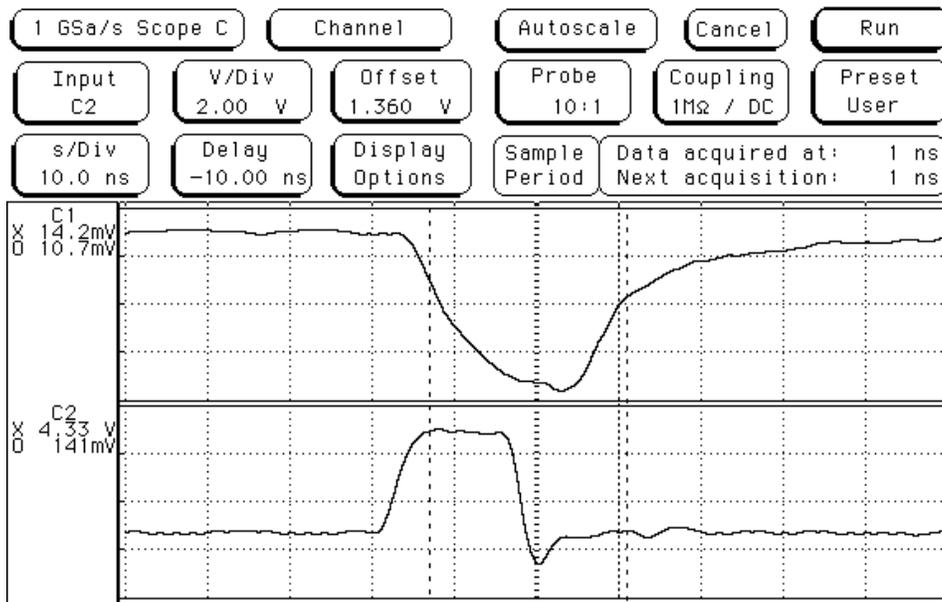
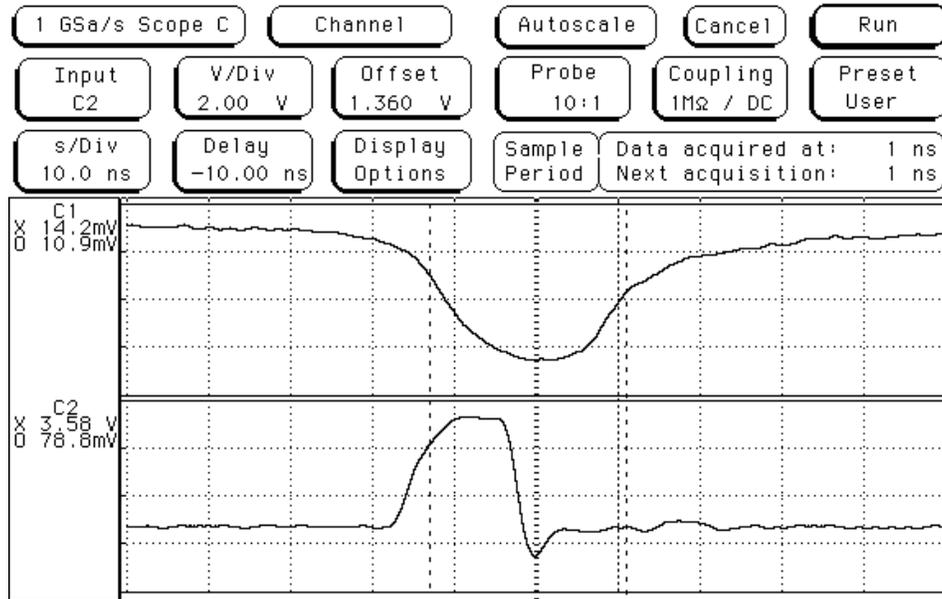




TEST A4: ECL - Cable #4 Steady State - High Test

The 1st picture below shows the differential input of channel 0 receiver as measured with the differential probe and the output of the receiver. The single low going pulse provided to only the channel 0 driver was 20ns wide. The Horizontal scale per division is 200mv/div for the top trace and 1v/div for the bottom trace.

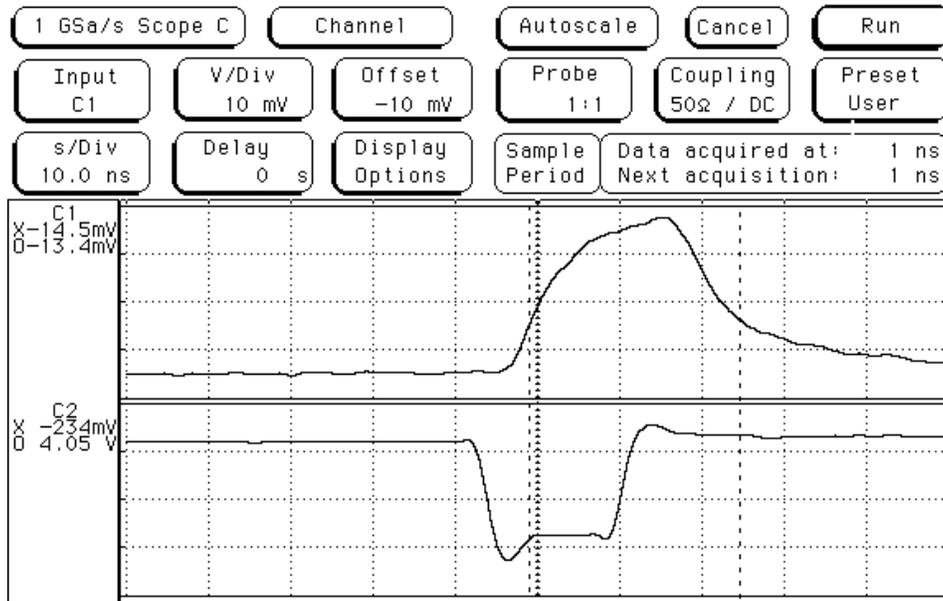
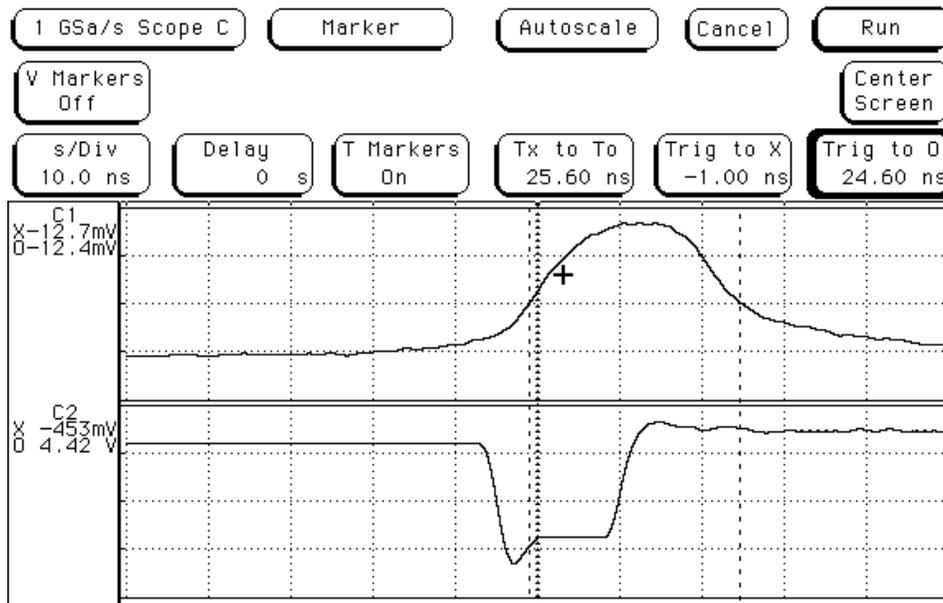
The channel being driven(viewed) was incremented so that the differential pulse shape present on all of the inputs to the receivers could be observed, there was only a minimal amount of pulse shape changes between channels. The 2nd picture is also of channel 0 at the differential input to the receiver, this picture shows the pulse shape when all the channels are being driven with one low going 20ns pulse at the same time.



TEST A5: ECL - Cable #4 Steady State - Low Test

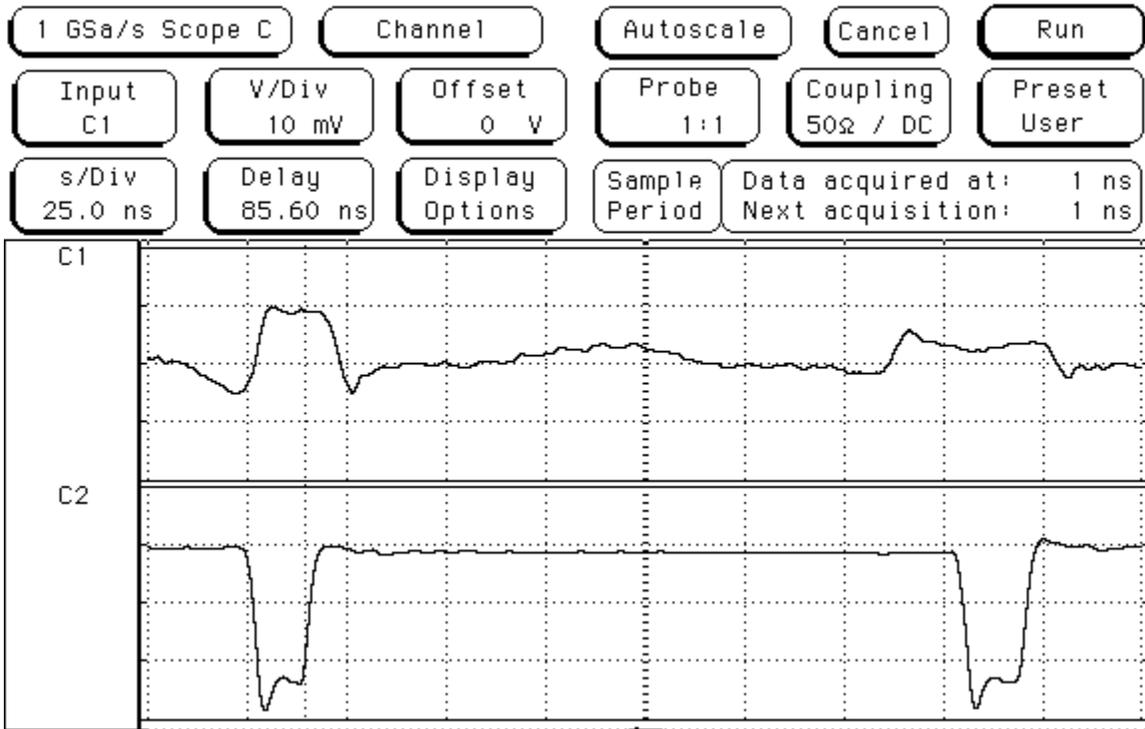
The 1st picture below shows the differential input of channel 0 receiver as measured with the differential probe and the output of the receiver. The single high going pulse provided to only the channel 0 driver was 20ns wide. The Horizontal scale per division is 200mv/div for the top trace and 1v/div for the bottom trace.

The channel being driven(viewed) was incremented so that the differential pulse shape present on all of the inputs to the receivers could be observed, there was only a minimal amount of pulse shape changes between channels. The 2nd picture is also of channel 0 at the differential input to the receiver, this picture shows the pulse shape when all the channels are being driven with one high going 20ns pulse at the same time.



TEST A6: ECL - Cable #4 Crosstalk Test

The following picture shows the results of the crosstalk test. The differential probe(C1) was placed across the differential input of the channel 10 receiver and another probe(C2) was placed at the output of the channel 9 receiver. The crosstalk from the adjacent channels can be observed at the differential input(C1) of the non-driven channel's receiver. The horizontal scale per division is 100mv/div for C1 and 1v/div for C2. The output of the channel 10 receiver never went to a high state. The picture below was taken with only channel 9 and channel 11 being driven, we also observed the crosstalk when all 23 channels were being driven and the changes were minimal

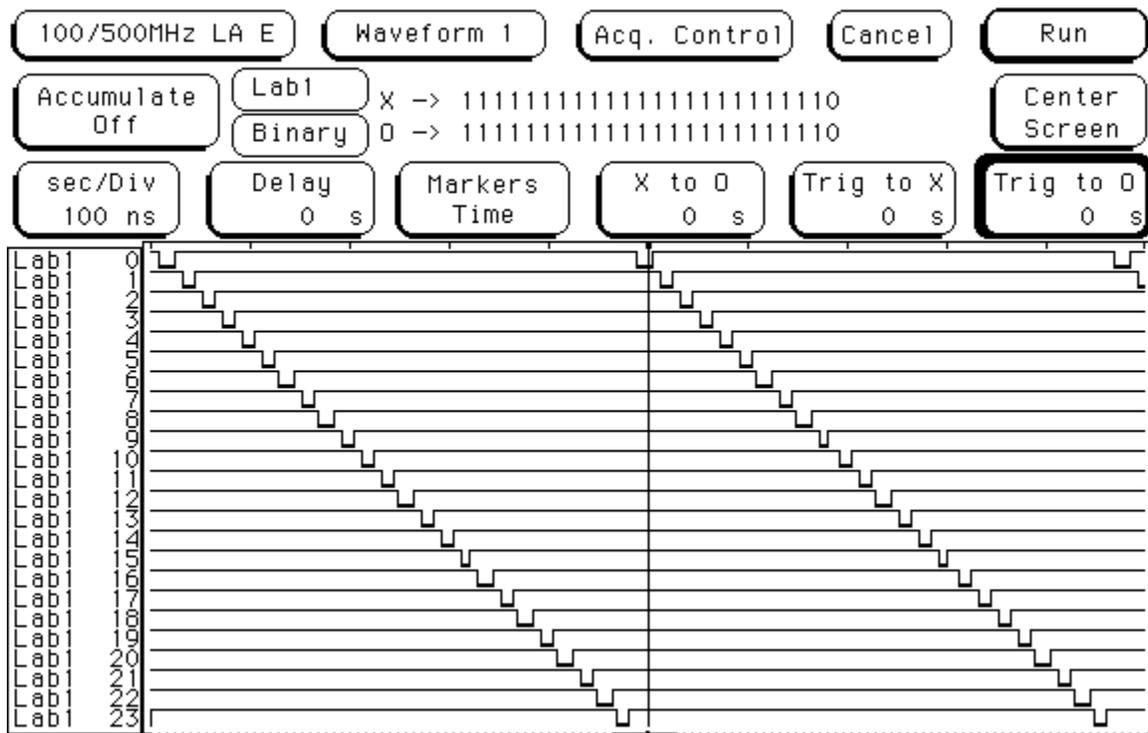


ECL Logic with ANSLEY cable and 10' Twist-N-Flat cable added at Receiver end.

The same tests were repeated with the ECL driver/receivers and ANSLEY cable #4 with a 10 ft. length of twist-n-flat cable added to the receiver end of the ANSLEY cable. The changes were minimal, the resulting pictures are shown below.

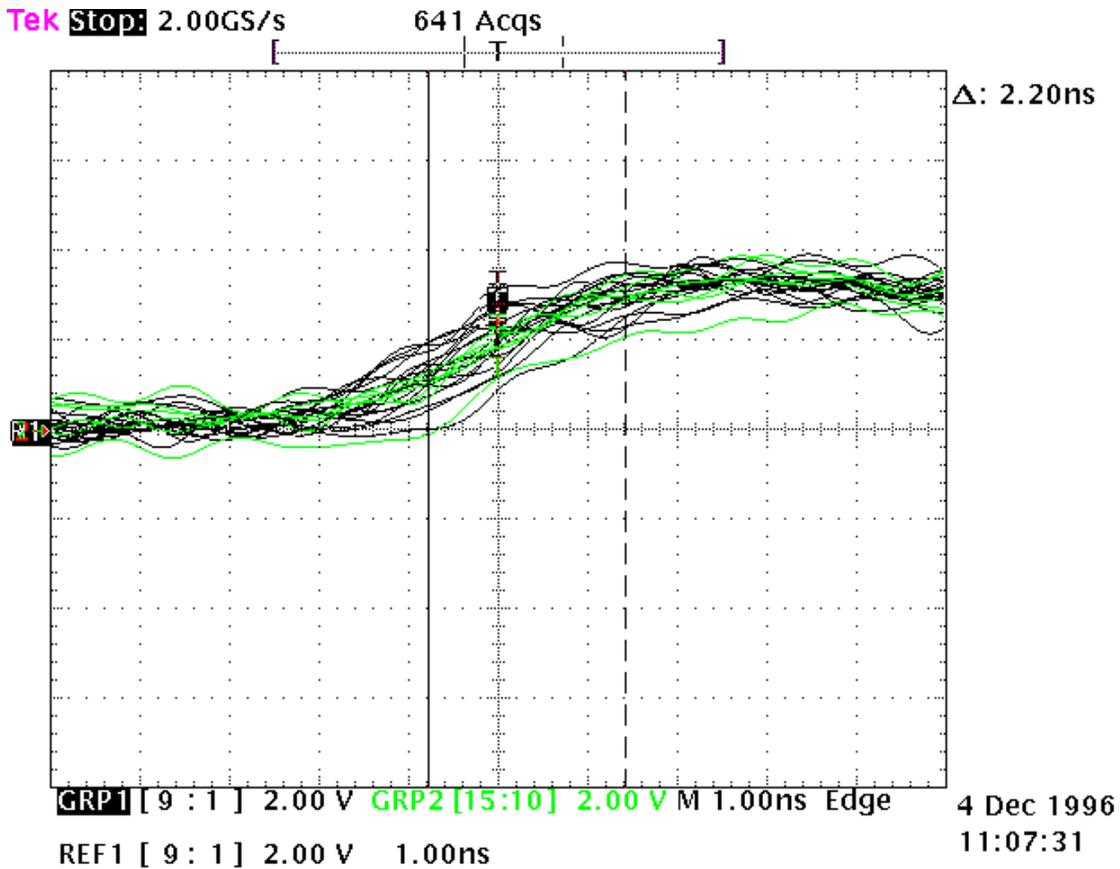
TEST B1: ECL - Step Test

The following picture shows the output of the ECL Receiver. The waveform was observed with the Logic Analyzer. The input pulse width was set to 20ns. This resultant waveform verifies the connection and functionality of the drivers, receivers and cable under test.



TEST B2: ECL - Skew Test

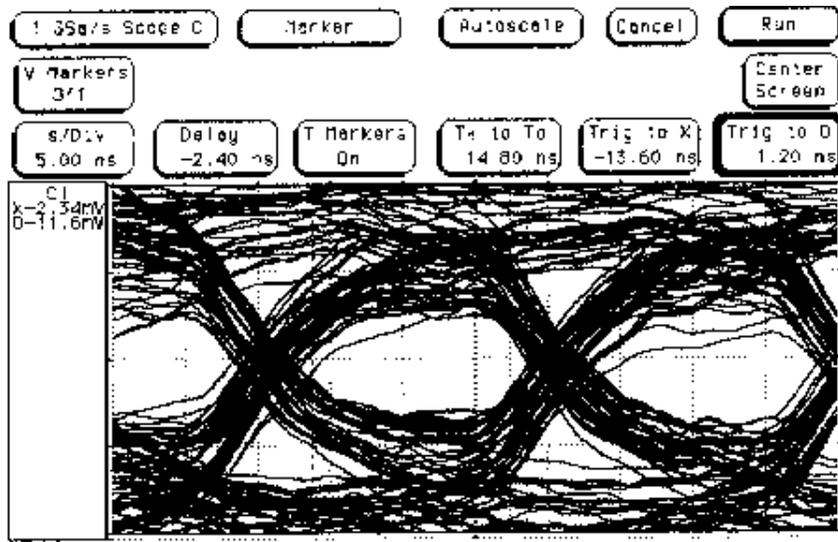
The following picture shows the skew between outputs of the 24 ECL Receivers, the waveform was observed with Tektronix TLS 216 Logic Scope. The total skew for the system was as shown: 2.72ns and occurred between channel 5 and channel 16. The skew measured between the inputs of the drivers was found to be 1.26ns. The skew measured between the outputs of the receivers and the input to the Logic Scope was found to be 0.1ns. The skew through the cable and drivers was then found by subtracting: $2.72\text{ns} - 1.26\text{ns} - 0.1\text{ns} = 1.36\text{ns}$.



TEST B3: ECL - EYE Test

The following picture shows the differential inputs of channel 0 as observed with the differential probe. The measured width of the eye opening for all the channels is shown in the following chart.

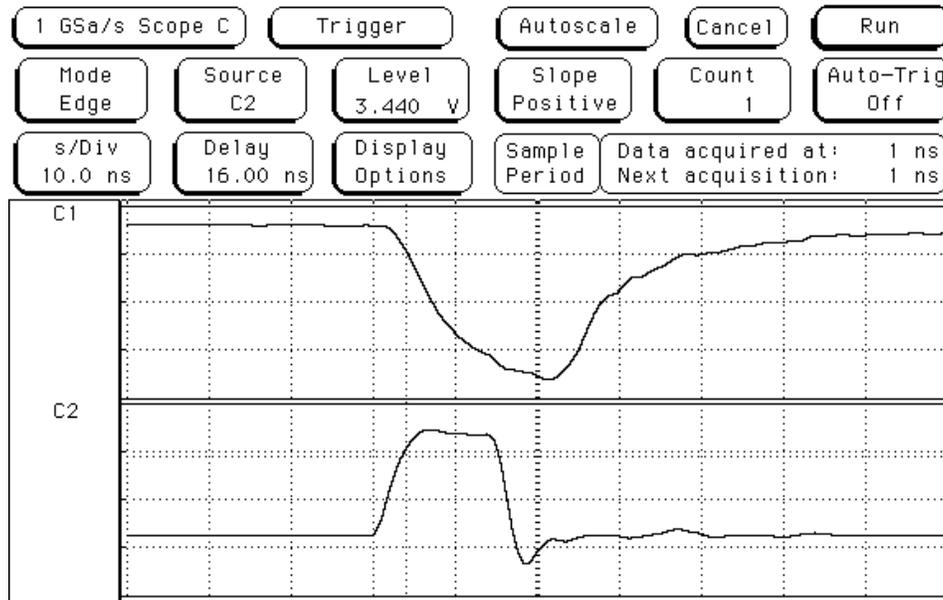
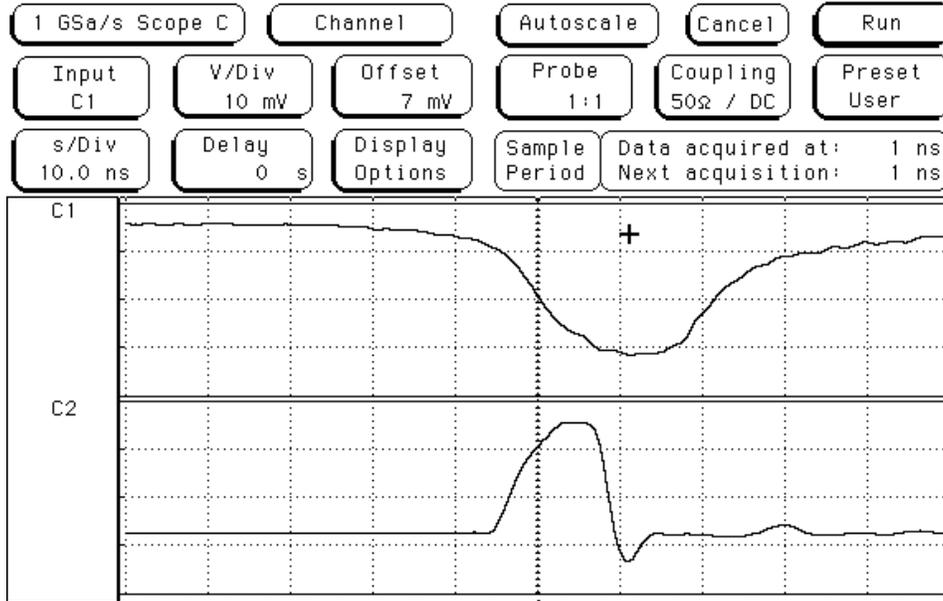
CHANNEL NUMBER	WIDTH OF EYE OPENING
0	14.8ns
1	11.9ns
2	13.5ns
3	14.1ns
4	13.4ns
5	12.4ns
6	14.5ns
7	14.7ns
8	14.0ns
9	12.8ns
10	13.2ns
11	12.2ns
12	14.0ns
13	14.3ns
14	13.7ns
15	13.9ns
16	12.2ns
17	12.7ns
18	14.2ns
19	13.6ns
20	13.7ns
21	14.1ns
22	13.8ns
23	14.7ns



TEST B4: ECL Steady State - High Test

The 1st picture below shows the differential input of channel 0 receiver as measured with the differential probe and the output of the receiver. The single low going pulse provided to only the channel 0 driver was 20ns wide. The Horizontal scale per division is 200mv/div for the top trace and 1v/div for the bottom trace.

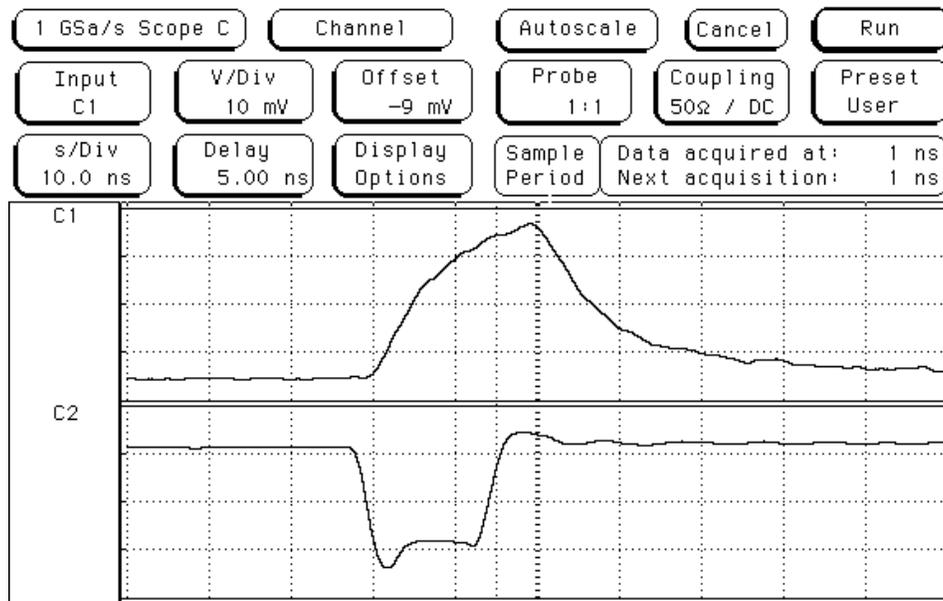
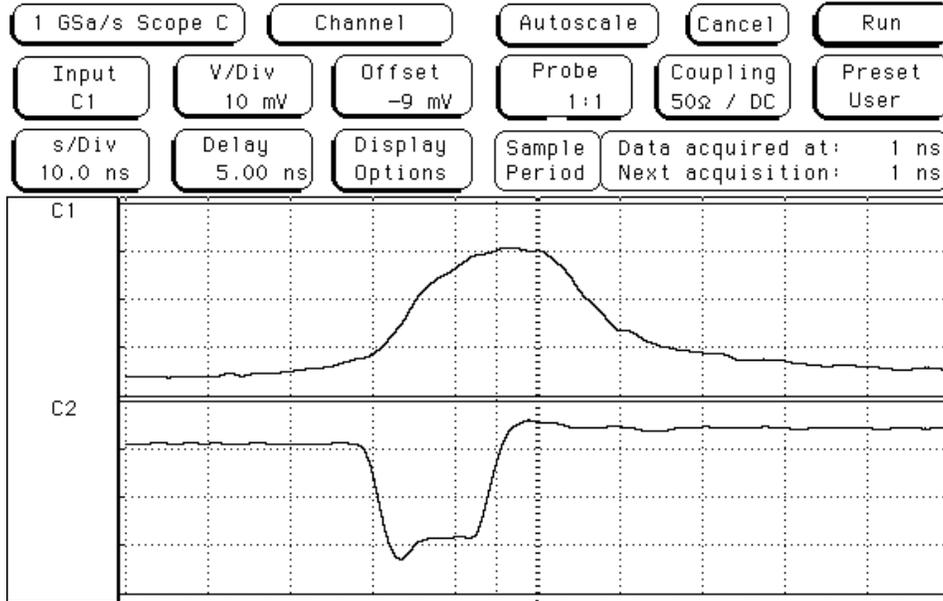
The channel being driven(viewed) was incremented so that the differential pulse shape present on all of the inputs to the receivers could be observed, there was only a minimal amount of pulse shape changes between channels. The 2nd picture is also of channel 0 at the differential input to the receiver, this picture shows the pulse shape when all the channels are being driven with one low going 20ns pulse at the same time.



TEST B5: ECL Steady State - Low Test

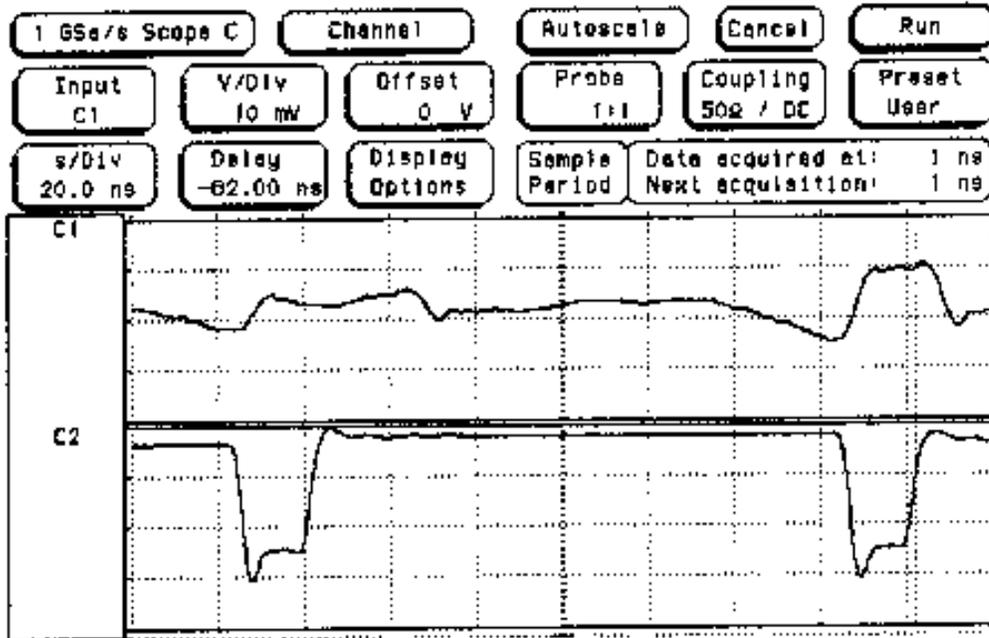
The 1st picture below shows the differential input of channel 0 receiver as measured with the differential probe and the output of the receiver. The single high going pulse provided to only the channel 0 driver was 20ns wide. The Horizontal scale per division is 200mv/div for the top trace and 1v/div for the bottom trace.

The channel being driven(viewed) was incremented so that the differential pulse shape present on all of the inputs to the receivers could be observed, there was only a minimal amount of pulse shape changes between channels. The 2nd picture is also of channel 0 at the differential input to the receiver, this picture shows the pulse shape when all the channels are being driven with one high going 20ns pulse at the same time.



TEST B6: ECL Crosstalk Test

The following picture shows the results of the crosstalk test. The differential probe(C1) was placed across the differential input of the channel 10 receiver and another probe(C2) was placed at the output of the channel 9 receiver. The crosstalk from the adjacent channels can be observed at the differential input(C1) of the non-driven channel's receiver. The horizontal scale per division is 100mv/div for C1 and 1v/div for C2. The output of the channel 10 receiver never went to a high state. The picture below was taken with only channel 9 and channel 11 being driven, we also observed the crosstalk when all 23 channels were being driven and the changes were minimal



ECL B6 C4.TIF