



**Fermilab**

Particle Physics Division/CDF Upgrade Project

**DRAFT**

**Specification for the  
Ansley Driver Module\_V2**

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## **1.0 Introduction**

A need exists in the XFT project to drive a large number of Ansley Cables in order to test the Finder Modules. To test a single SL1/3 Finder Module, we are required to drive 14 cables. To test a single SL2/4 Finder Module, 12 cables must be driven.

Currently we are using a pattern generator to test the input section of the Finder modules. This has two major disadvantages. The first, only a single cable can be driven at a time. The second, it is difficult to run the data up the cable at the 22ns rate we need (20ns is the natural data step).

Therefore, a board has been designed which will have the ability to drive 6 Ansley cables from front panel connections, and an additional two cables via a J3 backplane port to the TDC Transition module.

## **2.0 The Ansley Driver Module**

The Ansley Driver Module makes use of 128K deep static RAM. This RAM can be downloaded over VMEbus. The contents of the RAM can then be sent in a looping fashion to the XFT Finder Modules.



### **3.0 VMEbus Slave Interface**

The FINDER will implement a modified version of a VMEbus slave interface. Only 32 bit aligned data transfers will be supported; these may be either single word transfers or block transfers. Only extended (32-bit) addressing modes will be supported. All modules will be assigned a unique geographical address through use of backplane pins on VME64extension backplane. FINDER modules will respond to the following address modifier codes: 09, and 0B.

## Memory Map

YY00 0000 Diagnostic Register (32 bits) (R/W)

YY00 0004 Control (R/W)

<b><u>Bit</u></b>	<b><u>Function</u></b>
31	Software Reset (R/W)
30	Wait for Halt-Recover-Run-B0 (R/W) <b>(If bit “30” is set, the board will wait for a Halt-Recover-Run sequence followed by a B0 before starting to pump data. Otherwise the pump will start immediately)</b>
29	Enable VME access to RAM (R/W)
28	Enable RAM Data to Ansley Cables (R/W) Turns on Looping Mode
27	Undefined (R/W)
26	Undefined (R/W)
25	Undefined (R/W)
24	Undefined (R/W)
<b>23</b>	<b>Pump is Enabled (Read only)</b> <b>(when this bit is set to 1, the data is being pumped up the ANSLEY Cable ports)</b>
(23:0)	Undefined (R/W)

(The below word counts represent the number of RAM locations **minus 3** that the Sequencer will loop over as the RAM is sent up the cable. Example: To send a repeating pattern of six words, the user would load a three into the Word Count register.)

YY00 0008 Cable A Word Count (R/W)  
**Bit** **Function**  
(16:0) Active word count

YY00 000C Cable B Word Count (R/W)  
**Bit** **Function**  
(16:0) Active word count

YY00 0010 Cable C Word Count (R/W)  
**Bit** **Function**  
(16:0) Active word count

YY00 0014 Cable D Word Count (R/W)  
**Bit** **Function**  
(16:0) Active word count

YY00 0018 Cable E Word Count (R/W)  
**Bit** **Function**  
(16:0) Active word count

YY00 001C Cable F Word Count (R/W)  
**Bit** **Function**  
(16:0) Active word count

YY00 0020 Cable G Word Count (R/W)  
**Bit** **Function**  
(16:0) Active word count

YY00 0024 Cable H Word Count (R/W)  
**Bit** **Function**  
(16:0) Active word count

YY10 0000 - YY10 007F	ID PROM (upper 8 bits)
YY20 0000 - YY27 FFFC	Cable A RAM Bank (23:0) <b>R/W</b>
YY30 0000 - YY37 FFFC	Cable B RAM Bank (23:0) <b>R/W</b>
YY40 0000 - YY47 FFFC	Cable C RAM Bank (23:0) <b>R/W</b>
YY50 0000 - YY57 FFFC	Cable D RAM Bank (23:0) <b>R/W</b>
YY60 0000 - YY67 FFFC	Cable E RAM Bank (23:0) <b>R/W</b>
YY70 0000 - YY77 FFFC	Cable F RAM Bank (23:0) <b>R/W</b>
YY80 0000 - YY87 FFFC	Cable G RAM Bank (23:0) <b>R/W</b>
YY90 0000 - YY97 FFFC	Cable H RAM Bank (23:0) <b>R/W</b>

**For Cables A through H, the data represents the following signals for the Finder Boards:**

**NOTE: Signal Polarity is NOT inverted**

<b><u>Bit</u></b>	<b><u>Function</u></b>
0	Set Low
1	STROBE
2	Set Low
3	Beam Zero
4	Set Low
5	Word Zero
21:6	DATA(15:0)
22	Set Low
23	Set Low

NOTE: Due to the number of pins connecting the COT Transition module to the VME Backplane the Word\_Zero, Beam\_Zero and Strobe signals of RAM H are not sent thru the backplane to the COT transition module. The COT Transition module sends the Word\_Zero, Beam\_Zero and Strobe signals from RAM G with the DATA(15:0) from RAM H to the Cable H port. This means that in order to send data on Cable H the Word\_Zero, Beam\_Zero and Strobe signals from RAM G must also be sent.

**For example, to send a pattern of all Prompt hits followed by no Delay hits, a user would**

- (0) make sure 132ns CDF\_Clock is running on backplane
- (1) set the “Enable VME access to RAM” bit in the control register
- (2) load the following pattern into the RAM Bank A, B, C, D, E or F

```
0x3FFFE2  
0x3FFFC0  
0x3FFFC2  
0x000000  
0x000002  
0x000000
```

- (3) clear the “Enable VME access to RAM” bit in the control register
- (4) Set the Word Count Register to 0x3
- (5) set the “Enable RAM Data to Ansley Cables” bit in the Control register

The data will now begin pumping up the Cable in a looping pattern