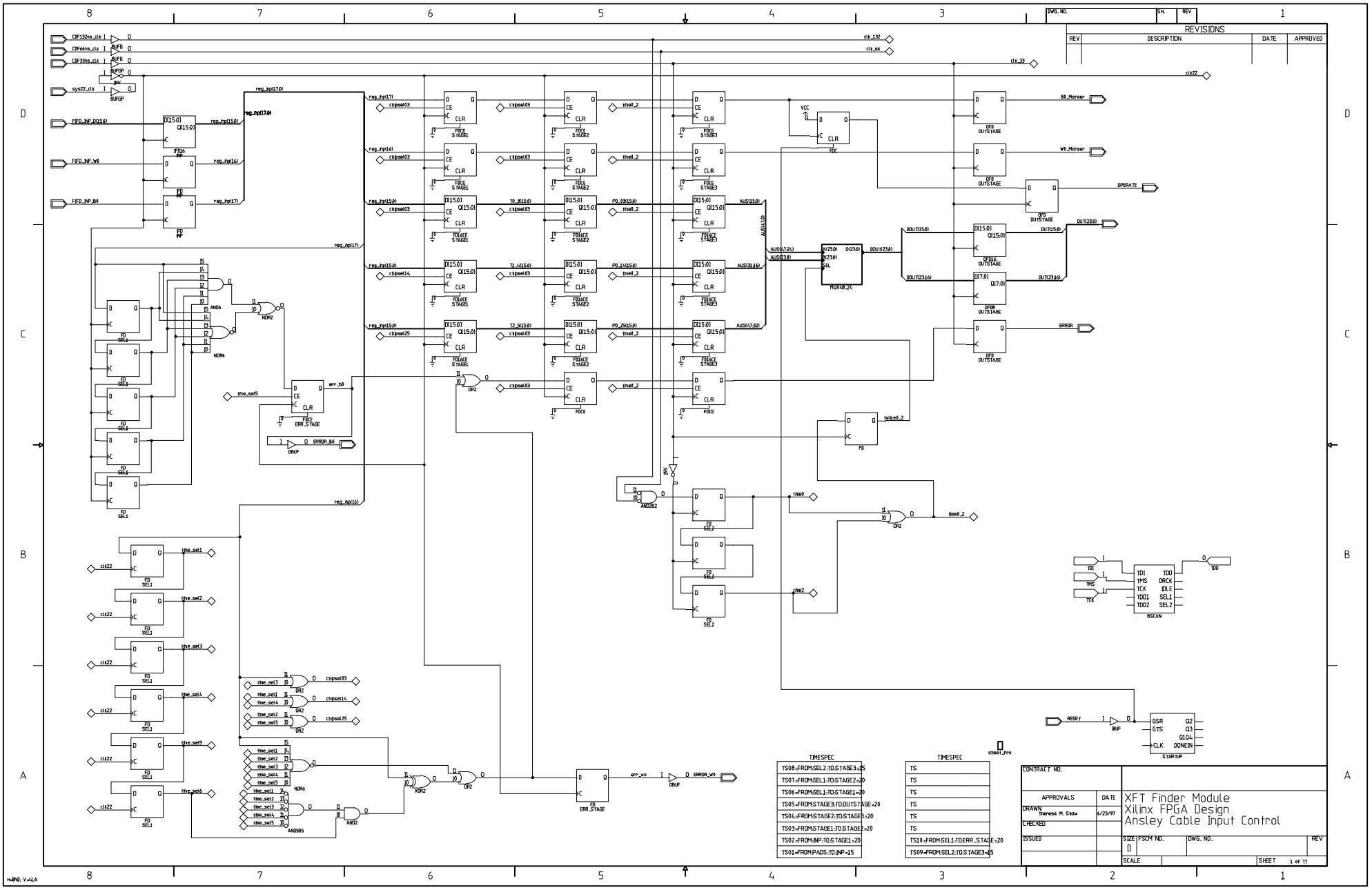
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
TIMESPEC
TS08=FROM:SEL2:TO:STAGE3=15
TS07=FROM:SEL1:TO:STAGE2=20
TS06=FROM:SEL1:TO:STAGE1=20
TS05=FROM:STAGE3:TO:OUTSTAGE=20
TS04=FROM:STAGE2:TO:STAGE3=20
TS03=FROM:STAGE1:TO:STAGE2=20
TS02=FROM:INP:TO:STAGE1=20
TS01=FROM:PADS:TO:INP=15
TIMESPEC
TS
TS
TS
TS
TS
TS
TS10=FROM:SEL1:TO:ERR_STAGE=20
TS09=FROM:SEL2:TO:STAGE3=15
CONTRACT NO.
APPROVALS
DATE
DRAWN
Theresa M. Shaw
6/23/97
CHECKED
ISSUED
XFT Finder Module
Xilinx FPGA Design
Ansley Cable Input Control
SIZE
D
FSCM NO.
DWG. NO.
REV
SCALE
SHEET
1 of ??
HAND: V-4LA