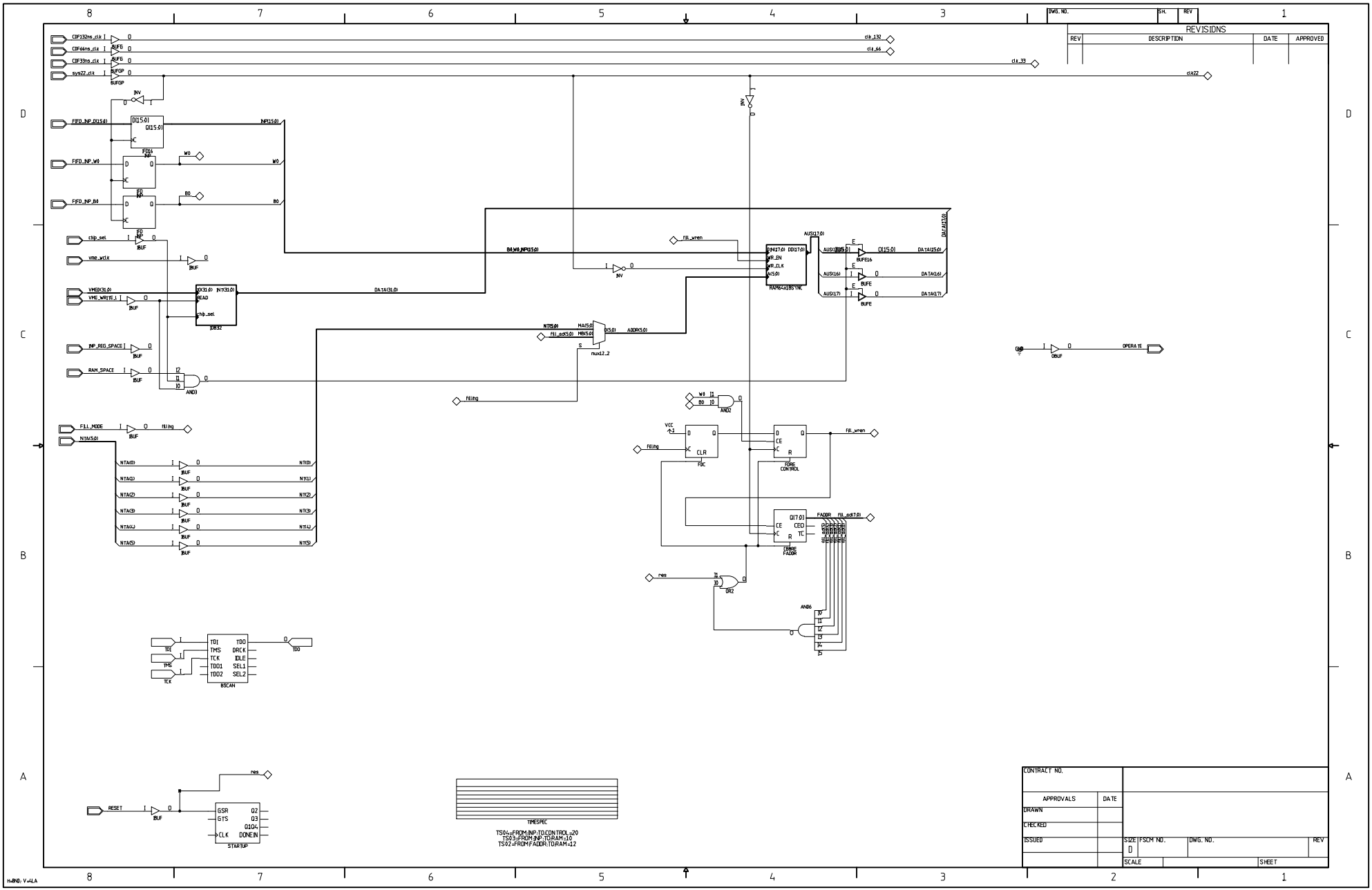
DWG. NO.
SH.
REV
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
CONTRACT NO.
APPROVALS
DATE
DRAWN
CHECKED
ISSUED
SIZE
D
FSCM NO.
DWG. NO.
REV
SCALE
SHEET
CDF132ns_clk
CDF66ns_clk
CDF33ns_clk
sys22_clk
clk_132
clk_66
clk_33
clk22
INV
FIFO_INP_D(15:0)
D(15:0)
Q(15:0)
INP(15:0)
FDR6 INP
FIFO_INP_W0
W0
FD INP
FIFO_INP_B0
B0
chip_sel
vme_wclk
IBUF
VME_D(31:0)
VME_WRITE_L
IDC32
DC(31:0)
NT(31:0)
READ
chip_sel
DATA(31:0)
B0,W0,INP(15:0)
fill_wren
RAM64-(18S)16L
DN(17:0)
DO(17:0)
WR_EN
WR_CLK
A(5:0)
AUS(17:0)
AUS(15:0)
AUS(16)
AUS(17)
BUFE16
BUFE
DATA(25:0)
DATA(16)
DATA(17)
DATA(17:0)
NT(5:0)
fill_adr(5:0)
MA(5:0)
MB(5:0)
ADDR(5:0)
mux12_2
INP_REG_SPACE
RAM_SPACE
AND3
filing
W0
B0
AND2
OBUF
OPERATE
FILL_MODE
NTA(5:0)
NTA(0)
NTA(1)
NTA(2)
NTA(3)
NTA(4)
NTA(5)
NT(0)
NT(1)
NT(2)
NT(3)
NT(4)
NT(5)
VCC
CLR
FDC
CE
C
R
FDRE
CONTROL
fill_wren
Q(7:0)
CEO
TC
FADDR
fill_adr(7:0)
CDRSE
FADDR
res
OR2
AND6
TDI
TMS
TCK
TDO
BSCAN
TDO1
TDO2
DRCK
IDLE
SEL1
SEL2
RESET
GSR
GTS
CLK
Q2
Q3
Q1Q4
DONEIN
STARTUP
TIMESPEC
TS04=FROM:INP:TO:CONTROL=20
TS03=FROM:INP:TO:RAM=10
TS02=FROM:FADDR:TO:RAM=12
H.BND: V.4LA