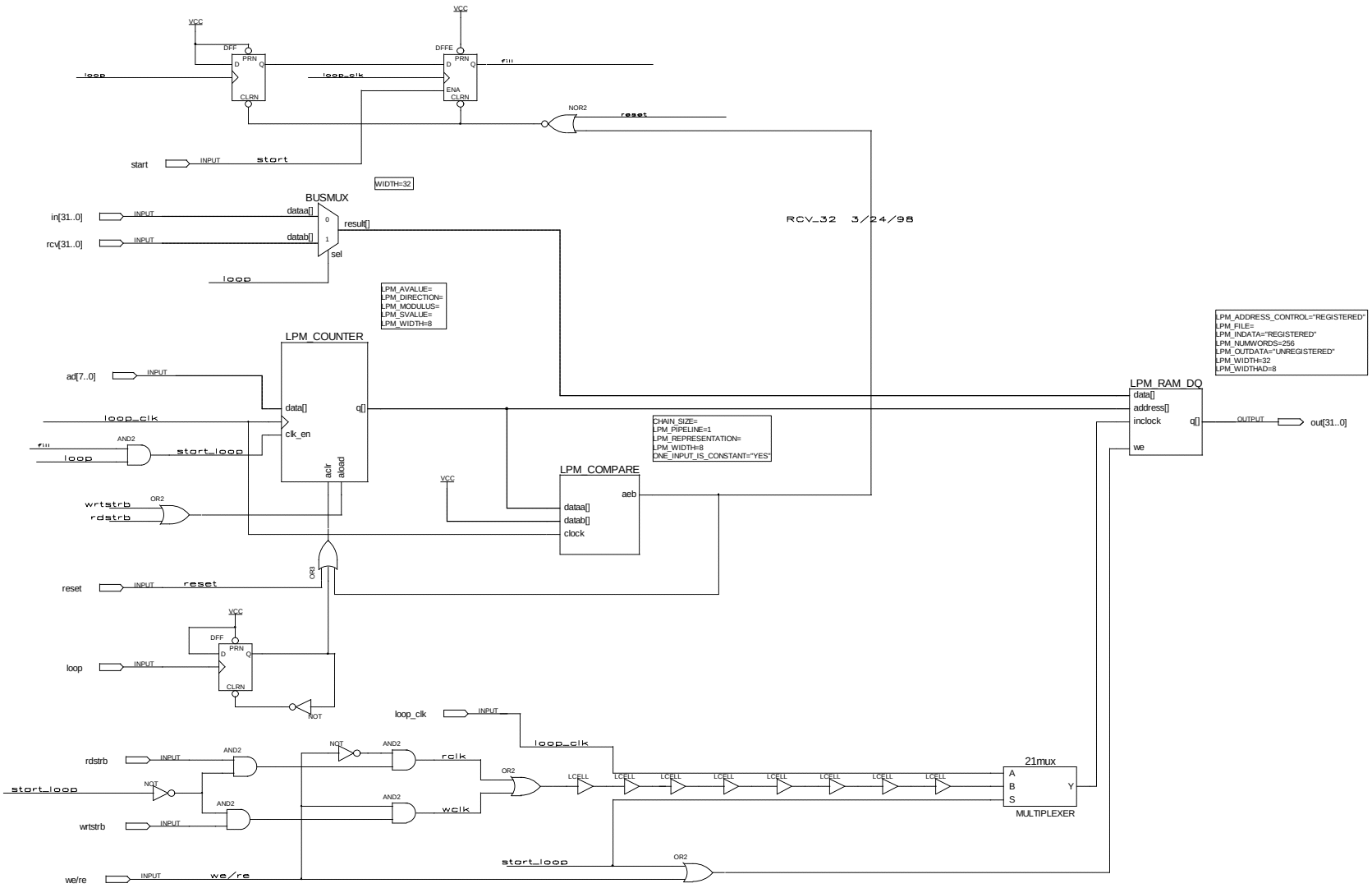
VCC
DFF
PRN
D
Q
CLRN
loop
loop_clk
DFFE
ENA
fill
NOR2
reset
start
INPUT
WIDTH=32
BUSMUX
in[31..0]
rcv[31..0]
dataa[]
datab[]
result[]
sel
RCV_32 3/24/98
LPM_AVALUE=
LPM_DIRECTION=
LPM_MODULUS=
LPM_SVALUE=
LPM_WIDTH=8
LPM_COUNTER
ad[7..0]
data[]
q[]
clk_en
aclr
aload
AND2
start_loop
OR2
wrtstrb
rdstrb
CHAIN_SIZE=
LPM_PIPELINE=1
LPM_REPRESENTATION=
LPM_WIDTH=8
ONE_INPUT_IS_CONSTANT="YES"
LPM_COMPARE
aeb
clock
LPM_ADDRESS_CONTROL="REGISTERED"
LPM_FILE=
LPM_INDATA="REGISTERED"
LPM_NUMWORDS=256
LPM_OUTDATA="UNREGISTERED"
LPM_WIDTH=32
LPM_WIDTHAD=8
LPM_RAM_DQ
address[]
inclock
we
OUTPUT
out[31..0]
NOT
rdstrb
wrtstrb
we/re
we/re
rclk
wclk
LCELL
21mux
A
B
S
Y
MULTIPLEXER