```
include "lpm_mux";

SUBDESIGN rmxsl2
(
    start, clk,  reset  : INPUT;
    B0_in,W0_in,ER_FLAG : INPUT;
    w_in[139..0]        : INPUT;
    wout[46..0]         : OUTPUT;
    wfifo[26..0]        : OUTPUT;
    B0_out              : OUTPUT;
    Word0_out           : OUTPUT;
    Er_flag_out     : OUTPUT;
    load_fifo           : OUTPUT;
)
VARIABLE
    remux1_4: MACHINE WITH STATES (S0,S1,S2,S3);
    mux1 : lpm_mux with (lpm_width=47, lpm_size=4, lpm_widths=2);
    XXX[3..0][46..0] : NODE;
    mux2 : lpm_mux with (lpm_width=27, lpm_size=4, lpm_widths=2);
    ZZZ[3..0][26..0] : NODE;
    mux_sel[1..0]   : NODE;
    wout[46..0]     : dff;
    wfifo[26..0]    : dff;
    B0_out          : dff;
    Word0_out       : dff;
    Er_flag_out     : dff;
    load_fifo       : dff;


BEGIN
    xxx[0][] = (w_in[120..108],w_in[84..71],w_in[49..41],w_in[39],w_in[13..12],w_in[10..3]);
    xxx[1][] = (w_in[126..114],w_in[90..77],w_in[55..47],w_in[45],w_in[19..18],w_in[16..9]);
    xxx[2][] =
(w_in[132..120],w_in[96..83],w_in[61..53],w_in[51],w_in[25..24],w_in[22..15]);
    xxx[3][] =
(w_in[138..126],w_in[102..89],w_in[67..59],w_in[57],w_in[31..30],w_in[28..21]);
    mux1.data[][] = xxx[][];
    mux1.sel[] = mux_sel[];
    wout[].d = mux1.result[];

    ZZZ[0][] = (ER_FLAG,W0_in,B0_in,w_in[121..116],w_in[75..70],w_in[51..46],w_in[5..0]);
    ZZZ[1][] = (ER_FLAG,W0_in,B0_in,w_in[127..122],w_in[81..76],w_in[57..52],w_in[11..6]);
    ZZZ[2][] = (ER_FLAG,W0_in,B0_in,w_in[133..128],w_in[87..82],w_in[63..58],w_in[17..12]);
    ZZZ[3][] = (ER_FLAG,W0_in,B0_in,w_in[139..134],w_in[93..88],w_in[69..64],w_in[23..18]);
    mux2.data[][] = zzz[][];
    mux2.sel[] = mux_sel[];
    wfifo[].d = mux2.result[];


    wout[].clk = clk;
    wout[].clrn = !reset;
    B0_out.clk = clk;
    B0_out.clrn = !reset;
    Word0_out.clk = clk;
    Word0_out.clrn = !reset;
    Er_flag_out.clk = clk;
    Er_flag_out.clrn = !reset;
    load_fifo.clk =clk;
    load_fifo.clrn =!reset;
    wfifo[].clk = clk;
    wfifo[].clrn = !reset;
    remux1_4.clk = clk;
    remux1_4.reset = reset;
```

```
    CASE remux1_4 IS
        WHEN S0 =>
        if start then
            load_fifo.d = vcc;
            B0_out.d = B0_in;
            Word0_out.d = W0_in;
            Er_flag_out.d= ER_FLAG;
            mux_sel[] = b"00";
            remux1_4 = s1;
        else
            B0_out.d = B0_in;
            Word0_out.d = W0_in;
            Er_flag_out.d= ER_FLAG;
            load_fifo.d = gnd;
            mux_sel[] = b"00";
            remux1_4 = s0;
        end if;

        WHEN S1 =>
            load_fifo.d = vcc;
            B0_out.d = B0_in;
            Word0_out.d = W0_in;
            Er_flag_out.d= ER_FLAG;
            mux_sel[] = b"01";
            remux1_4 = s2;
        WHEN S2 =>
            load_fifo.d = vcc;
            B0_out.d = B0_in;
            Word0_out.d = W0_in;
            Er_flag_out.d= ER_FLAG;
            mux_sel[] = b"10";
            remux1_4 = s3;
        WHEN S3 =>
            load_fifo.d = vcc;
            B0_out.d = B0_in;
            Word0_out.d = W0_in;
            Er_flag_out.d= ER_FLAG;
            mux_sel[] = b"11";
            remux1_4 = s0;
    END CASE;
END;
```