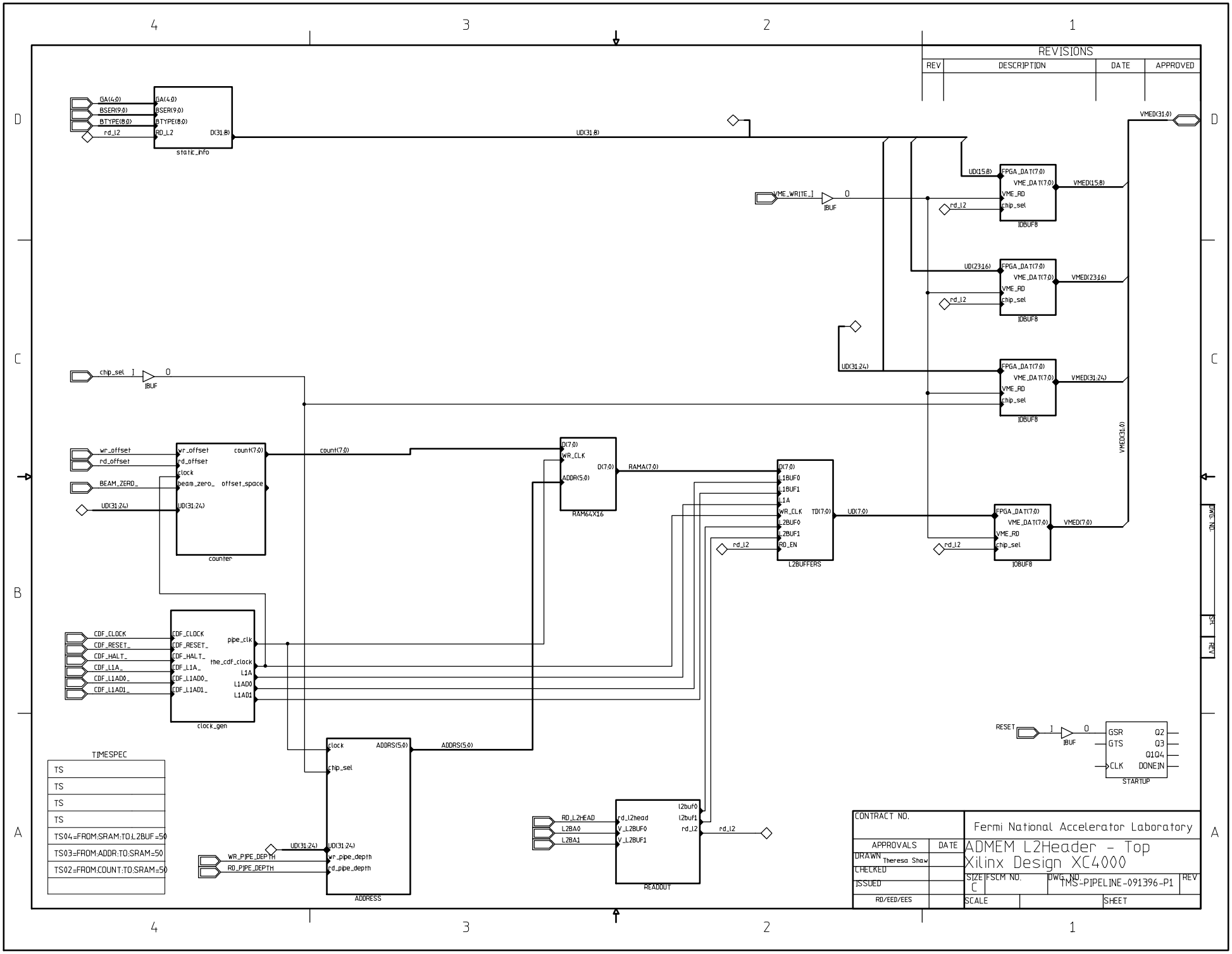
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
GA(4:0)
BSER(9:0)
BTYPE(8:0)
rd_L2
GA(4:0)
BSER(9:0)
BTYPE(8:0)
RD_L2
D(31:8)
static_info
UD(31:8)
VME_WRITE_I
IBUF
O
rd_L2
FPGA_DAT(7:0)
VME_DAT(7:0)
VME_RD
chip_sel
IOBUF8
UD(15:8)
VMED(15:8)
UD(23:16)
VMED(23:16)
UD(31:24)
VMED(31:24)
VMED(31:0)
VMED(7:0)
chip_sel
I
IBUF
O
wr_offset
rd_offset
BEAM_ZERO_
UD(31:24)
wr_offset
rd_offset
clock
beam_zero_
UD(31:24)
count(7:0)
offset_space
counter
count(7:0)
D(7:0)
WR_CLK
ADDR(5:0)
D(7:0)
RAM64X16
RAMA(7:0)
D(7:0)
L1BUF0
L1BUF1
L1A
WR_CLK
L2BUF0
L2BUF1
RD_EN
TD(7:0)
L2BUFFERS
UD(7:0)
rd_L2
CDF_CLOCK
CDF_RESET_
CDF_HALT_
CDF_L1A_
CDF_L1AD0_
CDF_L1AD1_
pipe_clk
the_cdf_clock
L1A
L1AD0
L1AD1
clock_gen
clock
chip_sel
ADDRS(5:0)
ADDRS(5:0)
UD(31:24)
WR_PIPE_DEPTH
RD_PIPE_DEPTH
wr_pipe_depth
rd_pipe_depth
ADDRESS
RD_L2HEAD
L2BA0
L2BA1
rd_L2head
V_L2BUF0
V_L2BUF1
l2buf0
l2buf1
rd_L2
READOUT
RESET
I
IBUF
O
GSR
GTS
CLK
Q2
Q3
Q1Q4
DONEIN
STARTUP
TIMESPEC
TS
TS
TS
TS
TS04=FROM:SRAM:TO:L2BUF=50
TS03=FROM:ADDR:TO:SRAM=50
TS02=FROM:COUNT:TO:SRAM=50
CONTRACT NO.
Fermi National Accelerator Laboratory
APPROVALS
DATE
DRAWN Theresa Shaw
CHECKED
ISSUED
RD/EED/EES
ADMEM L2Header - Top
Xilinx Design XC4000
SIZE C
FSCM NO.
DWG. NO. TMS-PIPELINE-091396-P1
REV
SCALE
SHEET
DWG NO.
SH
REV