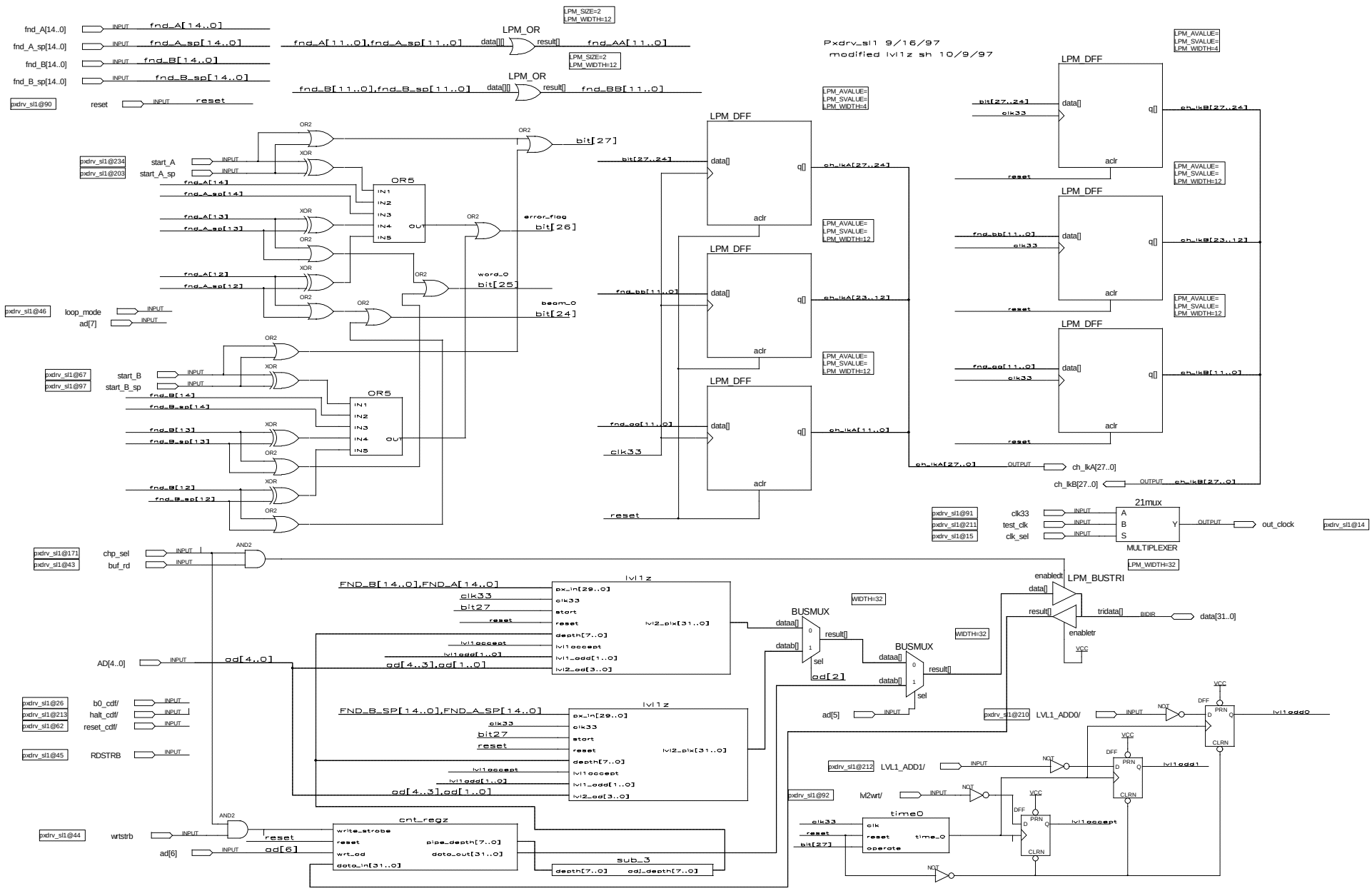
Pxdrv_sl1 9/16/97
modified lvl1z sh 10/9/97
fnd_A[14..0]
fnd_A_sp[14..0]
fnd_B[14..0]
fnd_B_sp[14..0]
reset
LPM_OR
fnd_A[11..0],fnd_A_sp[11..0]
fnd_AA[11..0]
fnd_B[11..0],fnd_B_sp[11..0]
fnd_BB[11..0]
bit[27]
bit[26]
bit[25]
bit[24]
error_flag
word_0
beam_0
start_A
start_A_sp
start_B
start_B_sp
loop_mode
ad[7]
OR5
LPM_DFF
ch_lkA[27..0]
ch_lkB[27..0]
clk33
21mux
MULTIPLEXER
clk33
test_clk
clk_sel
out_clock
chp_sel
buf_rd
AND2
lvl1z
FND_B[14..0],FND_A[14..0]
FND_B_SP[14..0],FND_A_SP[14..0]
AD[4..0]
ad[4..0]
ad[4..3],ad[1..0]
b0_cdf/
halt_cdf/
reset_cdf/
RDSTRB
wrtstrb
ad[6]
cnt_regz
sub_3
BUSMUX
LPM_BUSTRI
data[31..0]
ad[5]
LVL1_ADD0/
LVL1_ADD1/
M2wrt/
time0