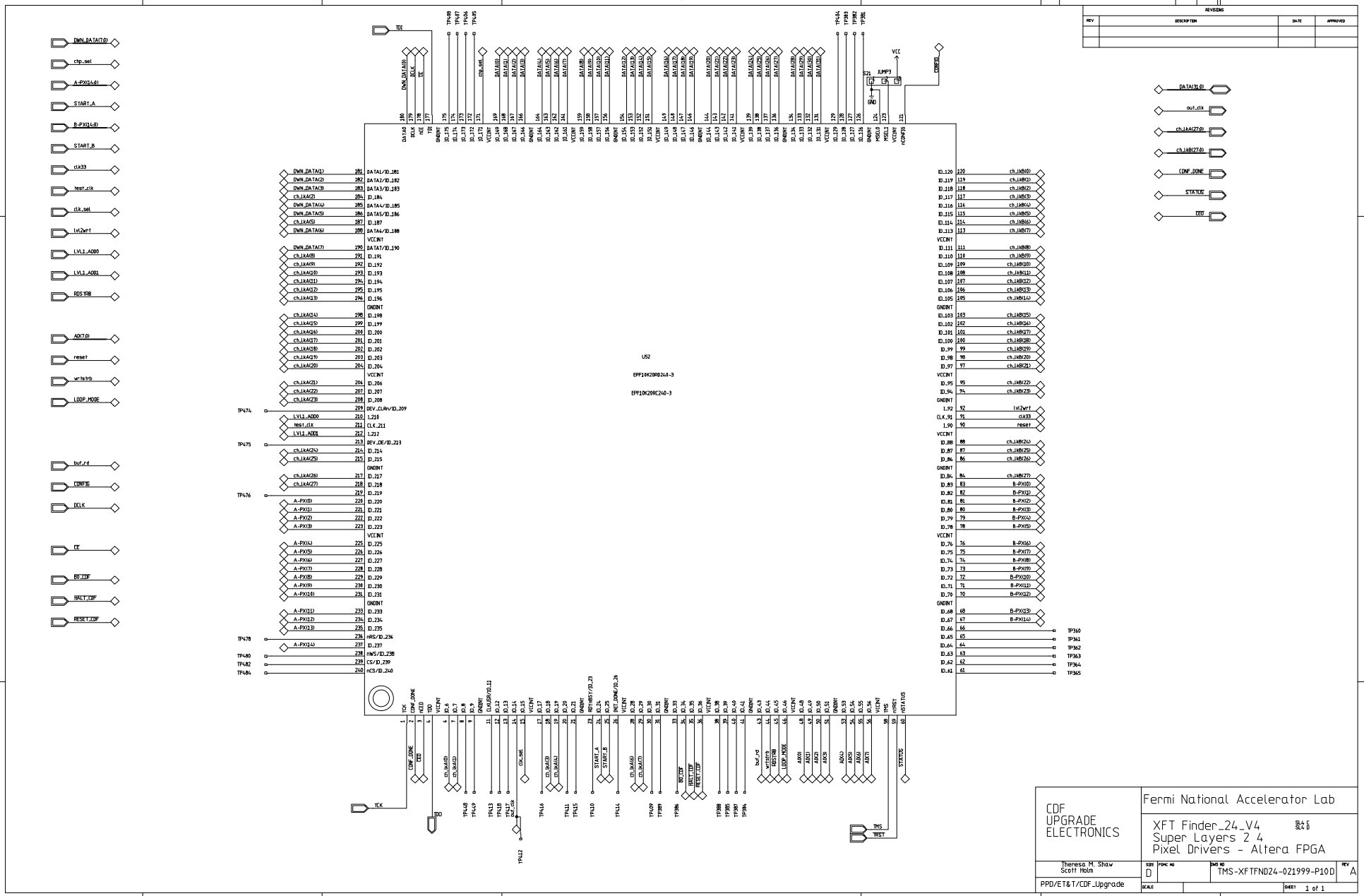
DWN_DATA(7:0)
ctp.sel
A-PX(14:0)
START_A
B-PX(14:0)
START_B
clk33
test.clk
clk.sel
LV12wrt
LVL1_ADD0
LVL1_ADD1
RDS1RB
ADC(7:0)
reset
wr1strb
LOOP_MODE
buf.rd
CONFIG
DCLK
CE
BO_IDF
HALT_IDF
RESET_IDF
DATA(31:0)
out.clk
ch.LkA(27:0)
ch.LkB(27:0)
CONF_DONE
STATUS
CEO
U52
EPF10K20RBD240-3
EPF10K20RC240-3
TDI
TCK
TDO
TMS
TRST
VCC
GND
JUMP3
S21
CONFIG
TP474
TP475
TP476
TP478
TP480
TP482
TP484
TP360
TP361
TP362
TP363
TP364
TP365
DWG NO
SH
REV
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
CDF
UPGRADE
ELECTRONICS
Fermi National Accelerator Lab
XFT Finder_24_V4
Super Layers 2 4
Pixel Drivers - Altera FPGA
Theresa M. Shaw
Scott Holm
PPD/ET&T/CDF_Upgrade
SIZE
D
FSCM NO
DWG NO
TMS-XFTFND24-021999-P10D
REV
A
SCALE
SHEET 1 of 1