

## *Timing Diagrams for XFT FINDER Board*

*S. Holm*

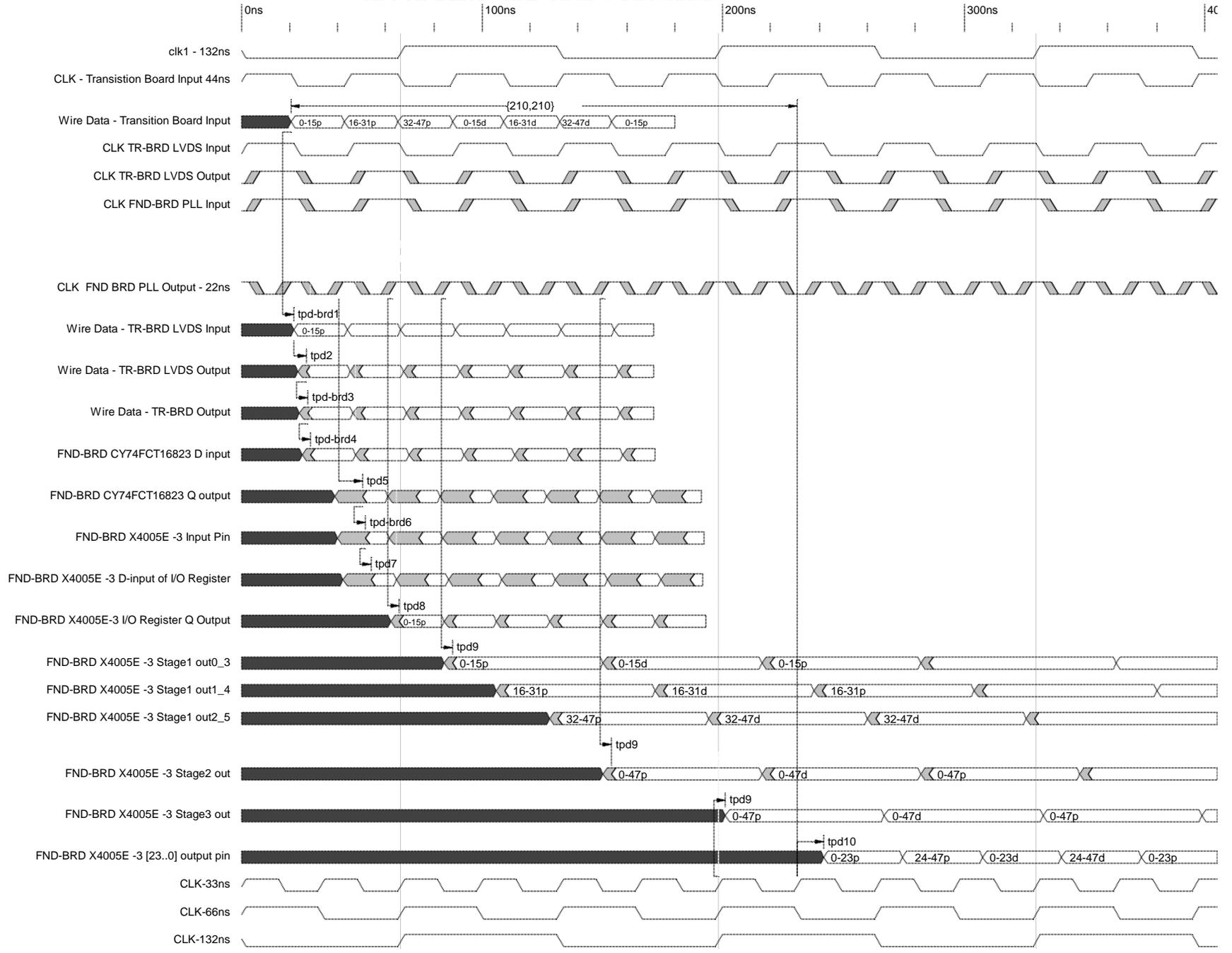
*October 23, 1997*

This note contains two diagrams which show the propagation of data thru the FINDER board. The diagrams were made using Chronology's Timing Designer software. The first diagram shows the delays from the Output of the Ansley Cables to the Output of the XC4005E fpga. The XC4005E device aligns the wire data to the 33ns clock which is derived from the CDF 132ns clock. The "Clk-33ns"(Clk-132ns) signal can be adjusted within the "tSU3 to tHLD3" constraint which according to this diagram is 59.5ns. The delay thru the first diagram from the input edge of wire/clk data on the ANSLEY cable to the CLK-33ns edge which clocks the data to the FINDER CPLD is shown as 210ns, this delay could decrease by 41.45ns(tSU3) or increase by 18.05ns(tHLD3) depending on the relationship of the 132ns CDF clock to the input data.

The second diagram shows the delays from the output of the XC4005E fpga to the LINKER board's Channel Link receiver outputs. Both diagrams have a signal "FND-BRD XC4005E -3 [23..0] output pin", on diagram one this is towards the bottom and on diagram two this signal is towards the top. This signal is the input to the FINDER CPLD device of the second diagram. The CLK-33ns(CLK-132ns) signal is the same on each diagram. The delay thru the second diagram from the CLK-33ns edge which clocks the data to the FINDER CPLD to the CLK-33ns edge which clocks the data to the into the Channel Link driver is 297ns.

The National Semiconductor DS90CR281-DS90CR282 Channel Link pair data sheet gives a specification that relates the Driver's input clock to it's output clock(tCCD) and also the maximum skew(tCCS) between the four differential output pairs and the differential clock pair. These two parameters along with the cable delay(1.7ns/ft) will determine when the differential signals will arrive at the LINKER board. The DS90CR282 channel link receiver specification lists similar parameters for the differential clock in to single ended clock out delay(rCCD) and then a parameter of the single ended data outputs with respect to the single ended clock output(rSRC).

# XFT FINDER BOARD TIMING DIAGRAMS



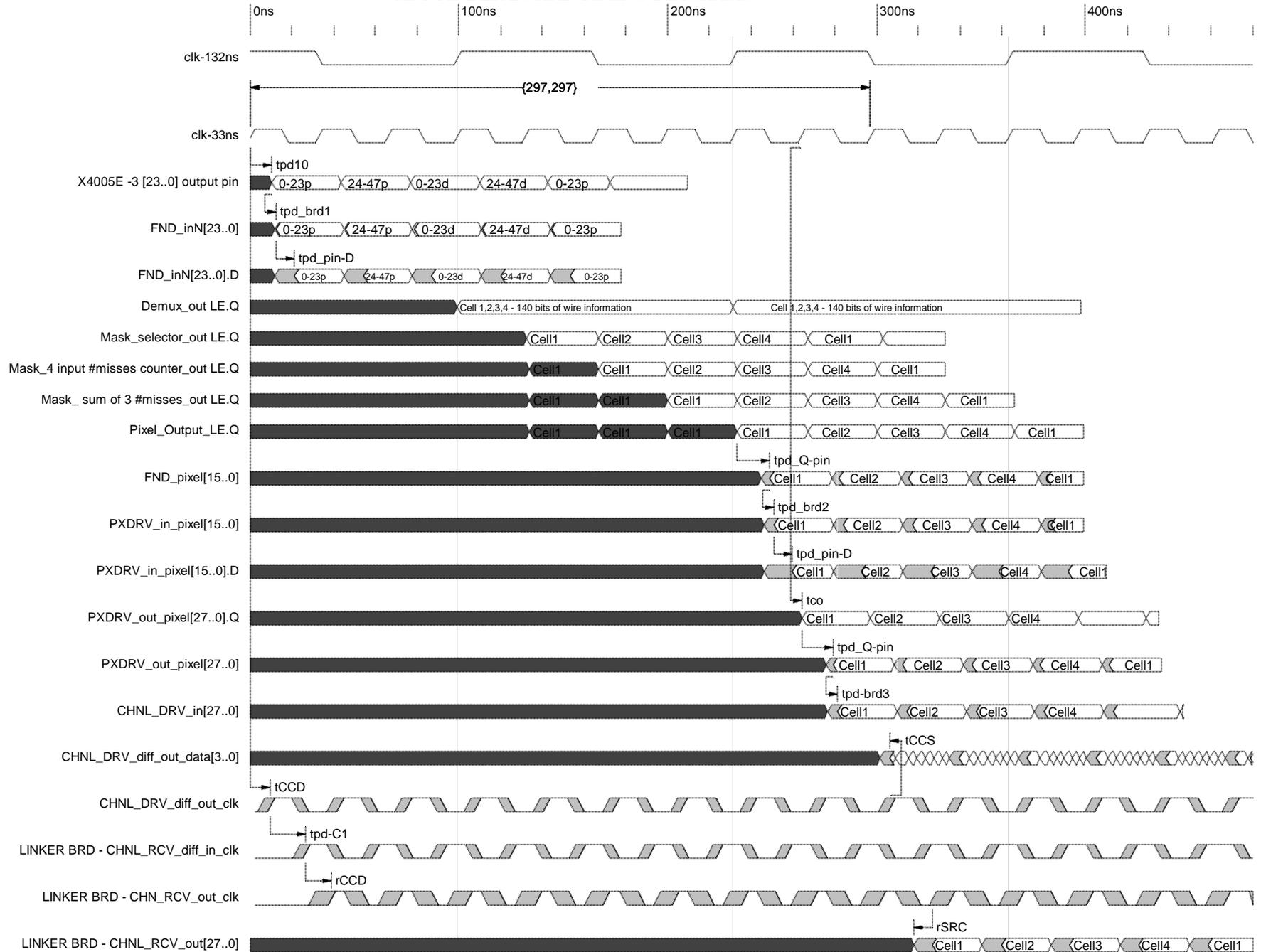
E:\TEMP\XFT2.TD - Diagram 1

XFT FINDER BOARD TIMING DIAGRAMS  
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Row	Name	Formula	Min	Max	Margin	Comment
1	D tpd2	[1.5,5]	1.5	5		National DS90C032 LVDS Receiver propagation delay
2	D tpd-brd1	1	1	1		board delay from TR-BRD cable connector to LVDS input
3	D tpd-brd3	1	1	1		board delay from LVDS output of TR-BRD backplane connector
4	D tpd-brd4	[1,]	1			board delay from FND-BRD input connector to input pin of X4005E
5	D tpd5	[1.5,10]	1.5	10		CY74FCT16823AT tpd clock to Q
6	C tSU1	[3,]	3			CY74FCT16823AT setup time
7	C tHLD1	[1.5,]	1.5			CY74FCT16823AT tHold
8	D tpd-brd6	1	1	1		board delay tpd between register output and Xilinx input
9	D tpd7	2.5	2.5	2.5		XC4005E Tpid Pad to I1,I2
10	C tSU2	[1.2,]	1.2			XC4005E -3 setup time of IFF
11	C tHLD2	[4.5,]	4.5			XC4005E -3 hold time of IFF
12	D tpd8	2.8	2.8	2.8		XC4005E -3 IFF global clock to Q of input flip flop
13	D tpd9	2.8	2.8	2.8		XC4005E -3 tpd CLB gclk to Q
14	D tpd9	2.8	2.8	2.8		
15	D tpd9	2.8	2.8	2.8		
16	D tpd9	2.8	2.8	2.8		
17	D tpd9	2.8	2.8	2.8		
18	D tpd10	10.7	10.7	10.7		XC4005E -3 OFF global clock to Q to output pin of output flip flop
19	M M1				{210,210}	Time for signal to propagate from input connector of TR-BRD to output pin of XC4005-3
20	C tSU3	[3,]	3			XC4005-3 CLB setup time
21	C tHLD3	[0,]	0			XC4005E -3 CLB hold time

E:\TEMP\XFT2.TD - Parameters for Diagram 1

### XFT FINDER BOARD TIMING DIAGRAMS



E:\TEMP\XFT1.TD - Diagram 2

XFT FINDER BOARD TIMING DIAGRAMS

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Row	Name	Formula	Min	Max	Margin	Comment
1	D	tpd_brd1	[1,2]	1	2	board propagation delay between Xilinx{Alingment FPGA} and Altera{Finder}
2	D	tpd10	10.7	10.7	10.7	Xilinx X4005E -3 OFF global clock to Q to output pin of output flip flop
3	D	tpd_pin-D	[0,8.6]	0	8.6	Altera 10k50-3 column pin to LE D input, delay to le + tlut + tcomb + ioe delay, actual min. nu
4	C	tSU1	[2.2,]	2.2		Altera 10k50-3 LE setup time
5	C	tHLD1	[0,]	0		ALTERA 10K50 - 3 LE hold time
6	D	tco	0.2	0.2	0.2	Altera 10k50-3 Clock to Q of LE
7	D	tco	0.2	0.2	0.2	Altera 10k50-3 Clock to Q of LE
8	D	tpd_Q-pin	[11.5,15.2]	11.5	15.2	Altera 10k50-3 LE to pin delay [different row ,two rows] actual min. number isn't given
9	D	tpd_brd2	[1,2]	1	2	board propagation delay between Altera{Finder} and ALtera{Pixel Driver}
10	D	tpd_pin-D	[0,8.6]	0	8.6	Altera 10k50-3 column pin to LE D input, delay to le + tlut + tcomb + ioe delay, actual min. nu
11	D	tCCD	[5,9.7]	5	9.7	DS90CR281 Transmit Clk in to Transmit Clk out delay
12	D	tpd-C1	17	17	17	Proagation delay of 3M 3600 cable 1.7ns/ft @ 10ft length
13	D	rCCD	[7.6,11.9]	7.6	11.9	DS90CR282 Reciever Clk in to Reciever Clk out delay
14	D	tco	0.2	0.2	0.2	Altera 10k50-3 Clock to Q of LE
15	C	tSU1	[2.2,]	2.2		Altera 10k50-3 LE setup time
16	D	tpd_Q-pin	[11.5,15.2]	11.5	15.2	Altera 10k50-3 LE to pin delay [different row ,two rows] actual min. number isn't given
17	D	tpd-brd3	[1,2]	1	2	board propagation delay between Altera{Pixel Driver} and National DS90CR281 Channel Link
18	C	tSU3	[8,]	8		National DS90CR281 Channel Link Driver setup time
19	C	tHLD2	[2.5,]	2.5		National DS90CR281 Channel Link Driver hold time
20	D	tCCS	(-0.35)	-0.35	-0.35	National DS90CR281 Channel Link Driver Transmit out Channel to Channel Skew
21	D	rSRC	(-9)	-9	-9	National DS90CR281 Channel Link Reciever Setup to clk out delay
22	M				{297,297}	

E:\TEMP\XFT1.TD - Parameters for Diagram 2