

FINDER MODULE CHECKOUT PROCEDURE

3/9/00

1. Visual inspection of correct parts and orientation.
2. Power to ground short test using ohm meter
The value on the meter should read
SL1/3 board = 2.8 ohms
SL2/4 board = 2.8 ohms
3. Install Jumpers in a manner similar to the sample module.
4. Install EPROMS. (Use the sample module's EPROMS as a means to program the new modules EPROMS using the Data I/O's quick copy routine).
5. Install ID PROM.
6. Install serial number tag.
7. Break shunts that identify the board type and serial number. (The shunts represent a hex value of the decimal board type and serial number)
8. Install module keys into front panel. Use sample module.
9. Power to ground short test using ohm meter.

Plug board into slot 18 in standalone crate "Tornado", with power off.

Crate should contain:

MV162 – "Tornado" slot 1

Testclkv7 slot 8,

1-Channel Link boards slot 4

Open an xterm window connected to 'b0dau30'

Log on using your password.

Type "source setup_162"

Type "cd xft"

Type "cd xftdaq"

Type "xftdaq &"

! This opens the XFTDAQ java - a window labeled "Generic Data Acquisition Control" (GDAC) will appear.

If the "GDAC" was last used in the same crate click on the DAO

10. Select the “Finder Register Tests” tab.

In the General Register Tests pulldown area select “Test All general Registers” and click on the execute button. If there are errors open the GDAC window to verify them, the actual write/reads are reported in that window. Yellow LED on front panel should blink a few times.

11. ID PROM test – select the “Register Access Panel” tab, select the ID PROM button, the window should display the contents in the following format. “00XX 05Z Finder SL 1/3 Ver. 4.0” where XX represents the module ID number, 05Z represents the module type. Record this number in the logbook.

12. Clock Generation and Distribution - select the “Register Access Panel” tab and set the “Clock Delay Register” value. With an Oscilloscope compare waveform on scope to master printout. May have to turn backplane clock on in Testclk module.

1. Validate the amount the register can adjust the master clock.

- **SL1/3 board –**
 - U27 pin 1 input pin 15 output
 - Set clk delay to 00h record the skew in-out.
 - Set clk delay to 30h record the skew in-out.
 - Set clk delay to 60h record the skew in-out.
- **SL2/4 board –**
 - U28 pin 1 input pin 15 output
 - Set clk delay to 0h record the skew in-out.
 - Set clk delay to 30h record the skew in-out.
 - Set clk delay to 60h record the skew in-out.

2. Validate the phase and frequency of the clock signals from the Main Robo clock: 33ns, 66ns, & 132ns. See attached drawing.

- **SL1/3 board –**
 - U44 pin 1 - 132ns(input)

13. Reset Switch Test. Validate with an oscilloscope that the Reset Switch and PAL is operating properly. With the switch depressed the following output pins of U21 should be low:

/XPROGRAM –	pin 2
/XPROGRAM_INP –	pin 4
/SL1_CONFIG –	pin 5 or SL2
/SL3_CONFIG –	pin 6 or SL4
/PX_CONFIG –	pin 7

The front panel LEDs should act as such:

Top LED(Red) should remain unchanged,

2nd LED(yellow) will blink,

3rd LED(green) will turn on while switch is depressed.

4th LED(Red) will blink when switch is released.

If there are no programs in the Flash RAMs the green LED will not be on.

14. FLASH RAM LOADING

Select the FlashRam Loading tab and download designs to the 4 programmable PLD chains. Select the “FILE CHOOSER” button, a window will appear that allows you to select the file. In the filter area of the window locate the following directory “cdf/people2/rklein/software/*”. After the filter is invoked scroll down the files menu until you find the appropriate file and double click. Click the enable download box and the correct chain box followed by the green “Reprogram from design file above” button. The download will take a number of minutes. The color on the button will change when the procedure is finished and the current programs in the FlashRam will be displayed in the GDAC. When a FlashRam is finished downloading click the “Force Download” button to download the contents of the FLASH into the PLD chain. The green LED should go off and then back on within 7 seconds.

15. Open the ScanPlus Runner software using the Windows “Start” button on the PC. Using the File pulldown menu select “Open Test Plan”. The popup window will allow you to select the correct folder and file which are listed below. Attach the appropriate cable between the Finder Board under test and the Corelis PCI board in the PC.

SL13 = SL13_Coreleis_V4/SL13_V4.tsp

SL24 = SL24_Coreleis_V4/SL24_V4.tsp

Click the Run Test button.

16. Return to the “Finder Register Tests” by selecting that tab. Test the Dead Wire registers and Finder Pipeline Depth registers by selecting the “Test all” selection in the pulldown menus in each area followed by the execute button.

17. Select the “Finder Ram Tests” tab and test the Alignment and Pixel Diagnostics Rams. Use the “Test all...” selection.

18. Select the “Solo Testing” tab, insert the file name “SL1_3miss_75_cell3” or “SL3_3miss_30” or “SL2_3miss_30” or “SL4_3miss_30” into the input/output file stub and run the test. This performs a short test of the Finder algorithm – testing the masks.

Download the following designs into the FLASHRAMS.

PLD	Finder SL1/3	Finder SL2/4
Pixel	px13_3.hex	px24_4.hex

19. Return to the “Finder Register Tests” by selecting that tab. Test the Pixel Pipeline Depth registers by selecting the “Test all” selection in the pulldown menu.

20. L2Header test. This test will load the Alignment RAMs with a set of data, the correct pipeline depth values, pipeline offset values and the correct

Download the following designs into the FLASHRAMS.

PLD	Finder SL1/3	Finder SL2/4
Finder 1 or 2	fnd_pass_4.hex	fnd_pass_3.hex
Finder 3 or 4	fnd_pass_4.hex	fnd_pass70_5.hex

Plug 2 Channel Link cables into the Finder board and into the appropriate input connectors on the 2 Channel Link boards.

21. Select the “Finder to Channel Link Board” tab, select the correct input/output file stub (sl13_longterm or sl24_longterm). The patterns sent from the Alignment chips to the Channel Link board are 05AF, walking ones and walking zeros. Start the test.

The remainder of the tests will be done in the two-crate system in which Ansley driver modules will be used to test the Input/Alignment connections and the timing of front end of the Finder board. There will be a short-term test followed by an overnight or weekend test.

System Setup with power off:

Finder Crate should contain:

*Power PC – “Terran” slot 1
Tracer slot 2,
SL13 transition boards slot 10,11,12
SL13 Finder Board slot 11
or
SL24 transition boards slot 19,20,21
SL24 Finder board slot 20*

Ansley Driver Crate should contain:

*Power PC – “Monkeys” slot 1
Testclk slot 3
Tracer slot 4
Clk Fanout slot 5
Ansley Drivers slot 7,9
COT transition boards slot 9*

The clock cabling is as follows: A cable should run from the Testclk modules “Clock Emulator” port to the Clk Fanout module’s “Input” port. Cables should go from the Clk Fanout module’s “outputs” to the Tracer’s “CDF Clock Input” port, one for each Tracer. An optical link fanout should be used to connect the Testclk module’s “TSIE” port to the two Tracer module’s “TSI Input” port.

Type "cd xft"
Type "cd xftdaq"
Type "xftdaq &"

! This opens the XFTDAQ java - a window labeled "Generic Data Acquisition Control" (GDAC) will appear.

If the "GDAC" was last used in the same crate click on the DAQ pulldown and click on the "INIT SYSTEM" button to initialize the crate.

If it doesn't work you may have to configure the crate under the FILE pulldown using the "Edit config." option.

Under the Board Status pulldown select "Finder Board". A finder board status window will appear.

Download the following designs into the FLASHRAMS.

PLD	Finder SL1/3	Finder SL2/4
Input-Alignment	xft_inp13v2.exo	xft_inp24v2.exo
Finder 1 or 2	fndrcv_4.hex	fndrcv_3.hex
Finder 3 or 4	fndrcv_4.hex	fndrcvk70_5.hex
Pixel	px13_3.hex	px24_4.hex

22. Select the "Finder Ram Tests" tab and test the Finder Diagnostics Rams.

This concludes the initial testing of the Finder board in the "Tornado" standalone crate.

23. Select the "Register Access Panel" tab and set the "Clock Delay Register" value to 20h.

24. In the GDAC window select pulldown menu Board Status, AnsleyBoard.

25. Run the test of multiple patterns.

26. Perform a Long-term test with other Finder modules, up to 4 Finder modules can be run together. Plug them into Slots 4,5,6,7(SL1/3) and

27. A method will need to be determined to validate the 4 error registers, the Finder error register section may be able to be validated by loading up Alignment Rams with incorrect data and then checking the error registers. A whole section may need to be dedicated to this. The error registers can be viewed by clicking on their buttons found in the “Register Access Panel”; writing the correct bits in the Control register, which can be accessed under the same Panel, can clear them.

