L2 μ INTERFACE UPDATE
4/19/02

FRED M. NIELL
U OF M

- STATUS OF BOARD
  - MEZZANINES
    - BUFFER
    - MAGIC BUS CONTROLLER
  - 9U BOARD
- FPGA FIRMWARE
  BUFFER FIRMWARE
  BUS CONTROLLER FIRMWARE
  TOM, STEPHEN
- TESTING
  - MUON TEST CARD, ERIC J.
  - VME CRATE CTRL
  - MICHIGAN TEST STAND

  - SCALEABLE DESIGN -

BOARD STATUS:

- **BUFFER MEZZANINES**
  - 5 ASSEMBLED, TEST GOOD
    - PARTS FOR REMAINING BEING ORDERED NEXT WK (4/24)
  - TEST STAND + FIRMWARE SET UP FOR TESTING MEZZANINES

    JTAG PROGRAMMING

    USING VIRTEX SERIES I.S.P. NON-VOLATILE PROMS (JTAG PROG.)
  - LEADTIME 2 WKS FOR REMAINING PARTS

BOARD STATUS:

- L2 μ INTERFACE 9U BOARD
  - LAYOUT, ARTWORKS DONE.
  - CROSSTALK SIM. DONE - CHANGES MADE, BOARD REVISED
  - BOARD REVIEW W/ G. FIELD 2/28/02 MULTIPLE SUBSEQUENT REVIEWS IN-HOUSE
  - BOARD QUOTES RECD 4/3/02
    - MANUFACTURE UNDERWAY.
    - SHIPPING DATE 4/24/02 FOR 5 9U BOARDS.
    - ASSEMBLY IN-HOUSE W/ OVEN
      - J. AMEEL, F. NIELL ASSEMBLING.
  - LINE-ITEM PARTS ORDERED FOR STUFFING 5 BOARDS 4/16/02
    - PARTS COMING ~ 4/30/02
  - REMAINING PARTS WE HAVE ON HAND FROM TDC + OTHERS—
- REMAINING TASKS:
  - DESIGN FRONT PANEL (4/30/02) *
  - ASSEMBLE BOARD (5/7/02) *
  - TESTING OF BUFFER MEZZANINES WITH VME INTERFACE THRU CRATE CTR'LR

* EXPECTED DATES

BOARD STATUS:

MAGIC BUS INTERFACE MEZZANINE

- SCHEMATICS DONE
- LAYOUT IN PROGRESS (4/30/02)
- QUOTES GO OUT (5/7/02)
- BOARDS BACK, ASS'Y (5/22/02)

- FULL TESTING OF INTERFACE BOARD AT MICHIGAN (5/27/02)

FIRMWARE STATUS

- BUFFER MEZZANINE FIRMWARE
  - SIMULATIONS INDICATED CHANGES IN EV_LOADED
  - SUMMARY OF FUNCTION:

    ① MATCHBOX/PREMATCH → L1 ACCEPT
    ↓ HLINK
    L2 μ → DP ASIC → BUFFER

    ② BUFFER DECODES BC, CHECKS-LOADS DATA INTO RAM
    ③ LOGIC IN FPGA "ORS" DATA BITS IN 15° WEDGES + PREMATCH BITS ⇒ 127 BITS PER BUFFER # IN L1
    ④ SENDS FLAG BITS, EV-LOADED
    ⑤ WAITS FOR X ADDRES BITS REQ.
    ⑥ SENDS DATA (MAYBE)
    ⑦ CLEARS RAM, LOADS NEXT DATA

    → HYPER-MODE (SUGGESTED) SKIP FLAG BITS, HAVE MAGIC INT. FPGA REPORT SALIENT μ'S SINCE L2 PROCESSING TIME WOULD ALLOW 7 OR SO μ'S TO BE X'MTD ....

  - FINE IN STANDALONE, WHEN MAGIC INT SIM TALKS → EV_LOADED ... FIXED.

  - LOADS ONTO FPGAS OK

FIRMWARE STATUS

- MAGIC INTERFACE
  - VERILOG TOM WRIGHT
  - SUMMARY:

    1. WAITS FOR EV-LOADED, TAKES DATA FROM BUS
    2. SENDS FLAG BITS OVER M-BUS OR VME
    3. WAITS FOR K, DECODES ADDRESS INTO BUFFER ADDRESS
    4. REQUESTS DATA FROM BUFFER
    5. SENDS DATA OVER M-BUS OR VME.

ALSO

- DECODES INTERNAL ERROR BUS
- DISPLAYS STATE MACHINE, ERRORS, ER. ON HEX DISPLAY ON FRONT PANEL
- MODE SELECTION VIA VME

POSSIBLE FUTURE IMPLEMENTATION:

- HIGH SPEED, SKIP FLAG BITS
- VIRTEX 1024 FRAME LOGIC ANALYZER IN FPGA LOGIC - JTAG SUPPORTED

BUILT IN - NO EXTRA CLB'S !

XCV1000 - 4FG

TESTING/COMMISSIONING

- ERIC'S μ-TEST BOARD FOR PATTERN GENERATION
- 1024 FRAME-BUFFER ON FPGA
- SPARE MATCHBOX

- BOARD WAS DESIGNED TO OPERATE W/ ANY NUMBER OF HL FIBERS - SO 1-2 SPLITTERS IN L2 TEST CRATE OF MATCHBOX HL'S WILL SUFFICE

- AS OUR CONFIDENCE IN THE BOARD INCR. WE CAN ADD MORE + MORE FIBERS UNTIL WE'RE TESTING THE ENTIRE μ DATA STREAM.