



## Spikes Problem for the Trigger?

- CEM spikes have typically contributed  $\sim 100$  Hz to L1 Photon and Jet rates
  - Note that Jet triggers are formed using sum of HAD+EM energy
- Clearly the spike rate is irrelevant for L1 bandwidth of 50kHz
- For  $L \sim 10^{31} - 10^{32}$  the real physics rate will dominate spikes
- There is no spike problem at L1 long term (ie with L2)

Rates for Run 128437  
 $L = 5 \times 10^{30}$

	L1 Rate (Hz)	
	Total	Spikes
Jet 5	1950	240
Photon 8	185	95
Jet 10	205	70



# Spikes Problem for the Trigger?

- At Level 2, we have less bandwidth (300Hz) available and the real physics rates are reduced
- Physics Jet rates are reduced by higher thresholds on clusters but the spike spectrum is harder.
  - The Jet 90 is a guess assuming that the spike fraction at 90 GeV is the same as at 60 GeV.
- For photon triggers the spikes will be killed by requiring CES hits from RECES.
- Until RECES is commissioned the spikes will be a real problem
- Rate for Photon 23 without RECES is estimated using 4718 estimate for Physics and extrapolating spike rate to 23GeV

Rates for Run  
 128437,  $L=5 \times 10^{30}$   
 From CDF 4718  
 Extrapolated spike rates

	L2 Rate (Hz)		
	Physics	Spikes	Total
Jet 15 (PS12)	0.7	0.3	1.0
Jet 60 (PS8)	0.3	1.8	2.1
Jet 90	1.5	9.0	10.5
Photon 23 (No RECES)	1	55.0	56.0
MET 25	?	50.0	



## *Spike Problems and Solutions*

- The spikes also feed directly into the MET triggers where we have no additional handles at L2
  - We have been requiring the CLC to do spike suppression but this has an efficiency of  $\sim 90\%$  for higher Et objects and it appears to roll-off for Low Et jets
- Solution Options:
- For jets could cut on hadronic fraction at L2 (eg  $HAD/EM > 0.05$ )
  - For Photons: get RECES working
  - For Met, require CLC or some other object in the event
  - Kill the spikes when forming trigger towers



## *How to kill Spikes in the Trigger*

- Bob Wagner is working on fixing worst tubes. We do not know exactly what the spike rate will be when he is done. Suppressing the towers in the Trigger will only help.
- In ADMEM, trigger towers are formed using an arithmetic sum of the tubes:  
$$PH(\text{trig}) = \frac{1}{2} (\text{Tube1} + \text{Tube2})$$
 rather than  
$$PH(\text{offline}) = \text{SQRT}(\text{Tube1} * \text{Tube2})$$
  
because there is not enough room in the FPGA to form the products and SQRTs.
- Note that  $PH(\text{trig}) > PH(\text{offline})$  so we are over-efficient relative to offline. Also note that if  $\text{Tube1} \gg \text{Tube2}$ ,  $PH(\text{trig}) \gg PH(\text{offline})$
- Characteristic of spikes is that one tube has large PH and other is near pedestal
  - $\text{ASSYM} = (\text{Tube1} - \text{Tube2}) / (\text{Tube1} + \text{Tube2}) > 0.95$
- It is not practical to look at the ASSYM in the trigger. However, we can suppress towers where one of the tubes is essentially at pedestal



## *How to kill Spikes in the Trigger*

- General idea:
  - Add two tubes together (after pedestal subtraction)
  - If one or both tubes has less than 8 counts above pedestal, suppress the sum (set it equal to 0)
  - Then add two towers to form trigger tower
- What will this do to the spike rates?
  - Assume pedestal is 3.5 counts (gross over-estimate)
  - Cut is at about 2 sigma
  - We cut out low tail and 90% of high tail
  - Implies we should get a rejection factor of at least 20
  - Real factor is probably closer to 100
  - Means that L1 spike rates ~ few Hz, L2 photon spike rate is ~ 1Hz



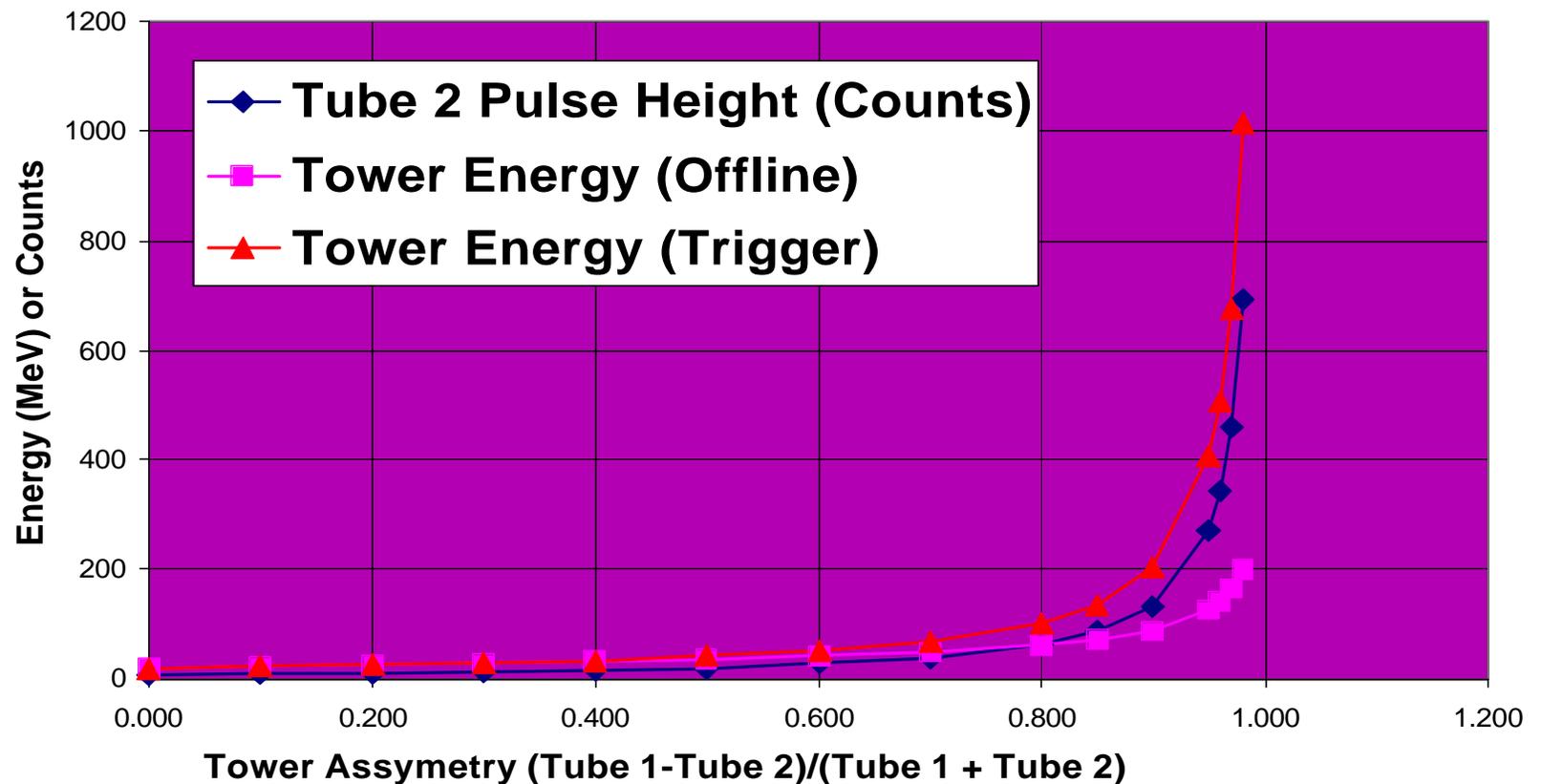
## *How to kill Spikes in the Trigger*

- What happens to real physics?
  - At 95% asymmetry, the highest Et tower that would be rejected has 406 MeV in the Trigger but only 125 MeV in offline
  - At 90% asymmetry, the highest Et tower that would be rejected has 203 MeV in the Trigger but only 88 MeV in offline
  - Remember that LSB in trigger is 125 MeV
  - Also, effect will be diminished further by Et weight
  - Very slight change in turn-on curves for triggers
- Effect from using  $Z=0$  for calculation of Et weight in the Trigger is much larger than spike killer



## Trigger vs Offline Tower Energy

- Lines represent Tube 1 with 7 counts, Towers below the line suppressed Spike Killer Effect





## *Implementing Spike Killer*

- Terri Shaw has made a new new version of the Trigger sum algorithm for the ADMEM implementing the spike killer.
  - It has been tested by Lee Scott in the 14<sup>th</sup> floor test-stand
  - There is no change in the timing
- We will make one slight modification which will allow the spike killer to be enabled/disabled using the MSB of the Trigger pedestal register (we didn't need 8 bits)
  - For the Plug 4 channel sums, CHA and WHA this would be disabled via a parameter in the hardware database
  - For the CEM we would make this a Trigger table parameter so that we can make tables with or without the spike killer
- Note that the Spike Killer will affect all L1 and L2 triggers using CEM energies. This is implemented at the Trigger tower formation.
- **Propose to switch to using the Spike Killer before the end of the shutdown.**



# *Problem with Pedestals in ADMEM*

Peter Wilson 9  
Calorimeter  
Meeting  
Oct 24, 2001

- Remember: Café FRAM converts the QIE range bits + FADC to a two piece linear output (factor of 8 gain difference in ranges) and adds a fixed pedestal value of 50 counts for every channel
- Trigger FPGA on ADMEM converts this to single range with no pedestal before summing the channels
- **The problem: the pedestals are being handled differently in these two places.**
- The symptom was small (few count) disagreements in checking trigger tower energies between that read out from DCAS with a simulation based on the D banks from the ADMEMs.
  - This was particularly noticeable for CEM spikes!
  - **Credit should go to Carla for being persistent about the disagreements**



# *Problem with Pedestals in ADMEM*

Peter Wilson 10  
Calorimeter  
Meeting  
Oct 24, 2001

## Café FRAM:

1. Linearize QIE+FADC (18bits)
2. Add pedestal of 50 counts
3. If  $>0x7fff$  (15 bits) shift right by 3 bits (divide by 8) and Set bit 15 high

## Trigger FPGA:

1. Subtract 50 counts
2. If bit 15 is high shift left by 3 bits (Multiply by 8)

If we are in the low range there is no problem. However, if we are in the high range we have a mismatch in the pedestal subtraction. The effective pedestal is 6 but we are subtracting 50 in the trigger!



# *Problem with Pedestals in ADMEM*

Peter Wilson 11  
Calorimeter  
Meeting  
Oct 24, 2001

- Could change Calibration code which generate FRAM download
  - Do pedestal addition after gain correction
  - Need to make certain that adding pedestal does not overflow the 15 bits
  - Need to change offline accessors to reflect this
  - This is easier to change if we mess it up since it is controlled locally at CDF
- Could change Trigger FPGA code to do pedestal subtraction after converting to single range
  - Requires Terri Shaw to change FPGA designs for Plug and Central. However, she is already doing this for the Spike Killer feature.
- **Whichever solution we choose, we should do it before the end of the shutdown.**