



L2 Trigger Commissioning Plan

Stephen Miller

May 31, 2001

CDF Collaboration Meeting



L2 Trigger Status

- Status at 36x36
 - L2 trigger in tagging mode. L1 interface board + Clist board + 1 Alpha
 - Sumet, MissEt, Jet triggers
 - L1 interface board had no errors for 250K events analyzed
 - except in Myron mode (4 L1A in a row)
 - Clist board had some data errors every 10K events.
 - Eta-Phi bits always corrupted



L2 Trigger Status

- **Lots of work since then**
 - L2 Cal System taken apart at start of shutdown and reassembled
 - All J3 backplanes replaced. VME chip replaced on all boards
 - One remaining single bit energy error for 2/3 clustering passes
 - Modification to firmware being tested
 - Integration work with L1, SVT/Track, Clist and Isolist interface boards
 - Firmware fix tested for L1 to handle L1A within 132ns
 - Lots of work on SVT/Track board for receiving data from SVT and XTRP
 - Fix of Eta-Phi data corruption on Clist board
 - Continued testing and improvement of Isolist firmware
 - Standalone test with Alpha and 4 Reces boards
 - Integration tests with 4 interface boards



L2 Trigger Status cont.

- **Outstanding Issues**
 - **Bus Arbitration problem with multiple interface boards**
 - Several boards try to send data at the same time
 - Problem is noise on PECL arbitration lines
 - Most severe on L1 and Isolist boards. Have tried several unsuccessful fixes.
 - Possible solution to be tested at B0 next week.
 - » With fpga kludge, can run with L1, Clist, SVT boards
 - Largest barrier to stable L2 running
 - **Stability of Alpha executable**
 - Code can crash unexpectedly after random number of events
 - Related to data being received by the interface boards
 - **Testing reliability of interface boards with collision data**
 - Especially true for Track and SVT board
 - Need to run for millions of events looking for data errors
 - Can be done with L2 in tagging mode
 - Offline/Trigmon code being written to look at data
 - **Running with Multiple Alphas & optimization of code and firmware**
 - With 1 Alpha, expect L2 time of 20 - 30us per event → 10-20 kHz L1A rate
 - Goal of 10us per event → 45 kHz L1A rate



L2 Processor Status

- **Hardware**

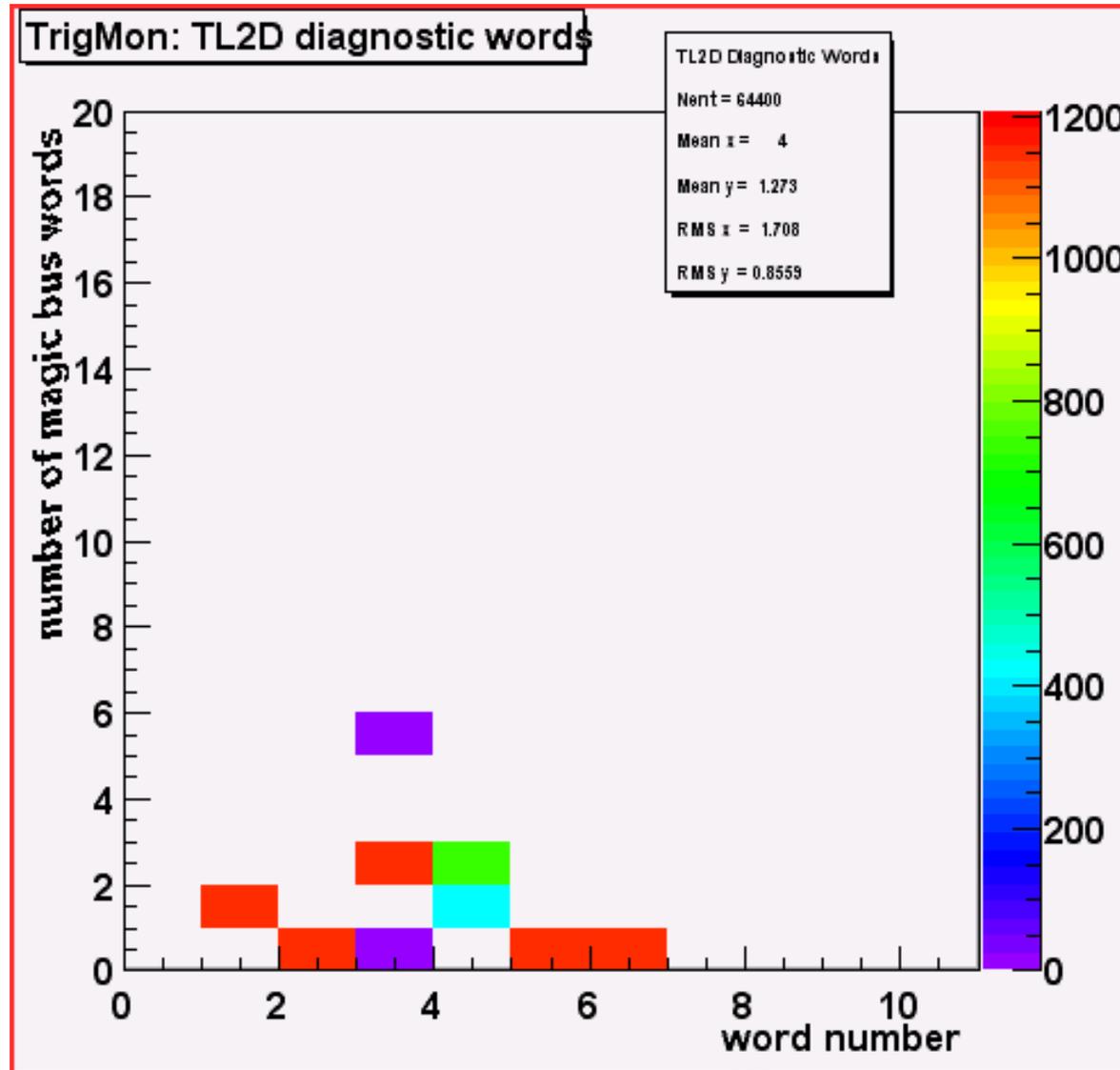
- 1 Pre-production board in b0l2de00 crate – minimum needed for running
 - 1 Production board at B0 for testing (occasionally fails due to a flaky via)
 - 3 boards at Michigan needing via debugging and repair
- Error in how data is received from the interface boards
 - Problem can be solved in software – but with 5-10us time cost
 - Fix to problem has been implemented with wires and firmware changes
 - Fix will only be applied to B0 boards when bad via Alpha boards are repaired
- Modified Alpha design to be sent out in next 2 weeks
 - 5 new boards will arrive in late summer (part of original order of boards)

- **Software**

- L2 executables created from TriggerDB
 - SumEt, MEt, Jet triggers available
 - Additional triggers being written
 - Work on making Alpha code more robust
- TrigMon, Trigsim and Offline monitoring code being developed
 - Accessors for TL2D being written



Cool TrigMon Plot





L2 Task Force

- **Goals:**
 - Provide constant level of effort for debugging L2
 - Meet each day to make a coherent debugging plan
 - Formalize what we're already doing
 - Enlist/Train more people in debugging effort
 - Help provide tools for identifying problems
 - Determine operational status of L2
 - Liaison for Ops-managers and shift crew
 - Check for errors in L2 data taken during running
 - Address operational difficulties found by the shift crew
 - Provide documentation and tools for shift crew
- **Date of Working System = Today + $\langle T_{\text{fix}} \rangle N_{\text{bugs}}$**



Tasks

- Order of Tasks
 - Bus Arbitration Problem
 - Reliable operation with L1, Track, Clist
 - Include Isolist, SVT
 - Add Reces
 - Additional Alpha boards
 - Optimized running
 - Muon board
- L2 Trigger during Collisions
 - “First, do no harm”
 - Tagging mode to verify data
 - Jet, Electron triggers
 - SVT triggers, Photons, low Et electrons
 - Full Rate at L2

Request for 3 hours of system each day (with beam if necessary)



Force

- **Personnel**

- Saltzberg, Wittich, Ristori, Kuhlmann, Tecchio, Miller, Worcester, Ray, Goldschmidt, Varganov, Byrum others
- Additional support as needed from engineers

- **Jobs**

- Crate debugging – testing new firmware, boards
- Firmware changes to interface boards
- Error handling and reporting during running
- Validation of data, Online and Offline
- Tools for error finding, debugging



Tools

- Ethernet connection for scope, LA to share pretty pictures
- Web of documentation – supplement to E-logs
- Additional TrigMon plots
- Offline data validation
- “Database” for status of crate and boards – including spares



Summary

- L2 is close to a minimal, stable system for running in tagging mode
 - Will add additional boards, triggers, cutting in steps
- L2 Task force to continue debugging effort, ensure stable operation
- L2 commissioning will require dedicated system time with beam on