

## Readout Lists - Status and Plans

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The Issue:

- We want to speed up readout by dropping some banks
- But, need the banks for a sample of events for online monitoring purposes

The Solution - Readout Lists:

- The DAQ system can support up to eight readout lists, numbered 0-7
  - Readout list for an event is determined by the L2 processor, sent to TSI
  - The DAQ uses this information to decide which banks to read out
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## Implementation

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- New TriggerDB option 'ReadOutList' which takes one parameter
- Make a specific option for each desired list, i.e. L2\_READOUTLIST\_1
- The ReadOutList specific options can be attached to any L2 trigger
- If no readout list is specified it defaults to zero
- The L2 executable will have an array of 8 readout list bitmasks
  - One bit per L2 trigger
  - Each bit will be set in only one readout list bitmask
- On L2A, Alpha will check its L2 bits against the readout list bitmasks
- Look for bits in each bitmask which match set L2 bits for the event
- The highest-number readout list is chosen in case of multiple matches

For special diagnostic runs, there will be a button in Run Control telling the DAQ to override readout lists and read everything

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## Readout List Triggers

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What sort of L2 trigger would carry a readout list specification?

- Only triggers with the appropriate readout list will be fed to TrigMon
- Want to be able to tune the rate to match what TrigMon can handle
- A L2 auto-accept will pass mostly track triggers
- Would like to get more high-occupancy events

New L2 trigger option - 'Inclusive'

- Doesn't have a specific L1 prerequisite
  - Auto-accepts a group of L1 bits rather than just one
  - Three settings: ALL, TRACK, NOTRACK
    - ALL passes if any L1 trigger fired
    - TRACK passes if a L1 track trigger fired
    - NOTRACK passes if any non-track L1 trigger fired
  - Bitmasks for each are calculated when a trigger table is made
  - Trigger is just an AND of its bitmask and the L1 bits
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## Consumers and Offline

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- Each table will have two Inclusive triggers, one TRACK and one NOTRACK
  - These will be prescaled to the desired rate and TRACK/NOTRACK fraction
    - Target rate is  $\sim 1$  Hz, but can be set anywhere we want
    - Would be a good candidate for a rate-limit prescale
  - Each will have a ReadOutList option attached, set to read everything
  - Set TrigMon to only look at events with a passed Inclusive trigger
    - Looks like this involves only a small change to the ConsumerInput talk-to
    - Selection is based on trigger name, not L2 bit
    - Not linked to a specific trigger table
  - The Inclusive triggers will be followed by L3 auto-accepts
  - Events will go to the MONITOR dataset in stream D
  - Will be easy to pick out offline using Prereq module
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## Status

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- Entire hardware chain has been successfully tested
  - Alpha in L2 crate sending to TSI
  - Initially a problem not latching values before Alpha dropped signals - fixed
  - DAQ reading from TSI, sending to crates
- Code to calculate readout list bitmasks, put into L2 exe written and tested
- Inclusive trigger code written and tested
  - Lots of problems using path with no L1 trigger

### To Do:

- Complete L2 exe which selects readout list using bitmasks
  - Configure TrigMon to monitor only Inclusive triggers
  - Configure crate software to send banks only for certain readout lists
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**Run Configuration for run [150667](#) : [L1](#) | [L2](#) | [L3](#) | [ShiftLog](#) | [ErrorLog](#) | [SessionLog](#) | [SlowControl](#) | [Offline](#)**

**Level 2 Prescale Changes for run [150667](#)**

BIT	TRIGGER_NAME	TIME	AT_EVENT	OLD_PRESCALE	NEW_PRESCALE	AUTOMATIC
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**Level 2 Triggers for run [150667](#)**

L2BIT	TRIGGER_NAME	UNPRESCALED	PRESCALED	RATE_HZ	NB
0	L2_AUTO_L1_CEM0_PT2_MINUS [1]	<a href="#">1,372</a>	<a href="#">1,372</a>	<a href="#">0.68</a>	31,181,818.18
1	L2_AUTO_L1_CEM0_PT2_PLUS [1]	<a href="#">1,424</a>	<a href="#">1,424</a>	<a href="#">0.70</a>	32,363,636.36
2	L2_AUTO_L1_CMU0_PT4 [1]	<a href="#">1,494</a>	<a href="#">1,494</a>	<a href="#">0.74</a>	33,954,545.45
3	L2_AUTO_L1_CMU1.5_PT1.5 [1]	<a href="#">2,372</a>	<a href="#">2,372</a>	<a href="#">1.17</a>	53,909,090.91
4	L2_AUTO_L1_MB_XING [1]	<a href="#">3,483</a>	<a href="#">3,483</a>	<a href="#">1.72</a>	79,159,090.91
5	L2_AUTO_L1_PJET2 [1]	<a href="#">0</a>	<a href="#">0</a>	<a href="#">0.00</a>	0.00
6	L2_AUTO_L1_SEVEN_TRK1.5 [1]	<a href="#">1</a>	<a href="#">1</a>	<a href="#">0.00</a>	22,727.27
7	L2_AUTO_L1_TAU0_PT4 [1]	<a href="#">1,494</a>	<a href="#">1,494</a>	<a href="#">0.74</a>	33,954,545.45
8	L2_AUTO_L1_TAU0_PT8 [1]	<a href="#">873</a>	<a href="#">873</a>	<a href="#">0.43</a>	19,840,909.09
9	L2_AUTO_L1_TRK1.5 [1]	<a href="#">2,372</a>	<a href="#">2,372</a>	<a href="#">1.17</a>	53,909,090.91
10	L2_AUTO_L1_TRK2 [1]	<a href="#">2,158</a>	<a href="#">2,158</a>	<a href="#">1.06</a>	49,045,454.55
11	L2_AUTO_L1_TRK4 [1]	<a href="#">1,493</a>	<a href="#">1,493</a>	<a href="#">0.74</a>	33,931,818.18
12	L2_AUTO_L1_TRK8 [1]	<a href="#">872</a>	<a href="#">872</a>	<a href="#">0.43</a>	19,818,181.82
13	L2_AUTO_L1_TWO_CMU1.5_DPHI120_&_TWO_CJET0.5 [1]	<a href="#">3</a>	<a href="#">3</a>	<a href="#">0.00</a>	68,181.82
14	L2_AUTO_L1_TWO_JET1.5 [1]	<a href="#">43,534</a>	<a href="#">43,534</a>	<a href="#">21.45</a>	989,409,090.91
15	L2_INCLUSIVE_NOTRACK_PS10_ROL1 [1]	<a href="#">49,102</a>	<a href="#">4,910</a>	<a href="#">2.42</a>	111,590,909.09
16	L2_INCLUSIVE_TRACK_PS10_ROL1 [1]	<a href="#">2,372</a>	<a href="#">237</a>	<a href="#">0.12</a>	5,386,363.64