

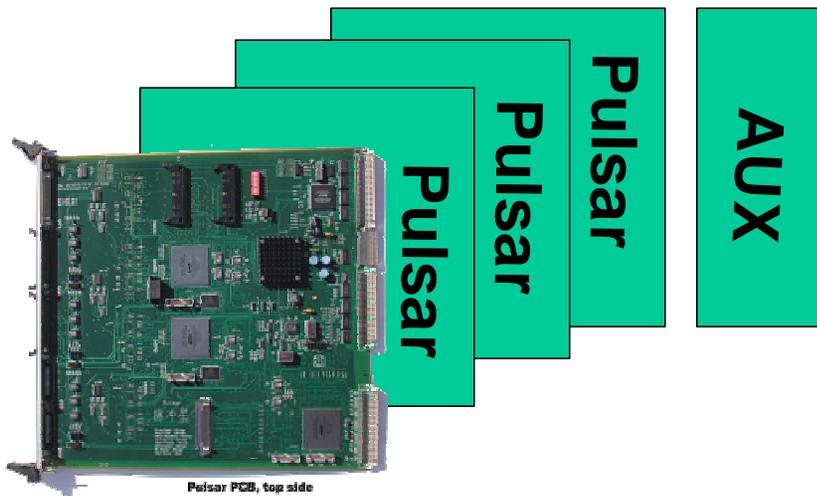
Pulsar Hardware Status

May, 16th 2003

Burkard Reisert (FNAL)

From parts ...

... to system



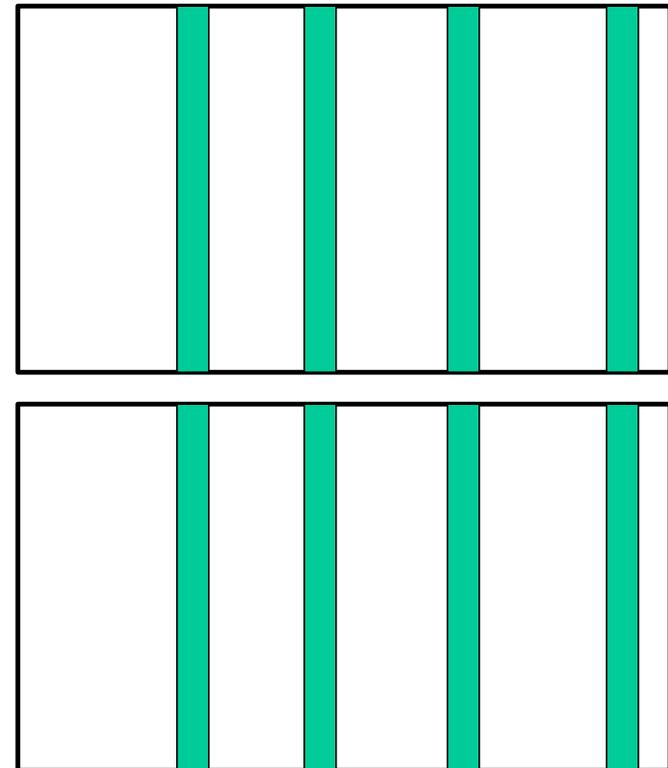
Hotlink



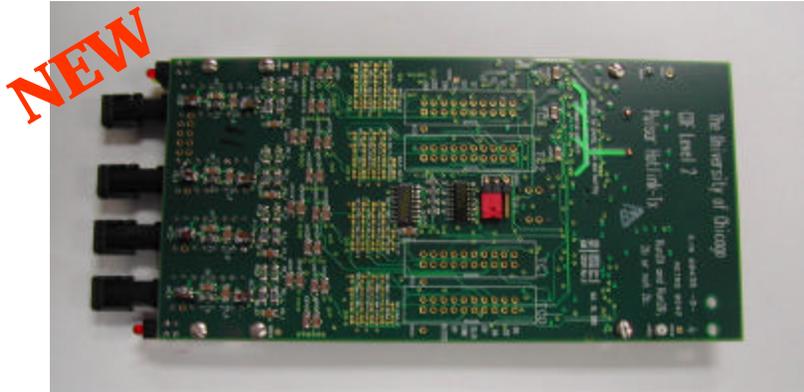
HotLVDS



Taxi



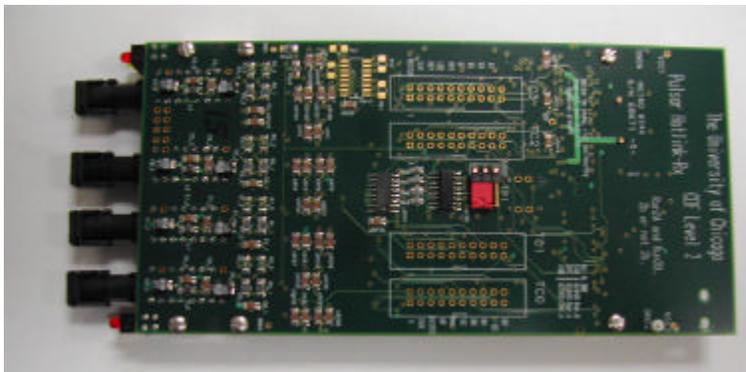
Hotlink Fiber mezzanine cards



Transmitter:

4 prototype cards UC
12 production FNAL

DONE



Receiver:

4 prototype cards UC
12 production FNAL

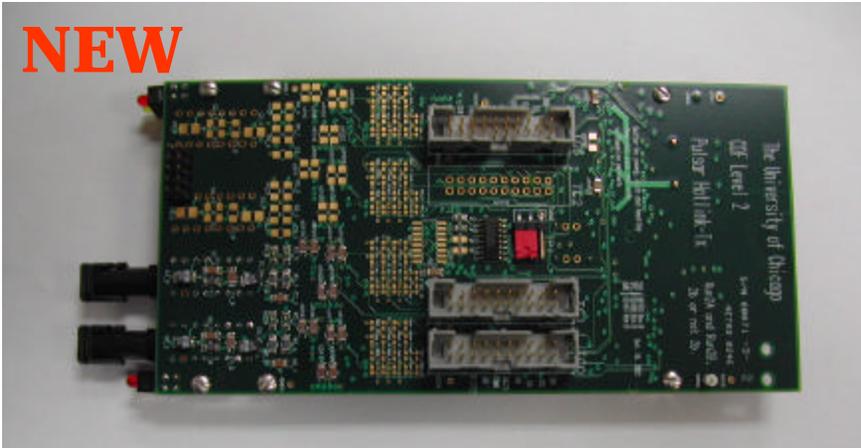
DONE

NEW: wrt last bi-monthly meeting

**Production completed,
Tests 10E7 events**

bi-weekly April 11th :

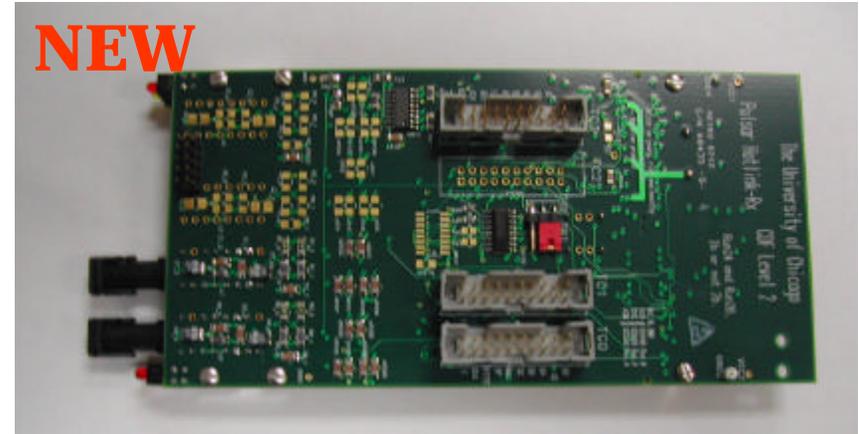
Hotlink Fiber & LVDS mezzanine cards



Transmitter:

2 prototype cards FNAL

- same PCB, different components
- adapt hotlink firmware
- fully tested



Receiver:

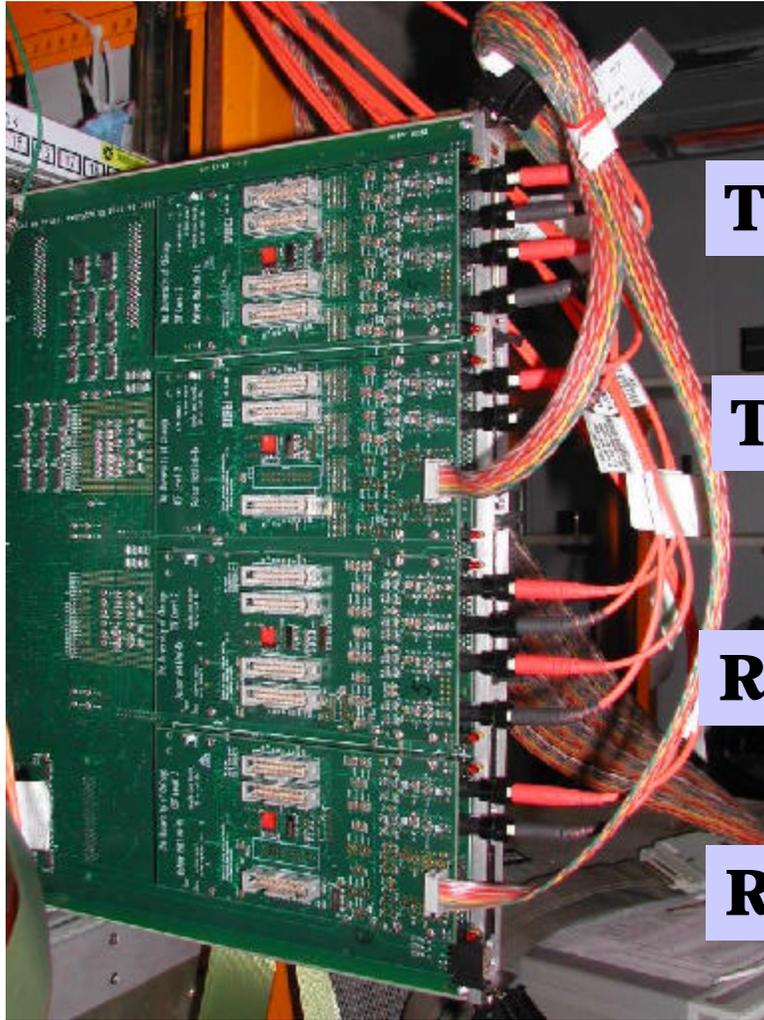
2 prototype cards FNAL

Ready to produce 3 more pairs

**Production completed,
Tests 10E7 events**

NEW

Hotlink Fiber & LVDS Pulsar board

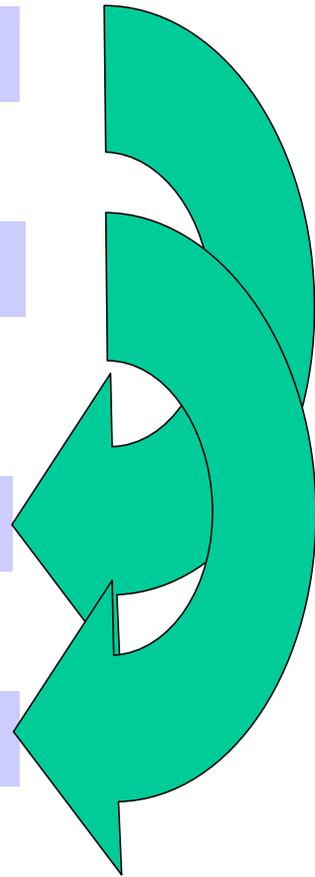


Tx Fiber

Tx LVDS

Rx Fiber

Rx LVDS



Hardware
for

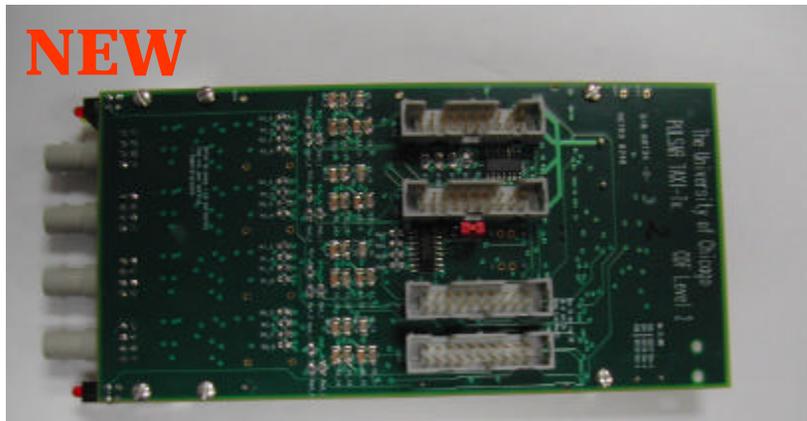
CLIST
Data path

bi-weekly April 11th :

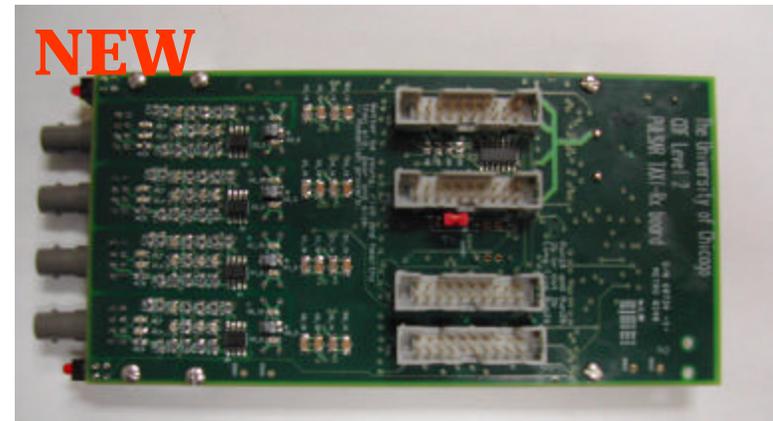
Taxi mezzanine cards

2 Tx prototypes UC

2 Rx prototypes UC



2+5 from prototype batch:
Fully tested



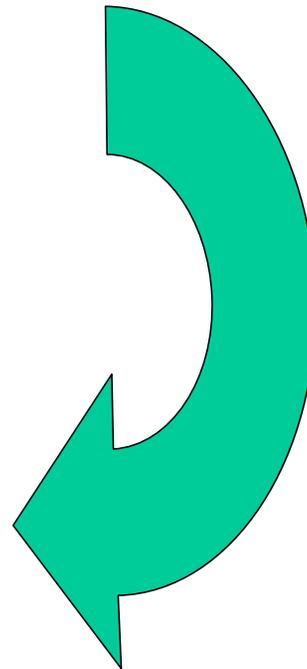
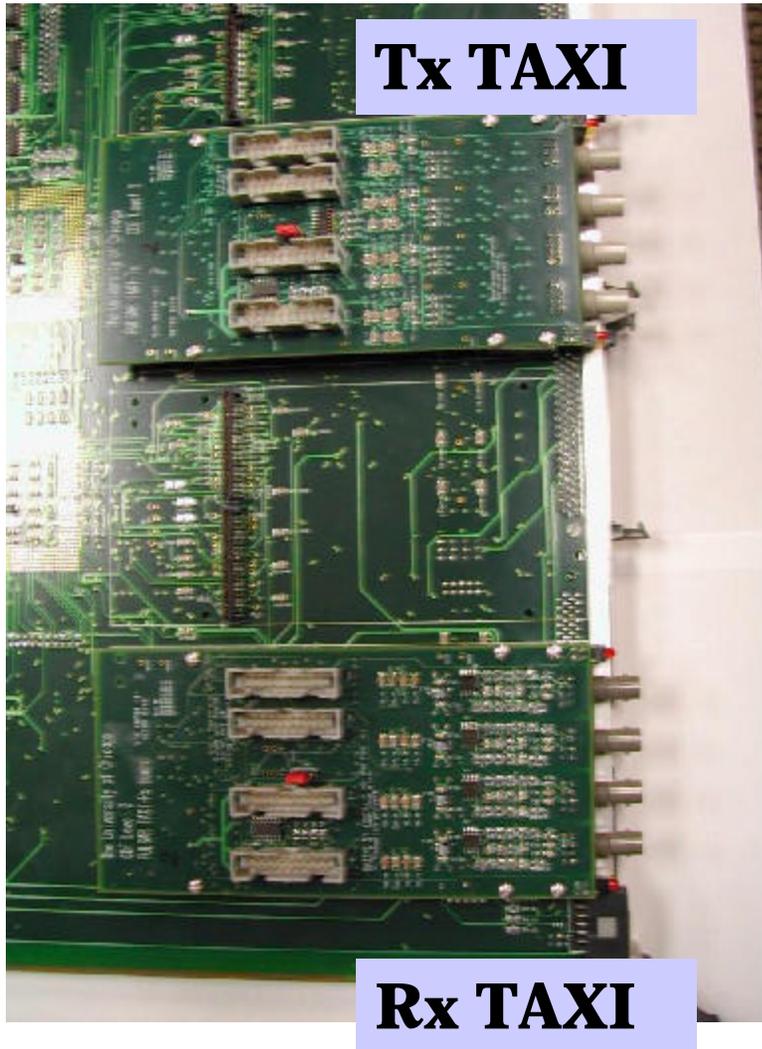
2+5 from prototype batch:
Tests ongoing

Adopt Hotlink fiber Firmware Cards fully test
→ Ready for production

Order PCB and components for production

Order is out

TAXI Tx Rx Pulsar board



Hardware
For

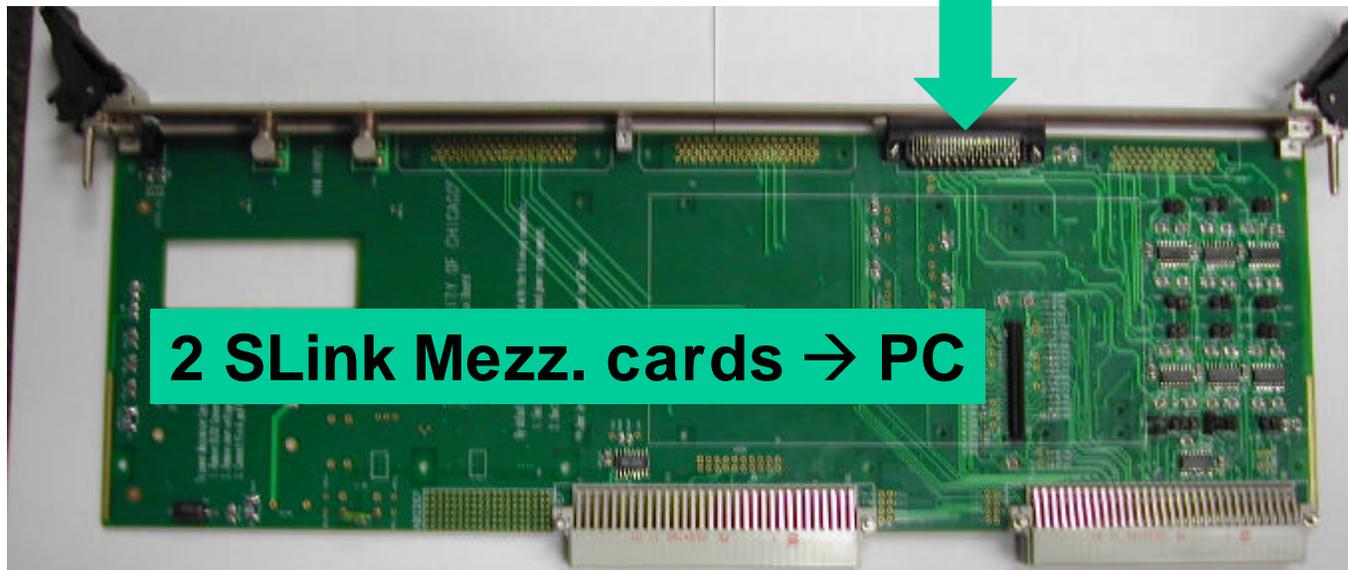
ISOLIST
&
RECES

Prototype AUX Cards

5 V version

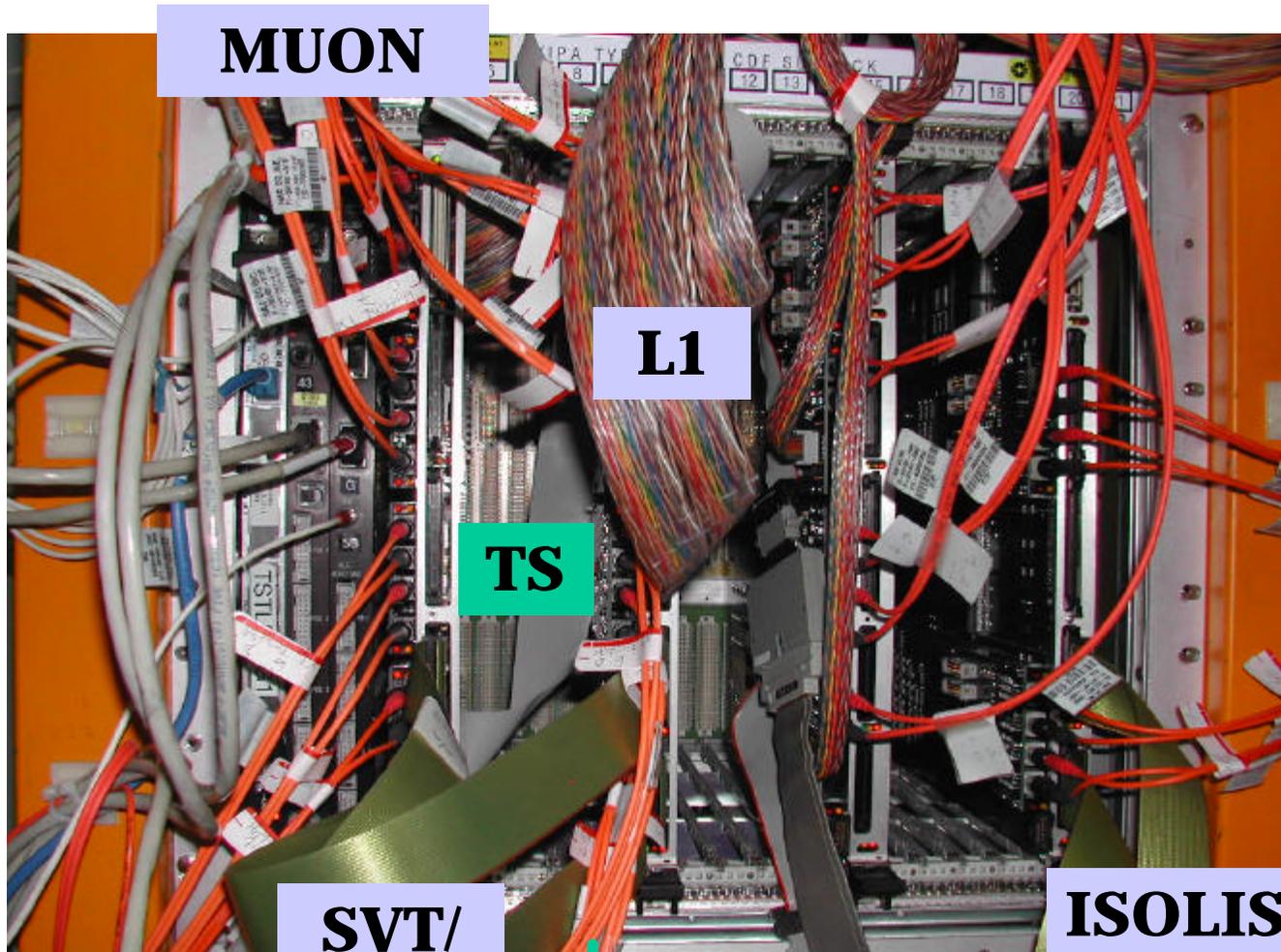
SVT/XTRP input

Fully tested



Other options: -- 3.3 V version
-- SVT/XTRP output
-- 2 TS connectors

PULSAR TEST STAND



MUON

L1

TS

**SVT/
XTRP**

CLIST

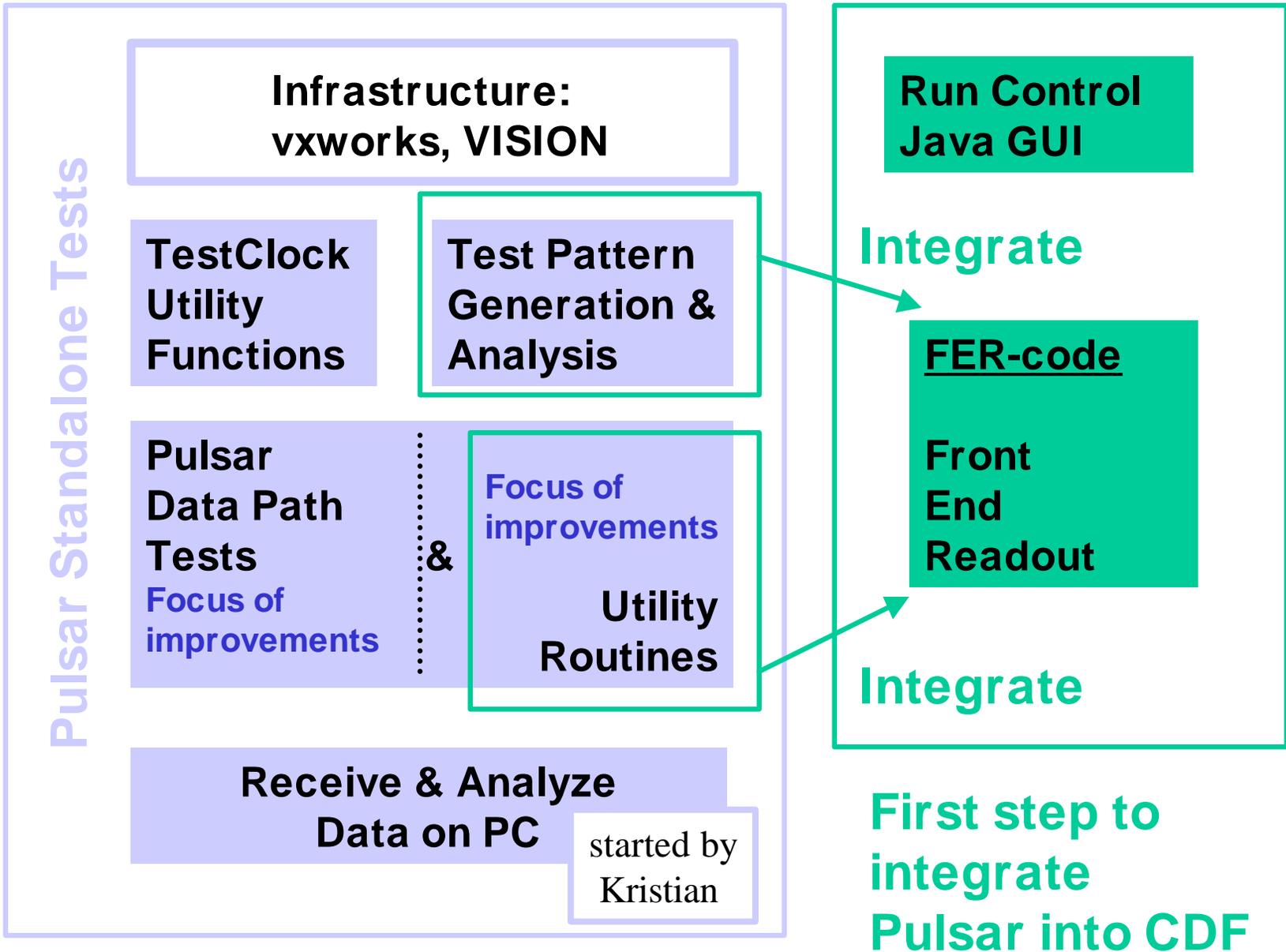
**ISOLIST/
RECES
v0.5**

PC ← AUX

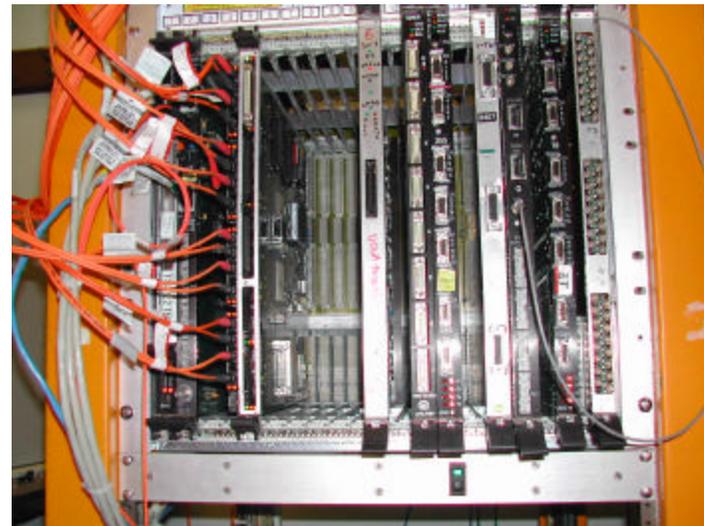
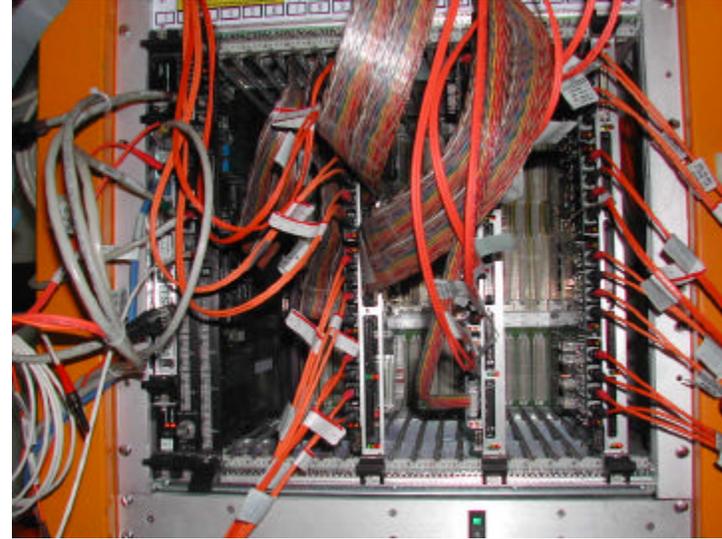
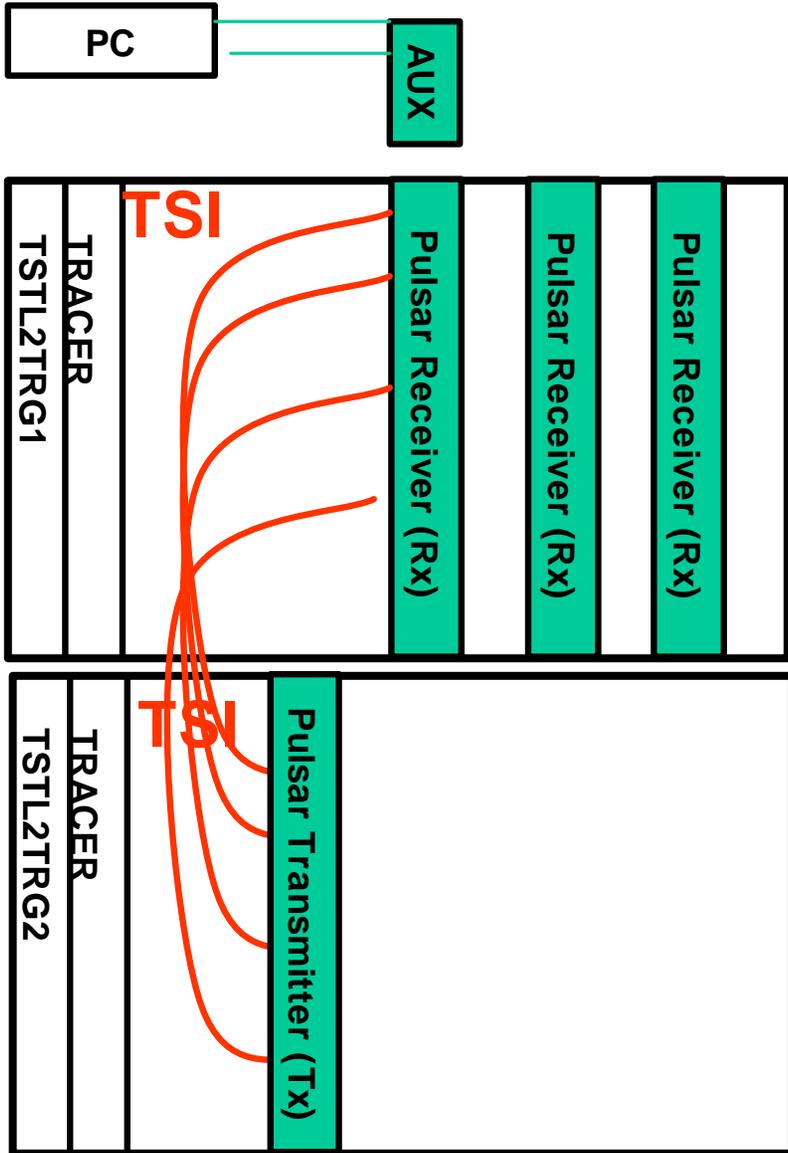
- Hardware/
Firmware for
all data paths
- Ready to
fully test
new Pulsars

Software

Structure as presented Jan. 30th :

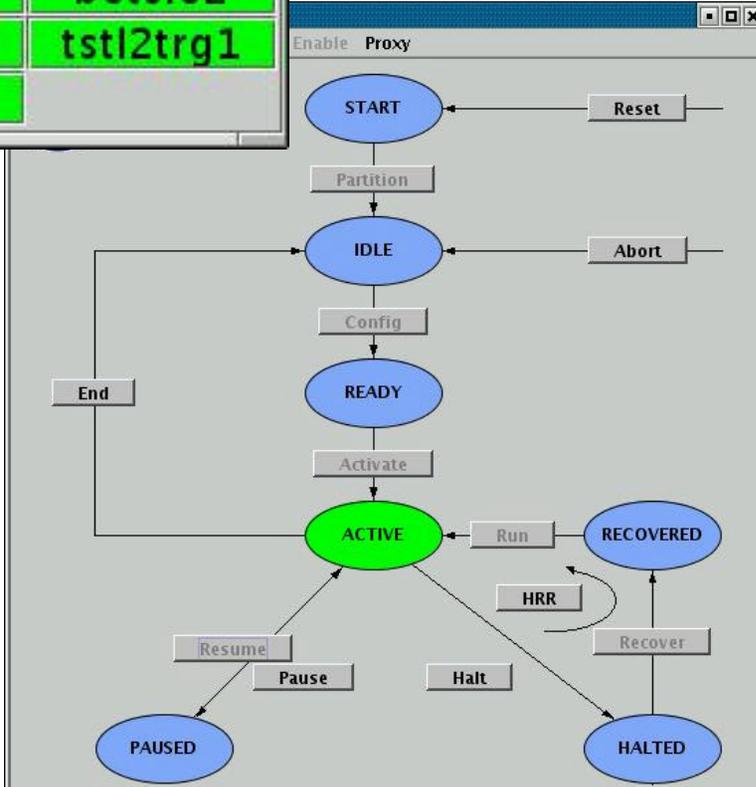


Pulsar Test Stand using 2 crates



Run Control

Partition 5:	b0tsi00
b0tsi01	b0tsi02
slow	tst12trg1
tst12trg2	



DAQ StateManager

RunControlStatus

State: ACTIVE
 Partition: 5
 ACTIVE
 No error conditions
 Activate: 2003.05.15 13:48:18
 TS Status: OK
 RunType: Physics
 TriggerType: null [0,0,0]

Transition: (none)
 Run: 2
 705 Events (L2A)
 705 Calib Events
 No Events (L3A) yet
 ● Clock ● Error ● SIL1TO ● L2TO
 Data Type: DAQ Testing

14:07:18 SVX ISL COT CMU CLC LOO

```

tst12trg1
OUTPUT on tst12trg1
startScanReg: -1593769984
L2Addr: 0
tsRL: 0
evtID: 10
Rx crate
Generated TestPattern 1
90000001 91111111 92222221 93333331 94444441 95555551 96666661 97777771
98888881 99999991 9aaaaaa1 9bbbbbb1 9ccccc1 9ddddd1 9eeeeee1 9ffffff1
Generated TestPattern 2
90000002 91111112 92222222 93333332 94444442 95555552 96666662 97777772
98888882 99999992 9aaaaaa2 9bbbbbb2 9ccccc2 9ddddd2 9eeeeee2 9ffffff2
Generated TestPattern 3
90000003 91111113 92222223 93333333 94444443 95555553 96666663 97777773
98888883 99999993 9aaaaaa3 9bbbbbb3 9ccccc3 9ddddd3 9eeeeee3 9ffffff3
Generated TestPattern 4
90000004 91111114 92222224 93333334 94444444 95555554 96666664 97777774
98888884 99999994 9aaaaaa4 9bbbbbb4 9ccccc4 9ddddd4 9eeeeee4 9ffffff4
RX Data10 FPGA1 Mezz1 INPUT FIFO
8fffffff1 90000001 90000001 91111111 92222221 93333331 94444441 95555551
96666661 97777771 98888881 99999991 9aaaaaa1 9bbbbbb1 9ccccc1 9ddddd1
9eeeeee1 9ffffff1 eeeeeeee eeeeeeee eeeeeeee eeeeeeee eeeeeeee eeeeeeee
RX Data10 FPGA1 Mezz2 INPUT FIFO
8fffffff2 90000002 90000002 91111112 92222222 93333332 94444442 95555552
96666662 97777772 98888882 99999992 9aaaaaa2 9bbbbbb2 9ccccc2 9ddddd2
9eeeeee2 9ffffff2 eeeeeeee eeeeeeee eeeeeeee eeeeeeee eeeeeeee eeeeeeee
RX Data10 FPGA2 Mezz1 INPUT FIFO
8fffffff3 90000003 90000003 91111113 92222223 93333333 94444443 95555553
96666663 97777773 98888883 99999993 9aaaaaa3 9bbbbbb3 9ccccc3 9ddddd3
9eeeeee3 9ffffff3 eeeeeeee eeeeeeee eeeeeeee eeeeeeee eeeeeeee eeeeeeee
RX Data10 FPGA2 Mezz2 INPUT FIFO
8fffffff4 90000004 90000004 91111114 92222224 93333334 94444444 95555554
96666664 97777774 98888884 99999994 9aaaaaa4 9bbbbbb4 9ccccc4 9ddddd4
9eeeeee4 9ffffff4 eeeeeeee eeeeeeee eeeeeeee eeeeeeee eeeeeeee eeeeeeee
BR FER_readout2 is in loop 770
Messenger: processStatechange Pause [0]
BR FER_readout2 is in loop 771
Sent ack to Run Control: 5 PAUSED SUCCESS
  
```

```

tst12trg2
OUTPUT on tst12trg2
startScanReg: -1593769984
L2Addr: 0
tsRL: 0
evtID: 10
Tx crate
TX TestPattern 1
a0000001 a1111111 a2222221 a3333331 a4444441 a5555551 a6666661 a7777771
a8888881 a9999991 aaaaaaa1 abbbbbb1 accccc1 addddd1 aeeeeee1 affffff1
TX TestPattern 2
a0000002 a1111112 a2222222 a3333332 a4444442 a5555552 a6666662 a7777772
a8888882 a9999992 aaaaaaa2 abbbbbb2 accccc2 addddd2 aeeeeee2 affffff2
TX TestPattern 3
a0000003 a1111113 a2222223 a3333333 a4444443 a5555553 a6666663 a7777773
a8888883 a9999993 aaaaaaa3 abbbbbb3 accccc3 addddd3 aeeeeee3 affffff3
TX TestPattern 4
a0000004 a1111114 a2222224 a3333334 a4444444 a5555554 a6666664 a7777774
a8888884 a9999994 aaaaaaa4 abbbbbb4 accccc4 addddd4 aeeeeee4 affffff4
BR FER_readout2 is in loop 770
Messenger: processStatechange Pause [0]
BR FER_readout2 is in loop 771
Sent ack to Run Control: 5 PAUSED SUCCESS
  
```

E1: near term goals from last meetings

- (1) **Feb:** have the automated testing procedure fully working for 16 hotlink channels (muon path): Tx->Rx->PC; **DONE**
- (2) **March:** finish testing 2 more Pulsar boards with hotlink/Taxi mezzanine cards and AUX cards; **DONE**

- (3) **April:** initial proof of principle test with S32PCI64 with test setup
intensify communication with UPenn

HARDWARE:

- End of Prototype Phase, all types of boards tested, no blue wires! ←
- (4) **May:** core firmware (Tx/Rx) fully developed and tested with hotlink/taxi mezzanine cards; → see talk of Sakari
“Poor man’s readout” running **Summer Shutdown**
 - (5) **June:** production/testing of Pulsar/hotlink/taxi/AUX cards
TAXI waiting for components **Use Pulsar**
Hotlink Rx/Tx Fiber/LVDS **As**
 - (6) **July:** have Tx->Rx→PC fully developed for Reces(taxi), cluster/Isolation (hotlink/taxi); **Teststand**
 - (7) **Aug:** document (Sakari’s thesis) everything: cdf note **Tools**

Goals for the coming months

June/July:

- integrate new Finnish Students (VISA okay now)
- continue improving Pulsar core firmware
- production & testing of TAXI mezzanine cards
- test four new Pulsars

- **Prepare for Summer Shutdown (Mid/End August?)**
 - fully develop firmware/software for Tx for ALL data paths:
 - **Firmware and Software for Rx: DAQ readout**

Time to make Pulsar useful