



University of
MICHIGAN



L2 Muon Interface Board Progress Report

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http://www-personal.engin.umich.edu/~mrniell/L2_progress/L2_progress.html

7/26/02

Overview

- **Receives data from Matchbox and Prematch cards via 16 HOTLink fiber inputs**
 - **Matchbox (12) 30 degree azimuth (CMU/CMX/CSX/IMU)**
 - **Prematch (4) 1 wall CMP/CSP**
- **Sends data to L2 processor over Magic Bus**
 - **Waits for Alpha to request or runs in "data push" mode**
 - **On request, data sent on MB**
 - **In push mode, muons are identified in FPGA, sent over MB before next event**

Path from L1 Trigger

- **Matchboxes and Prematches transmit concurrently over fiber on L1 accept.**
- **Data Phasing chipsets align data to CDF_CLOCK**
- **Data enters 1 of 4 event buffers contained in Xilinx Virtex series FPGAs (Buffer-type FPGAs)**
 - **grouped in 120 bit words**
- **Flag Bits computed and sent out over Magic Bus**
- **Data are fed out in parallel over Magic Bus**

Buffer FPGA Mezzanine

- **Function**
 - **receives/arranges/stores data arranged by subdetector**
 - **presents data bits grouped by azimuthal wedge**
- **Large design**
 - **Four 16 x 120 bit ram structures per device**
 - **Flag bit generation logic**
 - **Address reading and output mux-ing for ram buffers**
- **Virtex series Xilinx FPGA**
 - **XCV150-4PBGA352-I**
 - **352 pin ball grid array , favorable I/O characteristics**
 - **Two HOTLinks per FPGA, 8 buffer FPGAs on board**

MB Controller Mezzanine

- **Both Magic Bus Master and Slave**
 - **Mezzanine shipped 7/12**
 - **Boards stuffed**
- **Virtex II series FPGA**
 - **XCV600E-8FG680C**
 - **Verilog firmware, Tom**
 - **Built in 128 frame logic analyzer on JTAG**
- **Bridge to VME**
 - **Initial testing will include only VME transfers and reads**
Tom

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L2 Muon Board

- **General characteristics**
 - **9U Board with 9 mezzanine boards for FPGA mounting**
 - **FPGAs reside on swap-able mezzanine cards**
 - **16 HOTLink connectors**
 - **Two hex displays, 20 status LEDs**
 - **VME interface for reading out, debugging etc.**
 - **Minimal descreet logic on board**
 - **2.5V on board**
- **Board shipped 5/6/02, Assembled 5/20 (parts delays)**
 - **Approx 11 man-hours hand assembly**

Buffer FPGA Mezzanine cards

- **Mezzanine cards designed and sent out for manufacture**
 - **Assembled enough mezzanine cards to test entire board**
 - **Programmed with simple pattern generating code**
- **Each Mezzanine card has JTAG and Slave serial capability**
 - **Easier testing and verifying**
- **Cannot test with rest of board until MB Controller finished**

MB Controller mezzanine

- **Continued development of MB Interface FPGA firmware**
 - **VME state machine blocks written**
 - **MB state machine blocks written**
 - **Main operation state machine under development**
- **Boards finished, tested without finished firmware**
 - **Hardware done**
- **Mezzanine makes own 1.8V, tested OK**
- **Simple firmware loads**

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What remains?

- **Firmware, software**
 - **MB controller firmware**
 - **VME panel software (muon test card 0th order)**
- **Debugging**
 - **running in variuos configurations**
- **Tools needed (all are readily available)**
 - **FNAL:**
 - **matchboxes, muon test card (E. James)**
 - **UM:**
 - **Kludge test clock, development Alphas, crate controllers**
 - **L2 test crate**

Time Scale

- **Goals**
 - **Week of August 2**
 - **make board talk on VME, read HL data**
 - **Week of August 9**
 - **VME/MB studies, simple arbitration state machine**
 - **Week of August 16**
 - **Firmware work, MB transfers**
 - **Week of August 23**
 - **Latency tests**
 - **Week of August 30**
 - **Firmware development**
 - **September**
 - **Work in B0 test-crate with early version firmware by end of September (my personal deadline)**

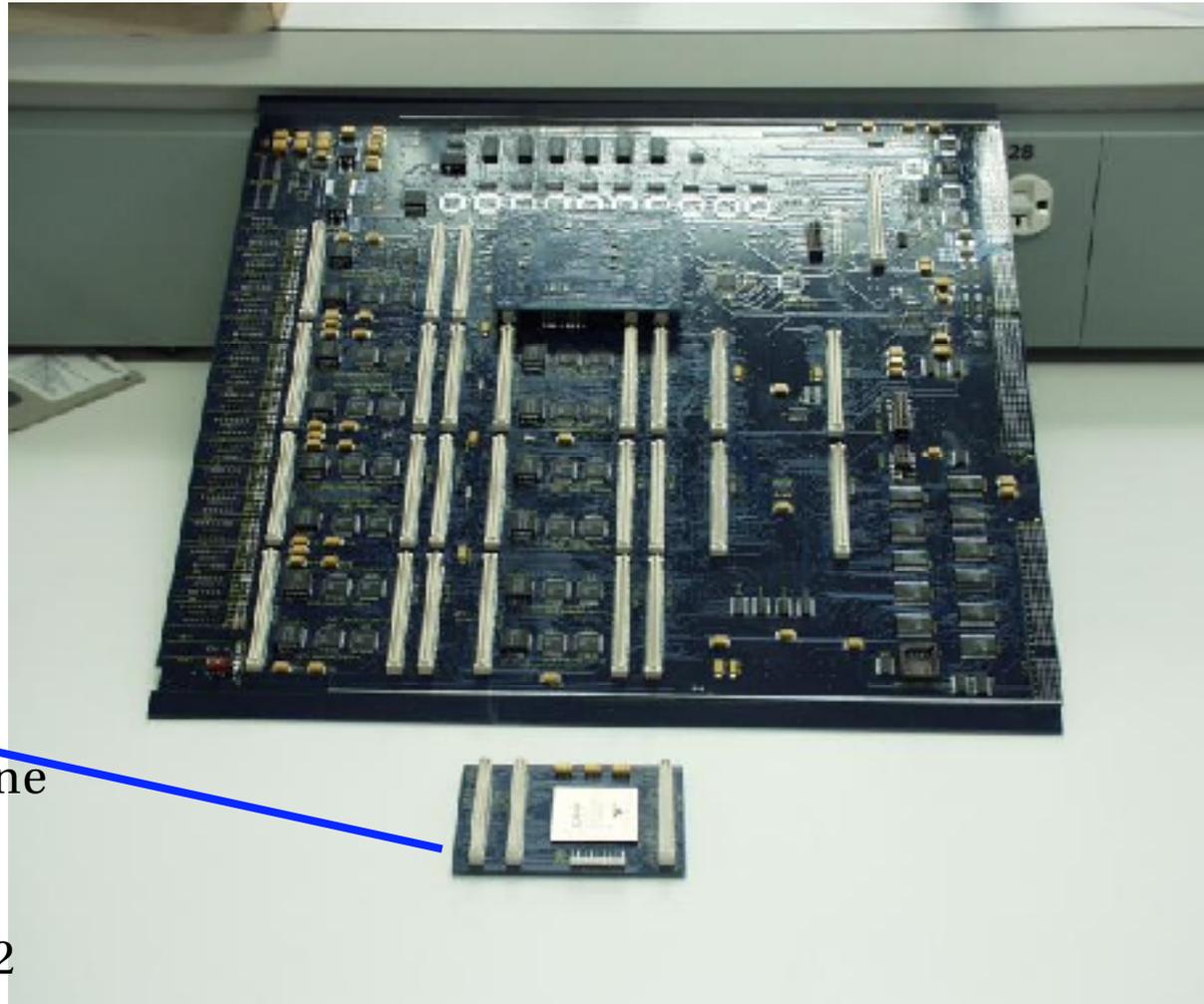
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Debugging plans

- **VME talking**
 - **simple register readout, write**
 - **data in on VME, out on VME**
- **HL configuration**
 - **DP ASIC must be initialized (shift register)**
- **Muon test card (4 fibers only)**
 - **data in on fiber, out on VME**
 - **write easy pattern, loop, read on VME**
 - **write hard pattern (dead time)**
 - **data in on fiber, out on MB**
- **Several muon test cards or Pulsar**
- **Matchbox cards & muon test cards**
 - **Work together**
- **B0**

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During assembly



Buffer
Mezzanine

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Finished 9U assembly

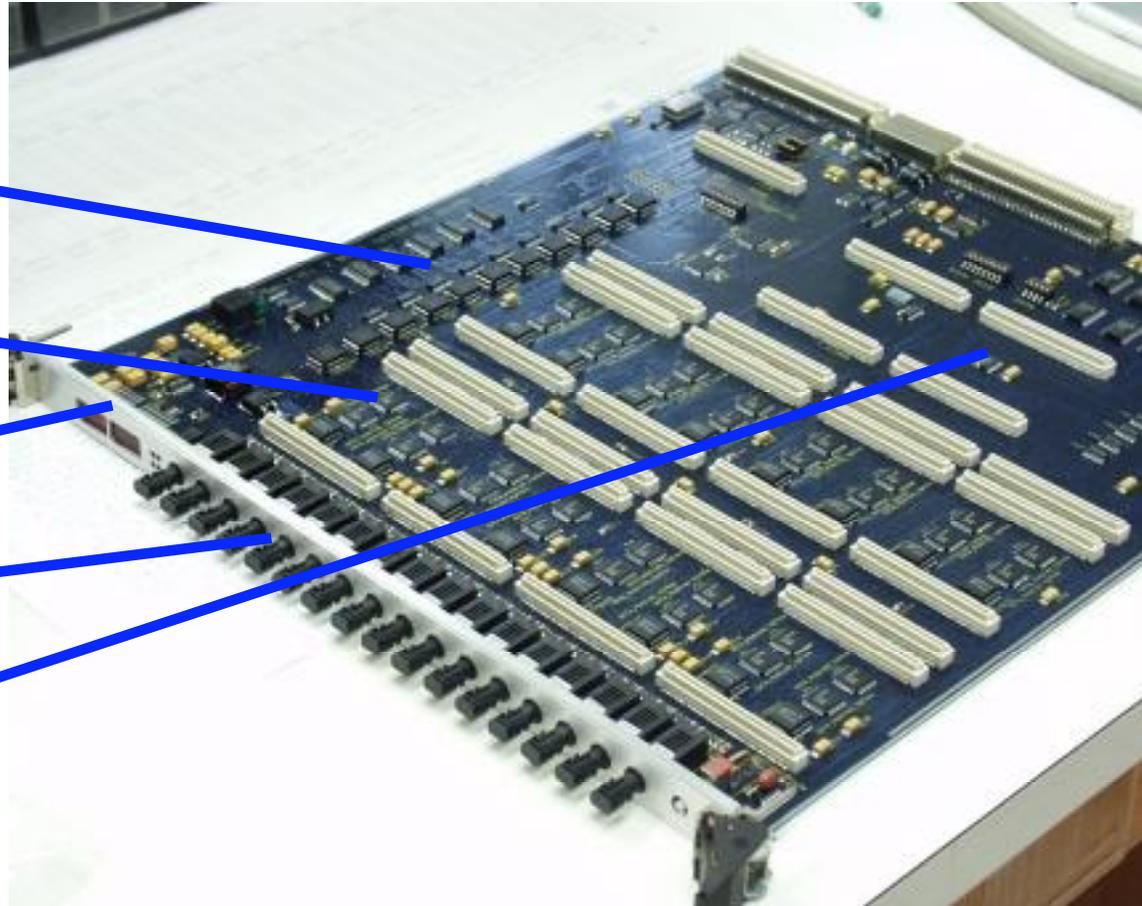
Clock generators

Buffer Mezzanine

Hex Displays

HL Fiber inputs

MB Controller
mezzanine



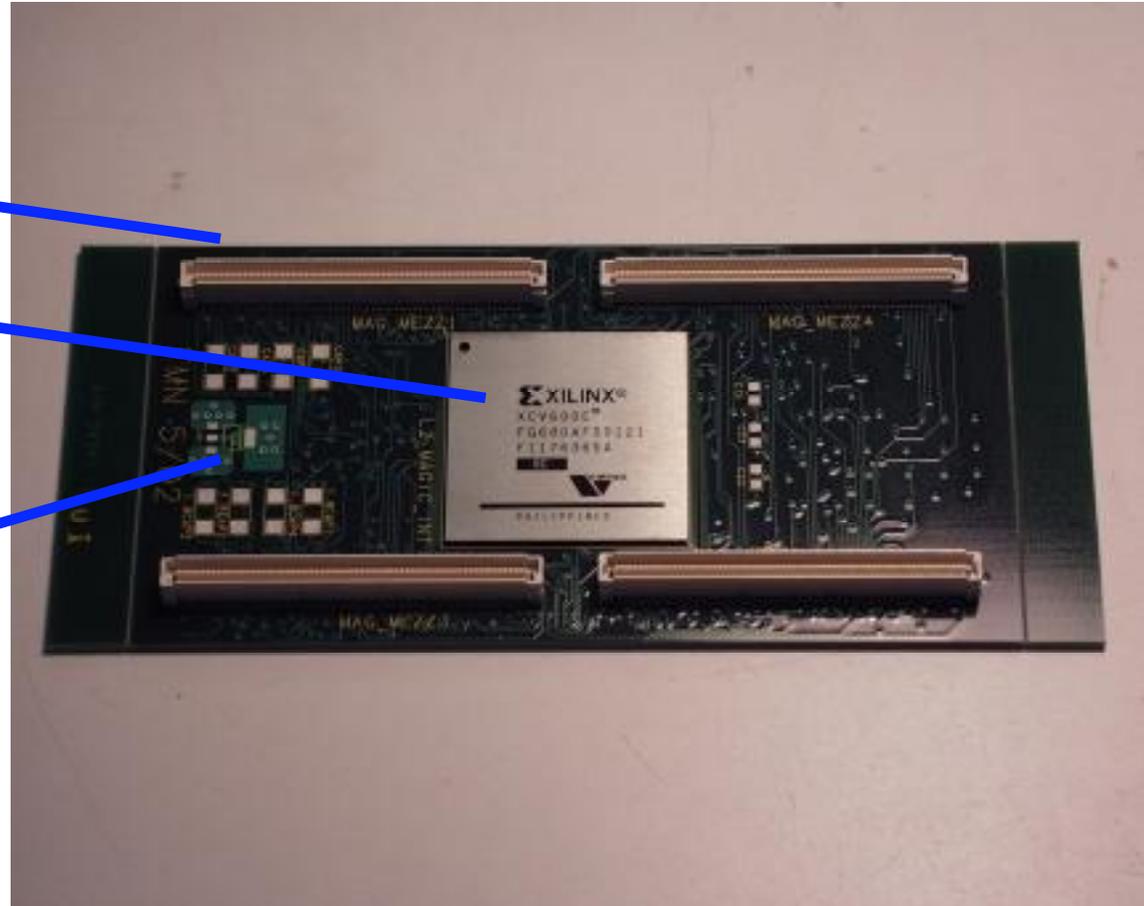
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MB Controller Mezzanine

140 Pin headers

XCV600E-8FG680C

1.8V regulator



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Process Oven

IR Oven

Test Board

TC gauge amp

Stripchart recorder

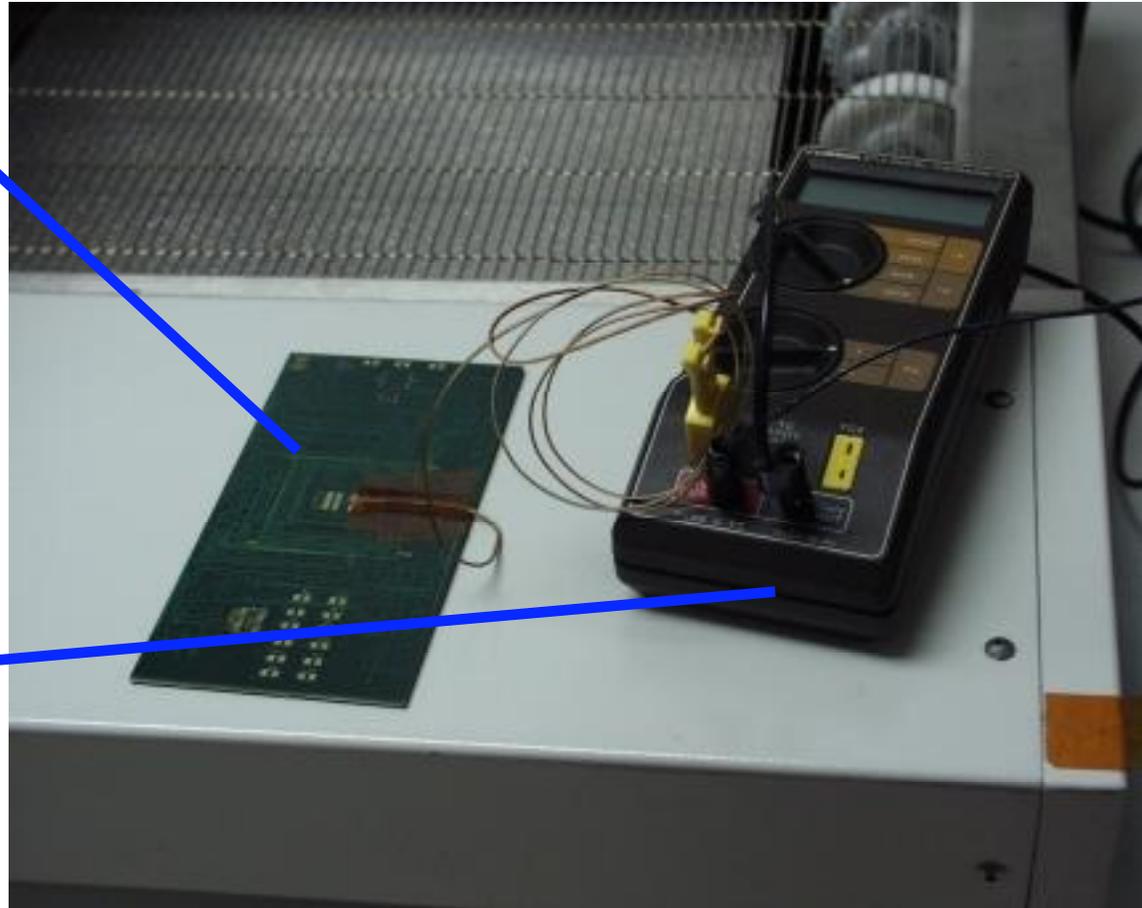


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Test Board

Test Mezzanine
board with TC
imbedded

TC gauge amp

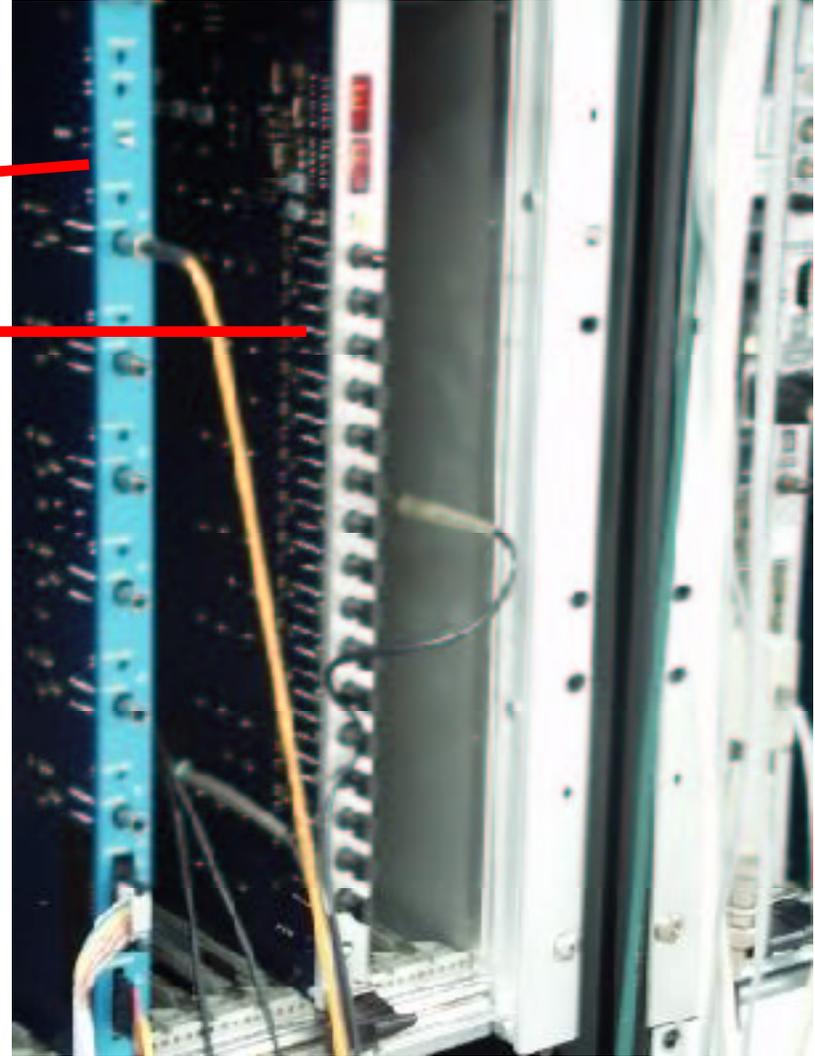


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Michigan Test Stand

CList

MuonBoard



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