TOTRIB hardware implementation.

Please see CDF note 5724 for details.

The board contains three coincidence units, which receive the E_I_MIP_J, W_I_MIP_J, E_I_HIP_J, W_I_HIP_J signals from ADMEMs. Each Coincidence unit searches for coincidences in the input signals on every clock cycle, and reports them to the outputs. The delay of these outputs is programmable via VME interface. The delayed coincidence outputs are supplied to the backplane connector and to the I_MIP_J, I_HIP_J connectors.

Each Coincidence unit calculates also the number of MIP coincidences on each clock cycle (partial MIP sum). To compute the total number of MIP coincidences, two units on the sides send their partial MIP sums to the unit in the middle, which adds these two numbers to its own partial MIP sum, and reports the total number to MIP_SUM output connector on the front panel.

CDF_CLK signal is delayed before being sent to the backplane output connector. The delay is programmable via VME with the step of ~5 ns, and the total delay can be from 5 to about 160 ns.

CDF_B0, CDF_RECOVER and CDF_HALT signals are processed as described in CDF note 5724 and sent to the backplane connector.

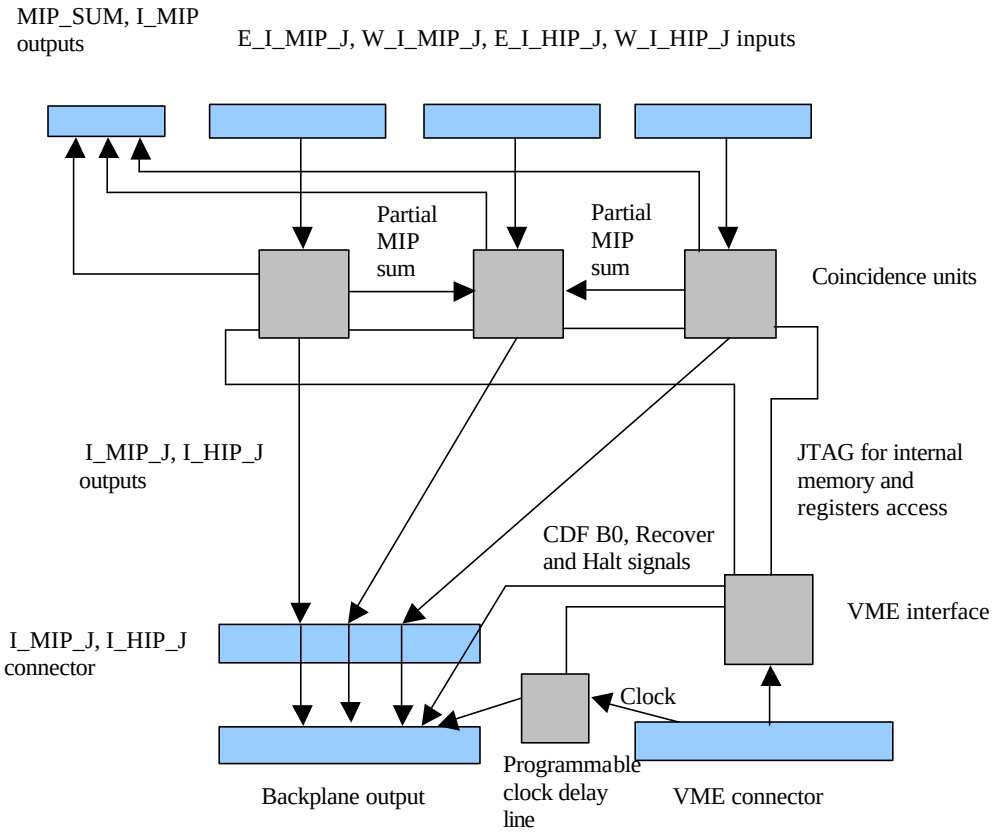
The coincidence units are planned to have the input and output FIFOs accessible from VME, to simplify the self-testing and in-system testing.

Note: since some of the corrections to the CDF note 5724 were done very recently, some parts of the schematics do not show the correct implementation yet. These parts are:

- MIP_SUM output connector
- I_MIP output connector

The schematics will be corrected very soon to reflect these changes.
The board routing is underway. To the moment of writing this note, about 70% is routed.

- Block schematics of the TOTRIB. Please see CDF note 5724 for details.



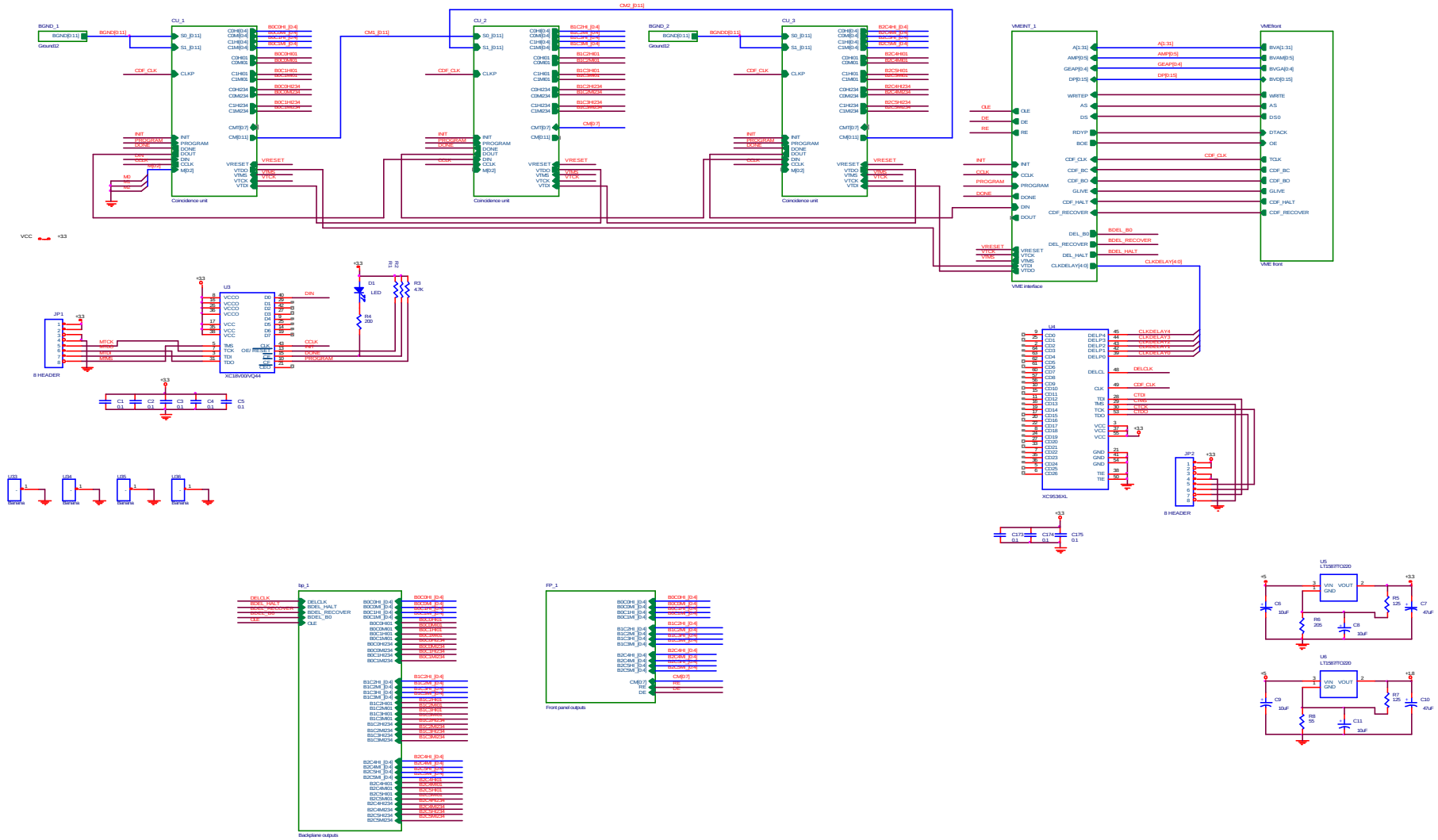


Figure 1. Root schematics

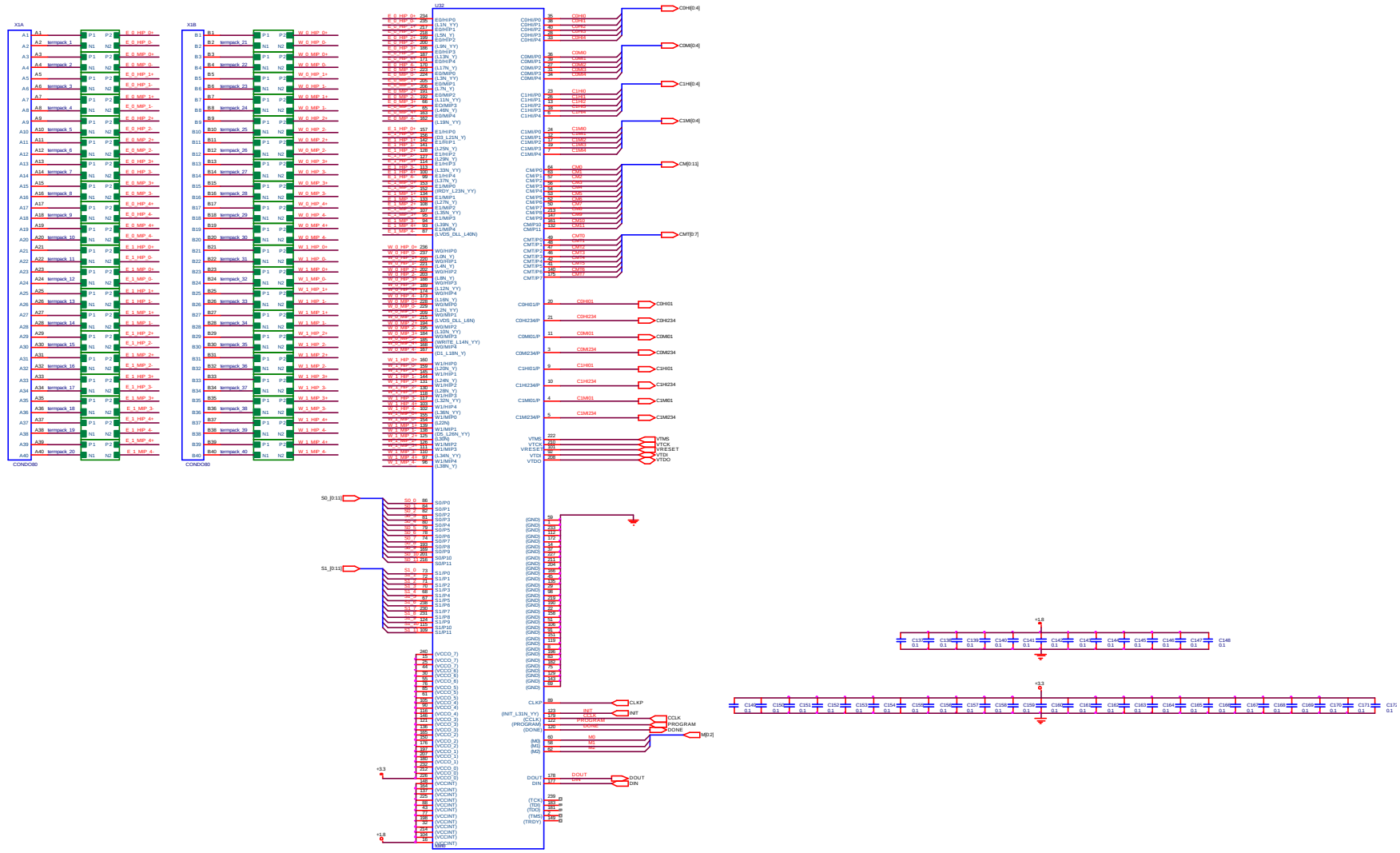
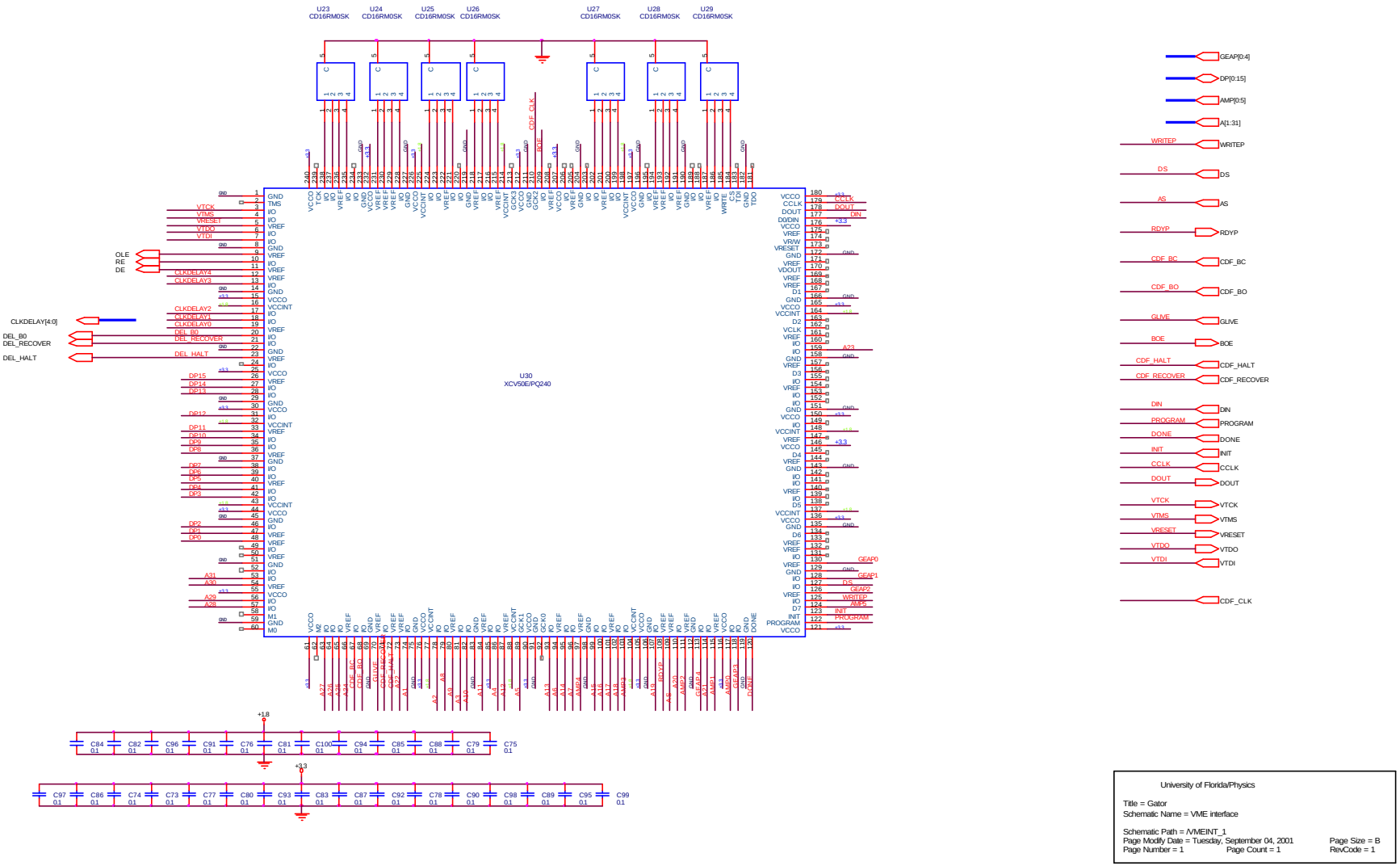


Figure 2. Coincidence unit



University of Florida/Physics

Title = Gator
Schematic Name = VME interface

Schematic Path = /VMEINT_1
Page Modify Date = Tuesday, September 04, 2001 Page Size = B
Page Number = 1 Page Count = 1 RevCode = 1

Figure 3. VME interface

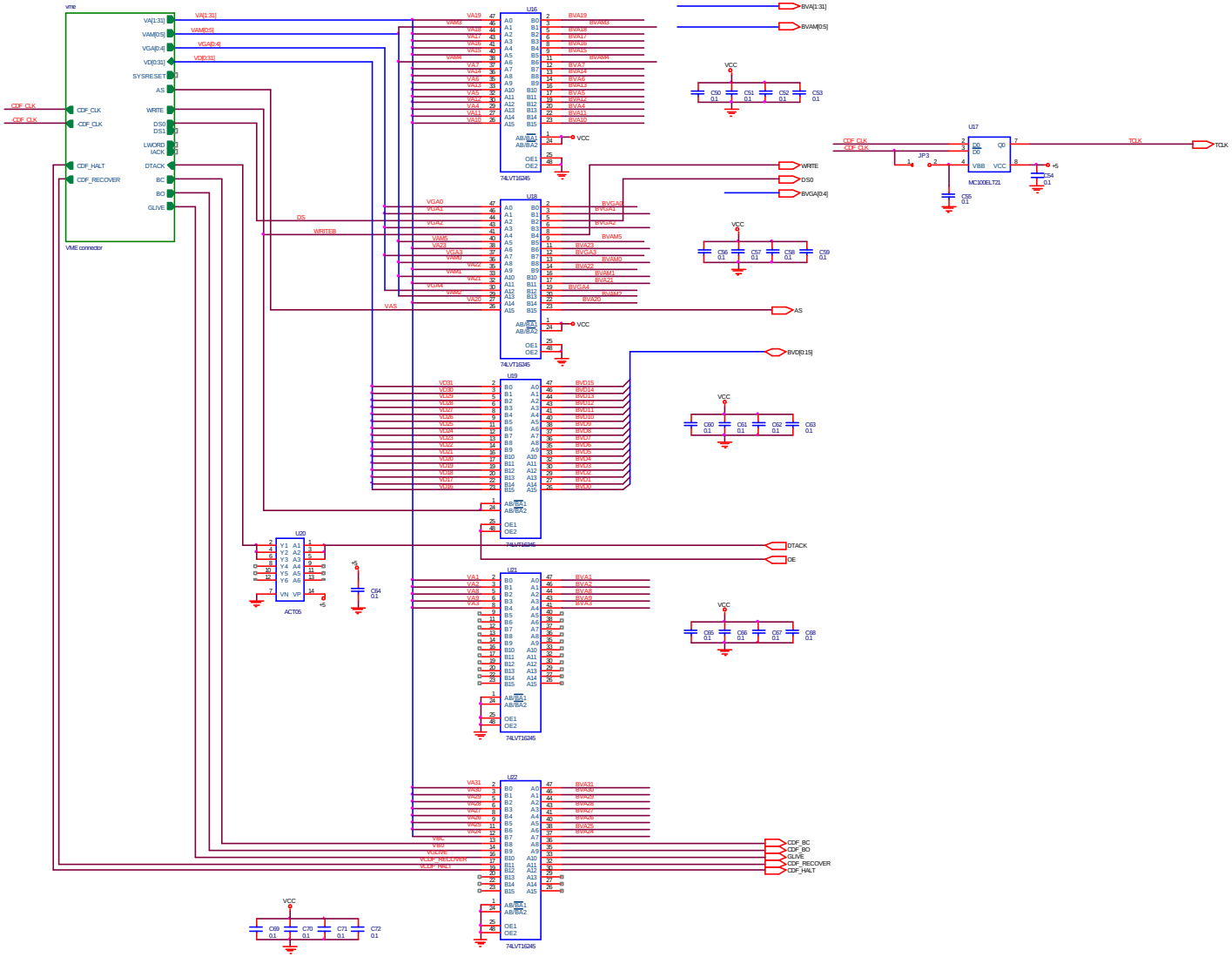


Figure 4. VME buffers

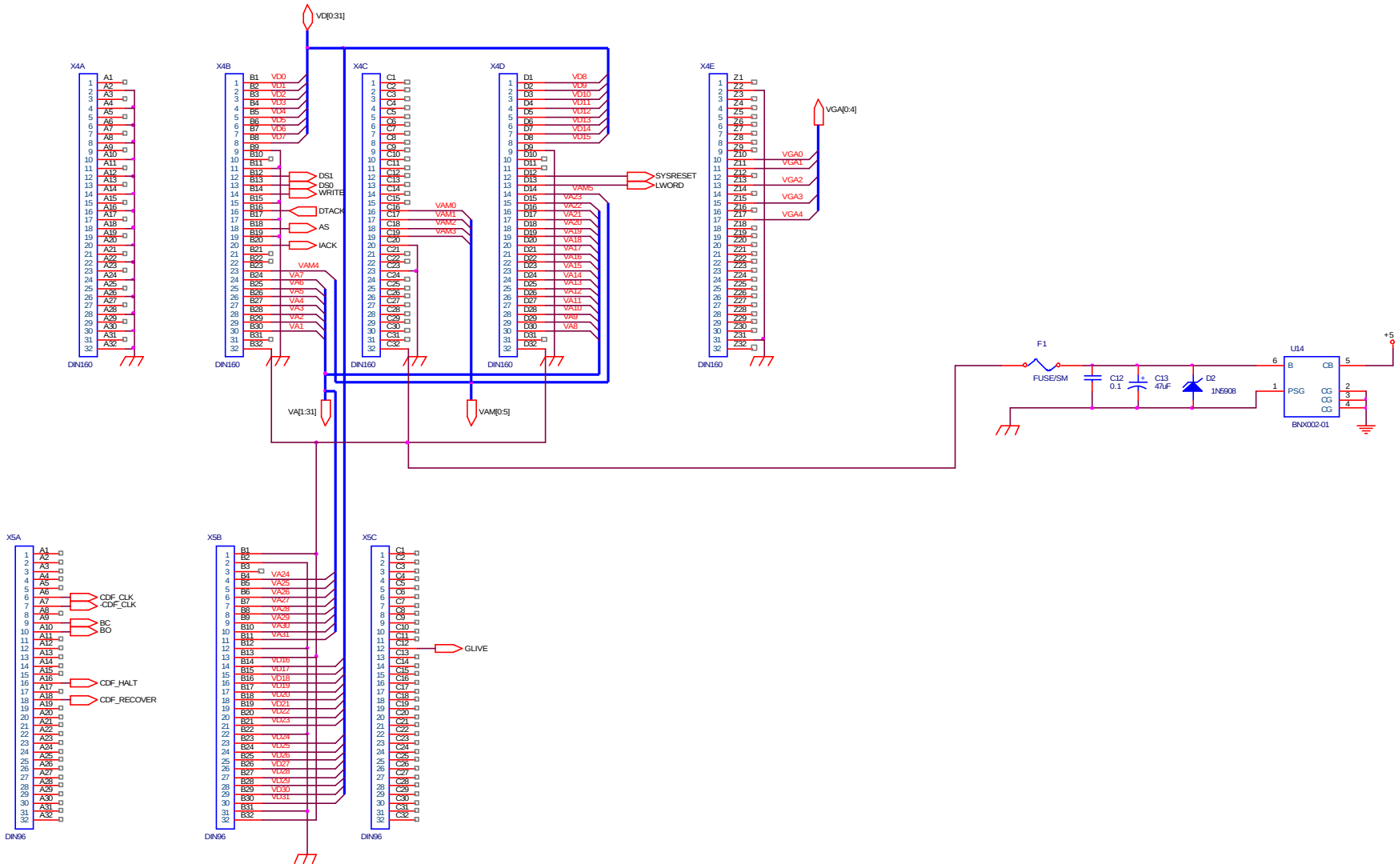


Figure 5. VME connector and power filter.

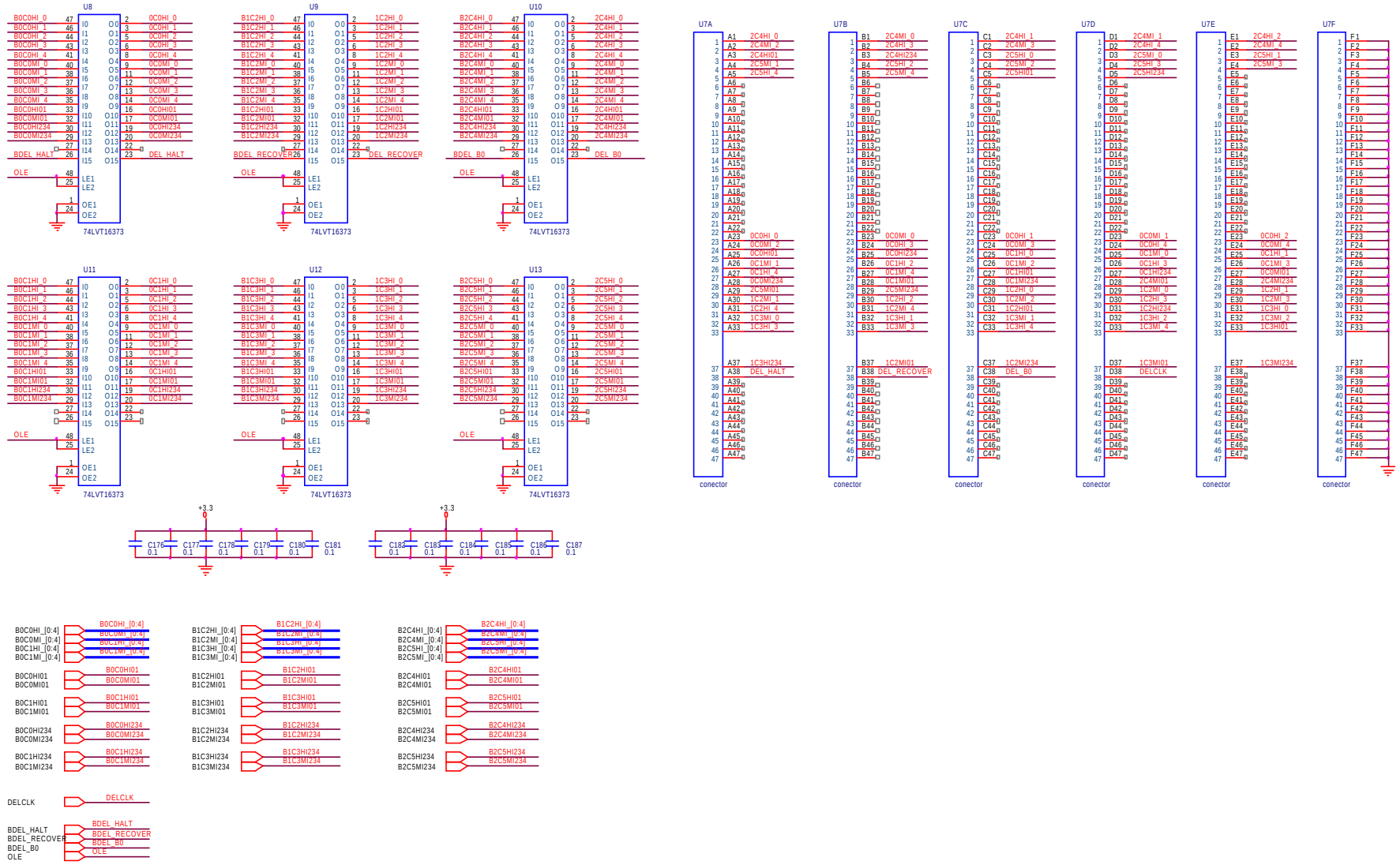


Figure 6. Backplane output

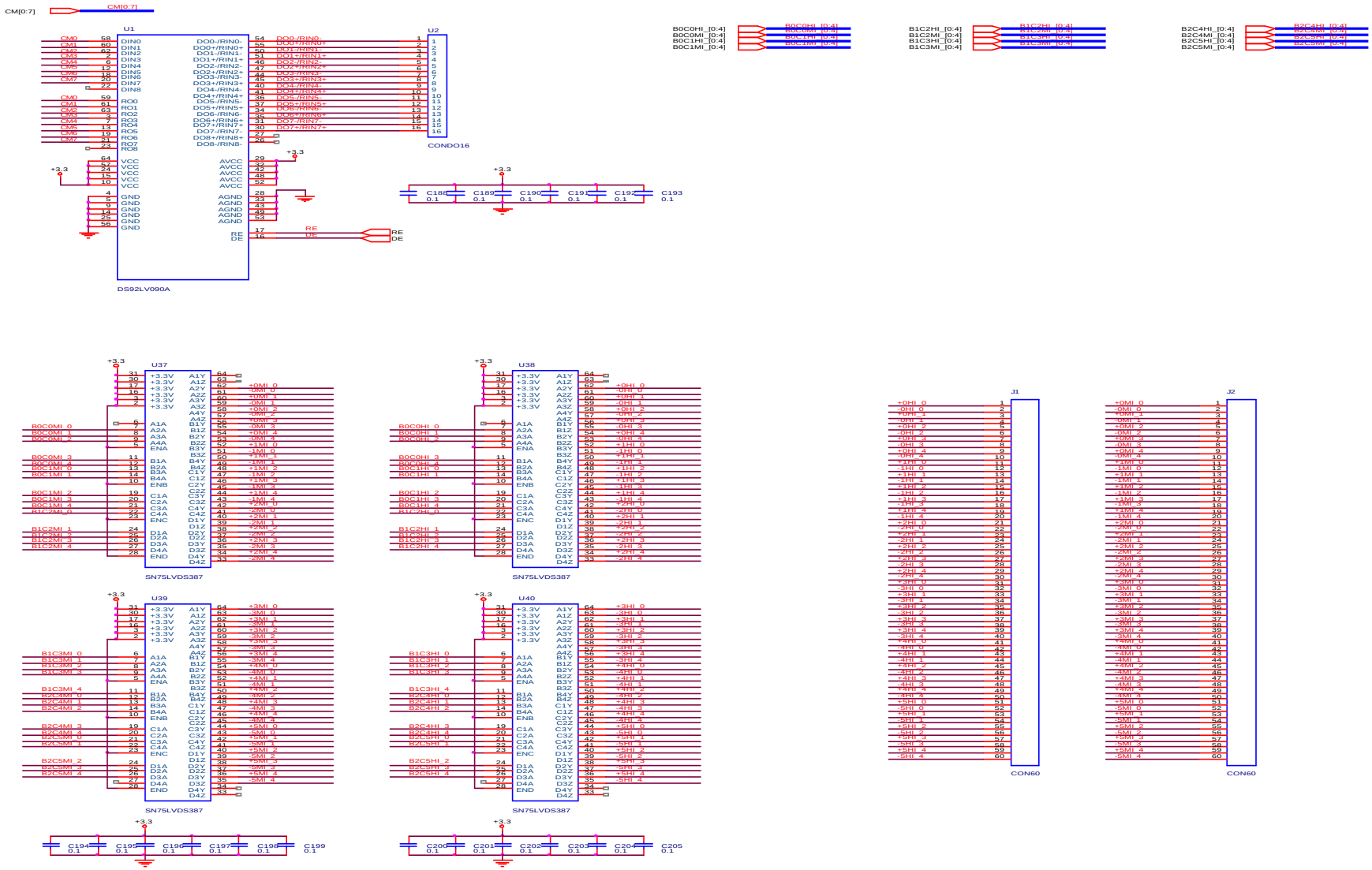


Figure 7. Front panel outputs