



Integrated Device Technology, Inc.

BICMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

IDT71B74

FEATURES:

- High-speed address to MATCH comparison time
— Commercial: 8/10/12/15/20ns (max.)
- High-speed address access time
— Commercial: 8/10/12/15/20ns (max.)
- High-speed chip select access time
— Commercial: 6/7/8/10ns (max.)
- Power-ON Reset Capability
- Low power consumption
— 830mW (typ.) for 12ns parts
— 880mW (typ.) for 10ns parts
— 920mW (typ.) for 8ns parts
- Produced with advanced BiCMOS high-performance technology
- Input and output directly TTL-compatible
- Standard 28-pin plastic DIP and 28-pin SOJ (300 mil)

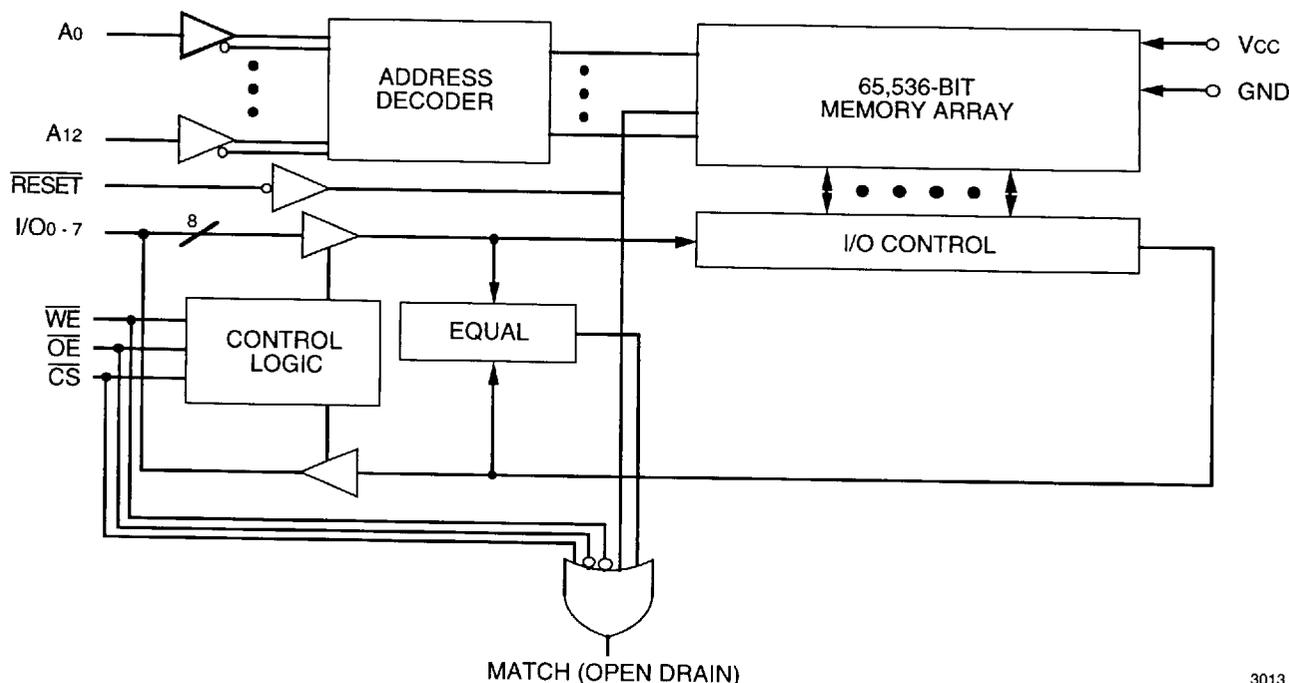
DESCRIPTION:

The IDT71B74 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT71B74 can map 8K cache words into a 2 megabyte address space by using the 21 bits of address organized with the 13 LSBs for the cache address bits and the 8 higher bits for cache data bits. Two IDT71B74s can be combined to provide 29 bits of address comparison, etc. The IDT71B74 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B74 can also be used as a resettable 8K x 8 high-speed static RAM.

The IDT71B74 is fabricated using IDT's high-performance, high-reliability BiCMOS technology. Address access times as fast as 8ns, chip select times of 6ns and address-to-match times of 8ns are available.

The MATCH pin of several IDT71B74s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput.

FUNCTIONAL BLOCK DIAGRAM



3013 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

AUGUST 1996

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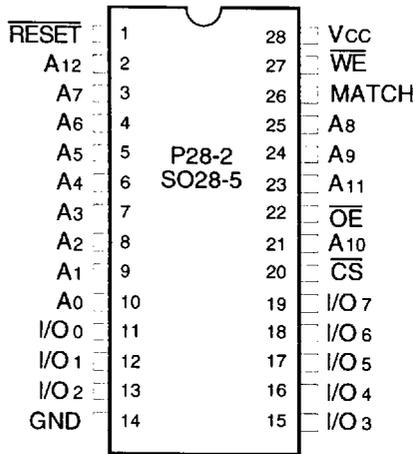
14.1

DSC-3013/4

1

4825771 0022810 857

PIN CONFIGURATION



**DIP/SOJ
TOP VIEW**

3013 drw 02

TRUTH TABLE^(1, 2)

WE	CS	OE	RESET	MATCH	I/O	Function
X	X	X	L	HIGH	—	Reset all bits to LOW
X	H	X	H	HIGH	Hi-Z	Deselect chip
H	L	H	H	LOW	DIN	No MATCH
H	L	H	H	HIGH	DIN	MATCH
H	L	L	H	HIGH	DOUT	Read
L	L	X	H	HIGH	DIN	Write

NOTES:

- H = V_{IH}, L = V_{IL}, X = DON'T CARE
- HIGH = High-Z (pulled up by an external resistor), and LOW = V_{OL}.

3013 tbl 01

PIN DESCRIPTIONS

Pin Names	Description
A ₀₋₁₂	Address
I/O ₀₋₇	Data Input/Output
CS	Chip Select
RESET	Memory Reset
MATCH	Data/Memory Match (Open Drain)
WE	Write Enable
OE	Output Enable
GND	Ground
V _{CC}	Power

3013 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 0.5V.

3013 tbl 03

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ Package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	7	pF

NOTE:

- This parameter is determined by device characterization, but is not production tested.

3013 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input HIGH Voltage ⁽¹⁾	2.2	—	6.0 ⁽⁴⁾	V
V _{IHR}	$\overline{\text{RESET}}$ Input Voltage	2.5 ⁽²⁾	—	6.0	V
V _{IL}	Input LOW Voltage	-0.5 ⁽³⁾	—	0.8	V

- NOTES:** 3013 tbl 05
- All inputs except $\overline{\text{RESET}}$.
 - When using bipolar devices to drive the $\overline{\text{RESET}}$ input, a pullup resistor of 1k Ω –10k Ω is usually required to assure this voltage.
 - V_{IL} (min.) = -1.5V for pulse width less than 10ns, once per cycle.
 - V_{TERM} must not exceed V_{CC} + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	5V \pm 10%

3013 tbl 06

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(V_{CC} = 5.0V \pm 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71B74S8	71B74S10	71B74S12	71B74S15	71B74S20	Unit	
I _{CC}	Dynamic Operating Current Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	$\overline{\text{WE}} = \text{V}_{\text{LC}}$	230	210	200	190	180	mA
		$\overline{\text{WE}} = \text{V}_{\text{HC}}$	210	200	170	160	150	mA

- NOTES:** 3013 tbl 07
- All values are maximum guaranteed values.
 - f_{MAX} = 1/trc, only input addresses are cycling at f_{MAX}.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V \pm 10%)

Symbol	Parameter	Test Condition	IDT71B74S		Unit
			Min.	Max.	
I _{LIL}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	5	μA
I _{LOL}	Output Leakage Current	V _{CC} = Max., $\overline{\text{CS}} = \text{V}_{\text{IH}}$, V _{OUT} = GND to V _{CC}	—	5	μA
V _{OL}	Output LOW Voltage	I _{OL} = 22mA MATCH	—	0.5	V
		I _{OL} = 18mA MATCH	—	0.4	
		I _{OL} = 10mA, V _{CC} = Min. (Except MATCH)	—	0.5	
		I _{OL} = 8mA, V _{CC} = Min. (Except MATCH)	—	0.4	
V _{OH}	Output HIGH Voltage	I _{OH} = -4mA, V _{CC} = Min. (Except MATCH)	2.4	—	V

3013 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

3013 tbl 09



3013 drw 03

Figure 1. AC Test Load

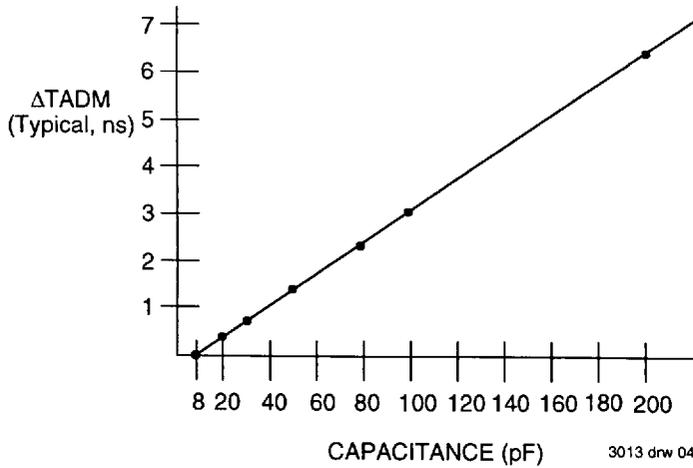


Figure 1A. Lumped Capacitive Load Typical Derating Curve

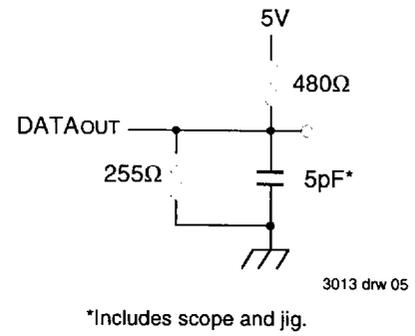


Figure 2. AC Test Load (for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

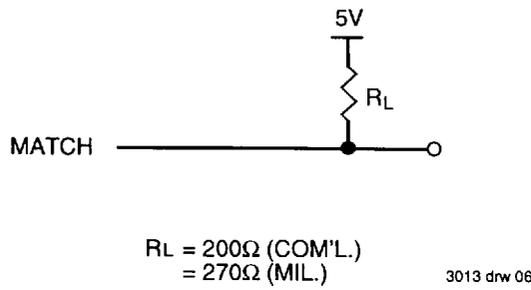


Figure 3. AC Test Load for MATCH

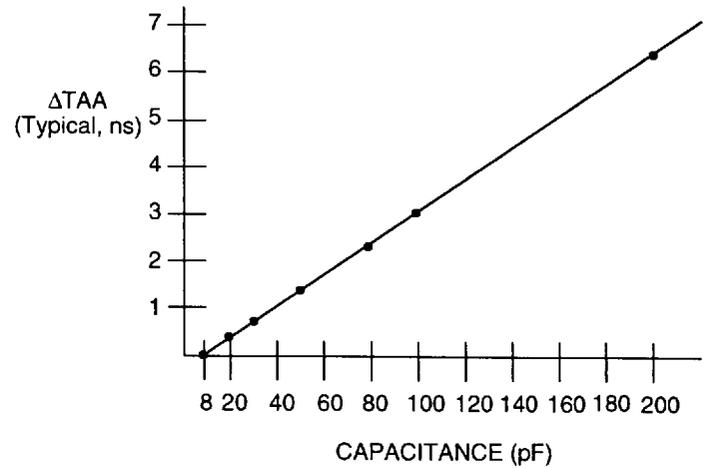
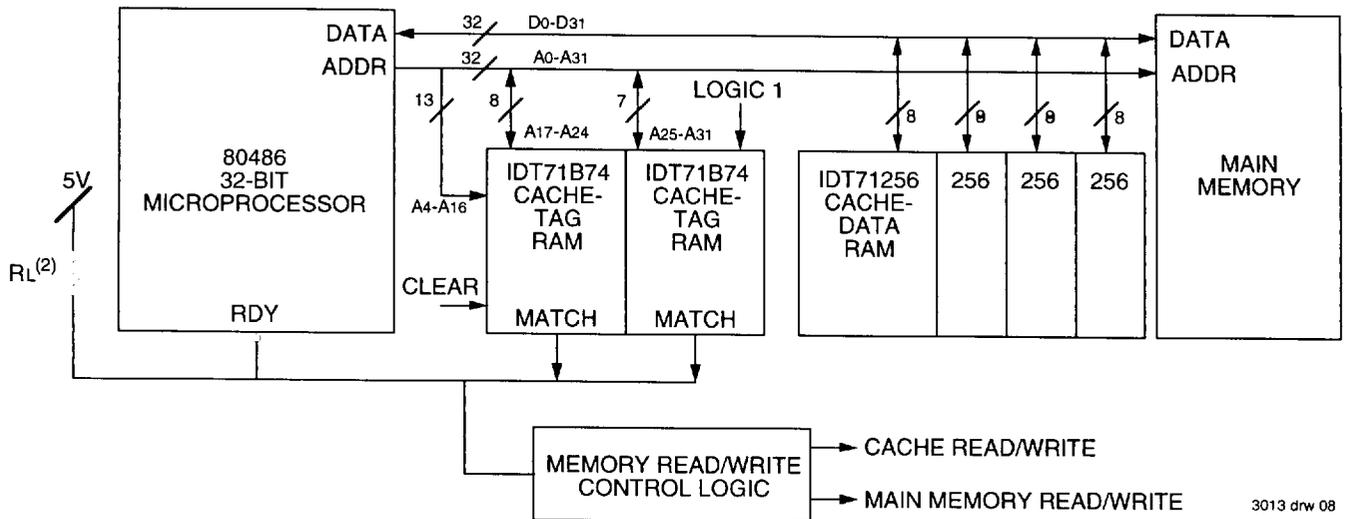


Figure 3A. Lumped Capacitive Load Typical Derating Curve



NOTES:

- For more information refer to IDT Application Notes AN-07 and AN-78 and Technical Notes TN-11 and TN-13.
- RL = 200Ω.

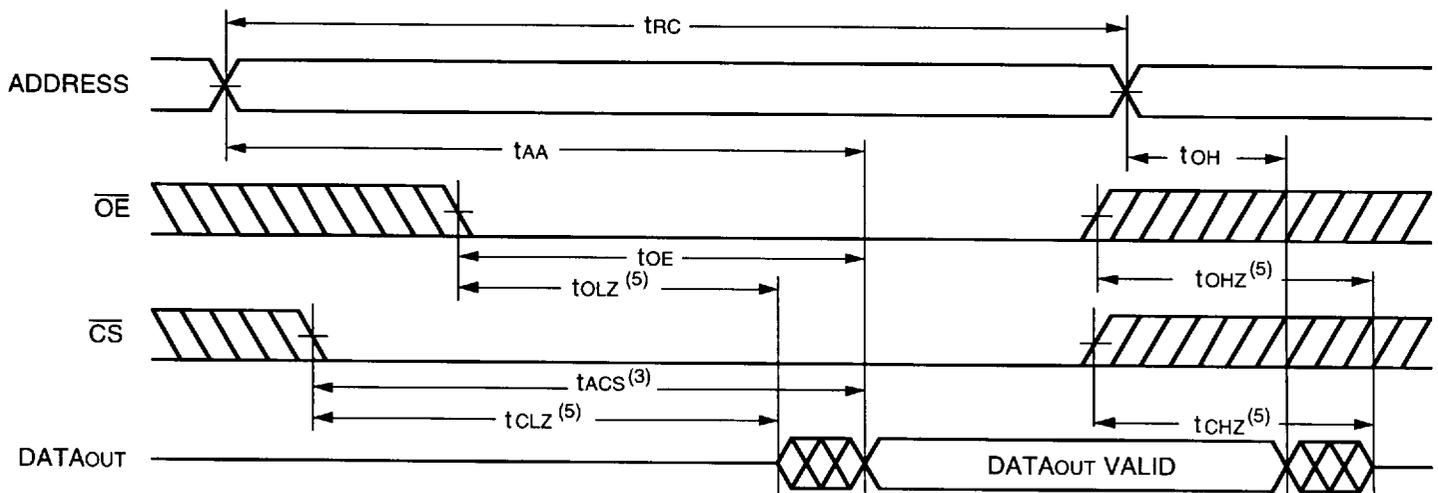
Figure 4. Example of Cache Memory System Block Diagram

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
t _{AA}	Address Access Time	—	8	—	10	—	12	—	15	—	20	ns
t _{ACS}	Chip Select Access Time	—	6	—	7	—	8	—	8	—	10	ns
t _{CLZ} ⁽¹⁾	Chip Select to Output in Low-Z	2	—	2	—	2	—	3	—	3	—	ns
t _{OE}	Output Enable to Output Valid	—	5	—	6	—	6	—	8	—	9	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	ns
t _{CHZ} ⁽¹⁾	Chip Select to Output in High-Z	—	4	—	5	—	5	—	7	—	8	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High-Z	—	4	—	4	—	5	—	5	—	8	ns
t _{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns

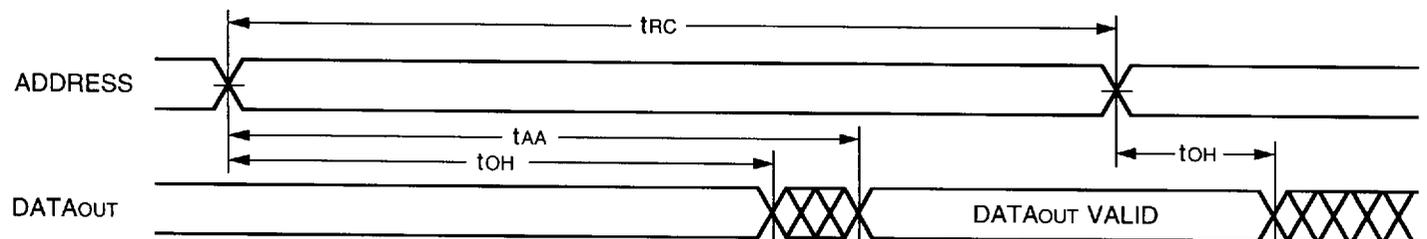
NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested. 3013 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



3013 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



NOTES:
1. \overline{WE} is HIGH for Read cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. Address valid prior to or coincident with \overline{CS} transition LOW; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is continuously active, \overline{OE} is LOW.
5. Transition is measured $\pm 200mV$ from steady state.

3013 drw 10

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$)

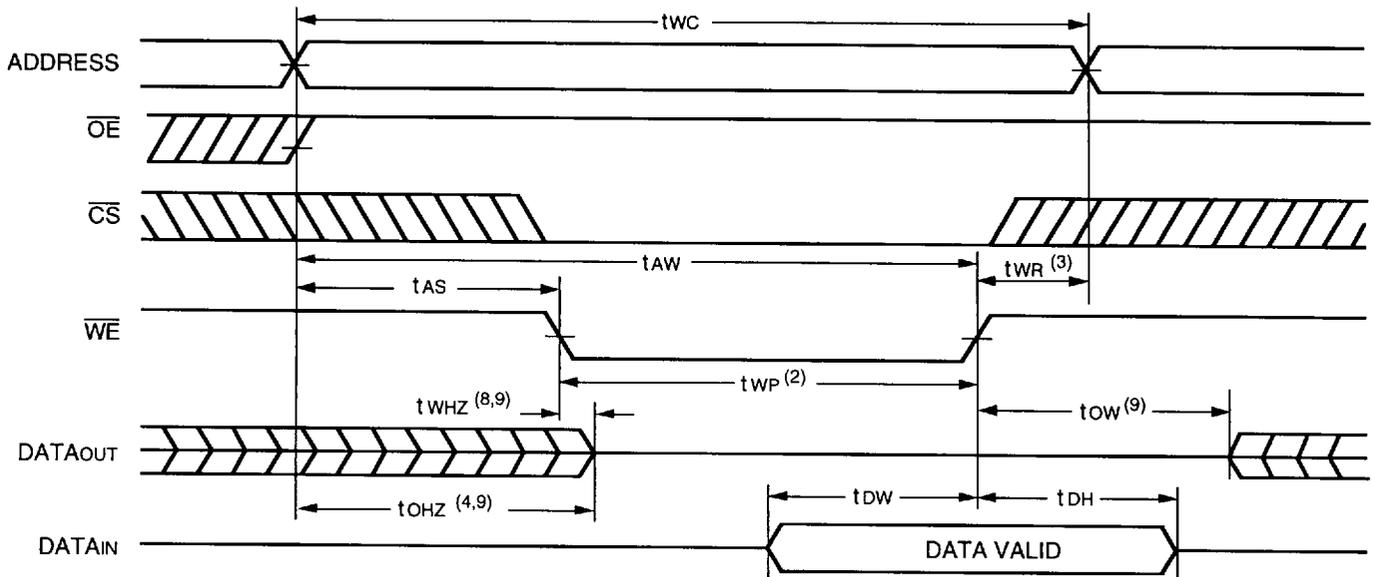
Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
tcw	Chip Select to End of Write	7	—	8	—	9	—	10	—	15	—	ns
tAW	Address Valid to End of Write	7	—	8	—	9	—	10	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	8	—	9	—	10	—	15	—	ns
tWR	Write Recovery Time (\overline{CS} , \overline{WE})	0	—	0	—	0	—	0	—	0	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	—	5	—	5	—	5	—	5	—	5	ns
tdw	Data Valid to End of Write	5	—	5	—	6	—	8	—	10	—	ns
tdH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tow ⁽¹⁾	Output Active from End of Write	2	—	2	—	2	—	2	—	2	—	ns

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

3013 tbl 11

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} Controlled Timing, \overline{OE} HIGH During Write)^(1, 6)

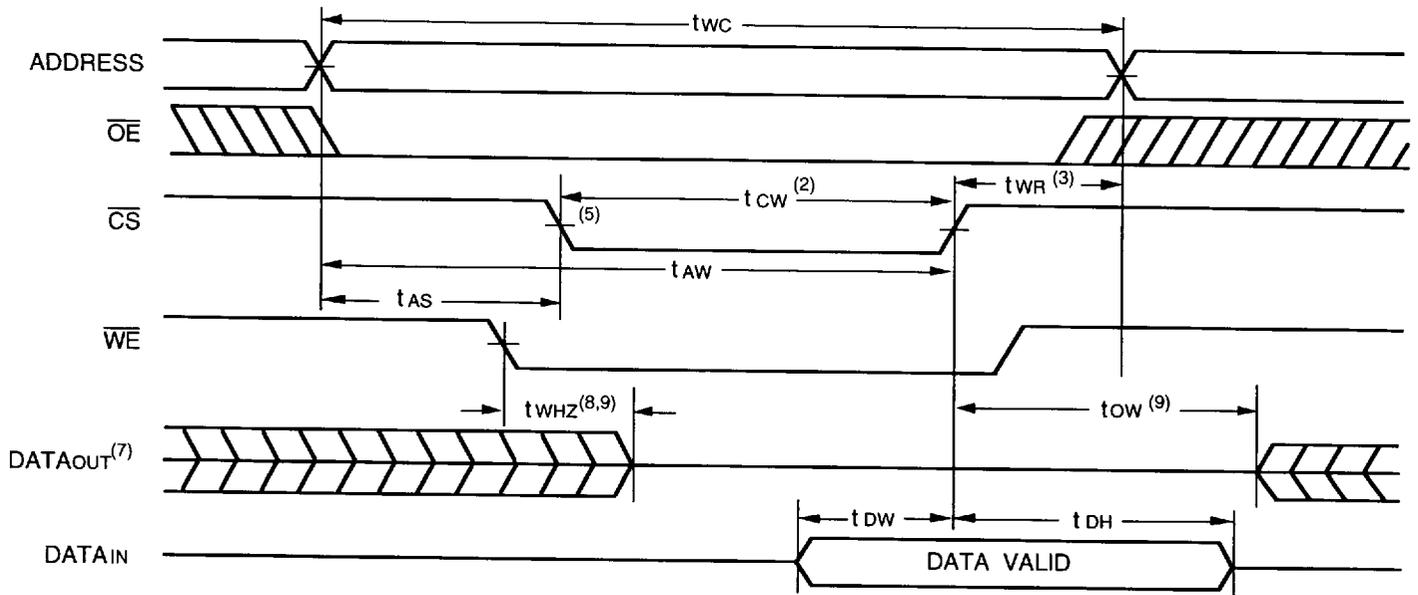


NOTES:

1. \overline{WE} , \overline{CS} must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW \overline{WE} and a LOW \overline{CS} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
6. \overline{OE} is continuously HIGH, $\overline{OE} \geq V_{IH}$. If during the \overline{WE} controlled write cycle the \overline{OE} is LOW, t_{WP} must be greater or equal to $t_{WHZ} + t_{ow}$ to allow the I/O drivers to turn off and the data to be placed on the bus for the required t_{ow} . If \overline{OE} is HIGH during the \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{wp} . For a \overline{CS} controlled write cycle, \overline{OE} may be LOW with no degradation to t_{cw} timing.
7. $DATA_{OUT}$ is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. t_{whz} is not included if \overline{OE} remains HIGH during the write cycle. If \overline{OE} is LOW during the Write Enabled write cycle then t_{whz} must be added to t_{wp} and t_{cw} .
9. Transition is measured $\pm 200mV$ from steady state.

3013 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} Controlled Timing)^(1, 6)



NOTES:

1. \overline{WE} , \overline{CS} must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW \overline{WE} and a LOW \overline{CS} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
6. \overline{OE} is continuously HIGH, $\overline{OE} \geq V_{IH}$. If during the \overline{WE} controlled write cycle the \overline{OE} is LOW, t_{WP} must be greater or equal to $t_{WHZ} + t_{OW}$ to allow the I/O drivers to turn off and the data to be placed on the bus for the required t_{OW} . If \overline{OE} is HIGH during the \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP} . For a \overline{CS} controlled write cycle, \overline{OE} may be LOW with no degradation to t_{CW} timing.
7. $DATA_{OUT}$ is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. t_{WHZ} is not included if \overline{OE} remains HIGH during the write cycle. If \overline{OE} is LOW during the Write Enabled write cycle then t_{WHZ} must be added to t_{WP} and t_{CW} .
9. Transition is measured $\pm 200mV$ from steady state.

3013 drw 12

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$)

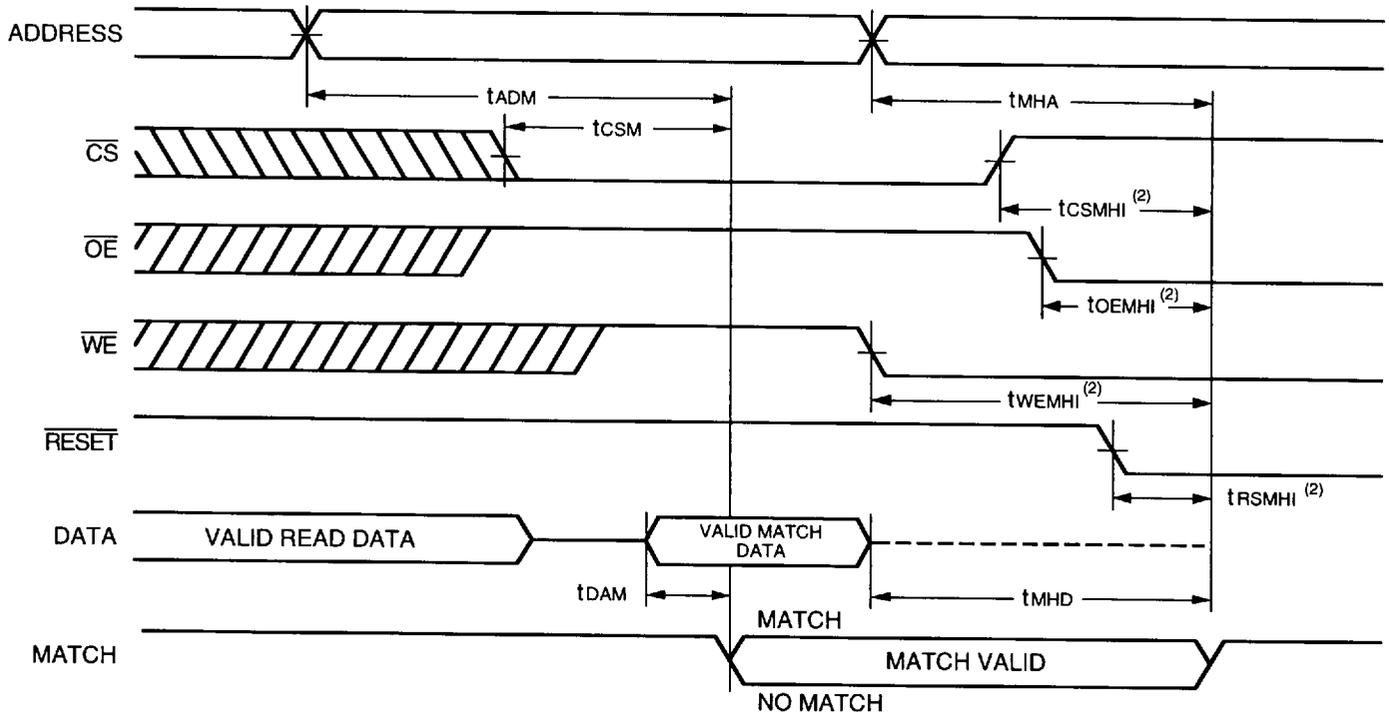
Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Match Cycle												
t_{ADM}	Address to MATCH Valid	—	8	—	10	—	12	—	15	—	20	ns
t_{CSM}	Chip Select to MATCH Valid	—	7	—	7	—	8	—	10	—	10	ns
$t_{CSMH}^{(1)}$	Chip Select to MATCH HIGH	—	7	—	8	—	8	—	8	—	8	ns
t_{DAM}	Data Input to MATCH Valid	—	7	—	8	—	10	—	12	—	12	ns
$t_{OEMH}^{(1)}$	\overline{OE} LOW to MATCH HIGH	—	7	—	8	—	10	—	10	—	10	ns
$t_{WEMH}^{(1)}$	\overline{WE} LOW to MATCH HIGH	—	7	—	8	—	10	—	10	—	10	ns
$t_{RSMH}^{(1)}$	\overline{RESET} LOW to MATCH HIGH	—	8	—	10	—	10	—	12	—	15	ns
t_{MHA}	MATCH Valid Hold From Address	2	—	2	—	2	—	2	—	2	—	ns
t_{MHD}	MATCH Valid Hold From Data	2	—	2	—	2	—	2	—	2	—	ns

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3013 tbl 12

MATCH TIMING⁽¹⁾



NOTES:

1. It is not recommended to float data and address input pins while the MATCH pin is active.
2. Transition is measured at $\pm 200\text{mV}$ from steady state.

3013 drw 13

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{V} \pm 10\%$)

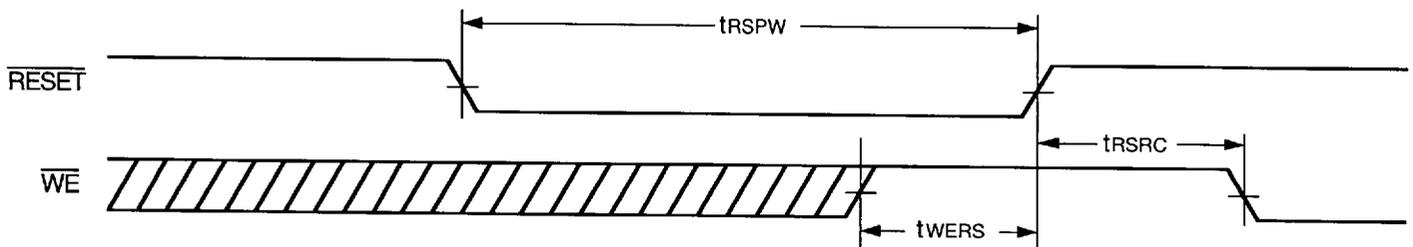
Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle												
$t_{RSPW}^{(1)}$	Reset Pulse Width	30	—	35	—	35	—	40	—	45	—	ns
t_{WERS}	\overline{WE} HIGH to Reset HIGH	5	—	5	—	5	—	5	—	5	—	ns
t_{RSRC}	Reset HIGH to \overline{WE} LOW	25	—	25	—	25	—	30	—	30	—	ns
$t_{PORS}^{(2)}$	Power On Reset	100	—	100	—	100	—	120	—	120	—	ns

NOTES:

1. Recommended duty cycle = 10% maximum.
2. This parameter is guaranteed with the AC Load (Figure 1) by device characterization, but is not production tested.

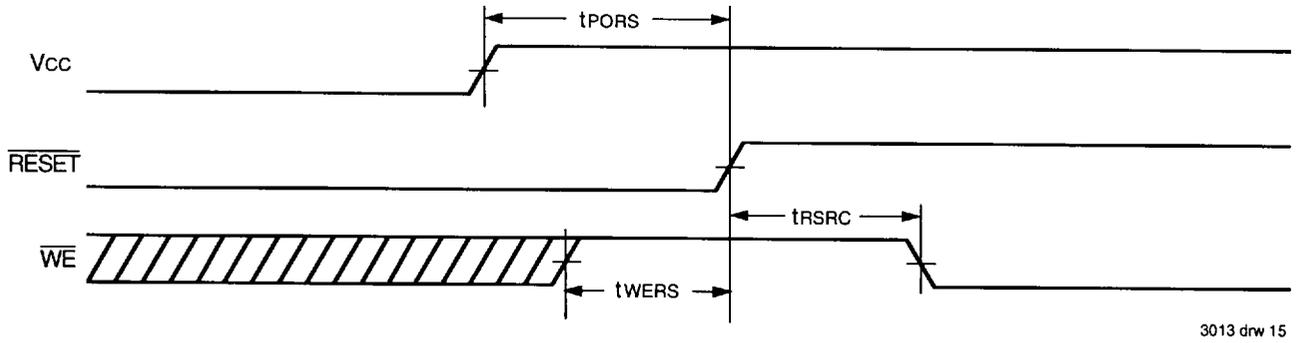
3013 tbl 13

RESET TIMING

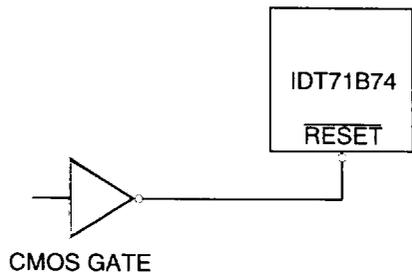


3013 drw 14

POWER ON RESET TIMING

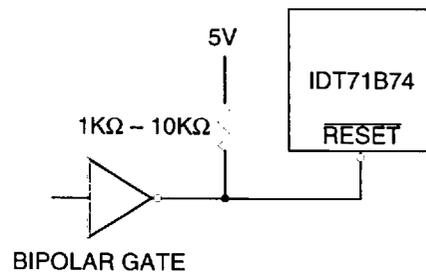


3013 drw 15



3013 drw 16

Driving the $\overline{\text{RESET}}$ pin with CMOS logic.



3013 drw 17

Driving the $\overline{\text{RESET}}$ pin with bipolar logic.

Figure 5.

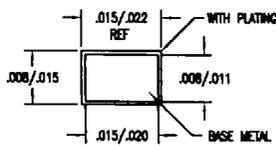
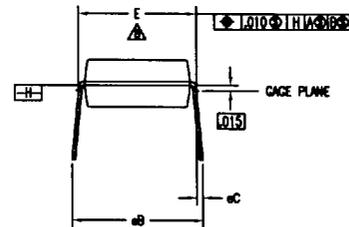
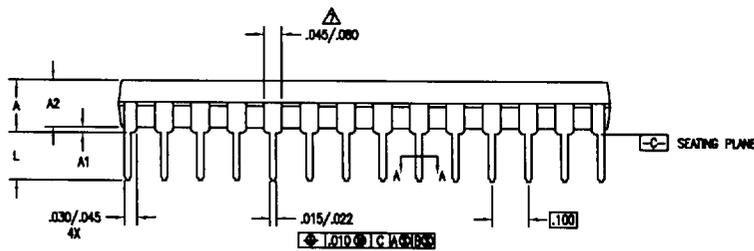
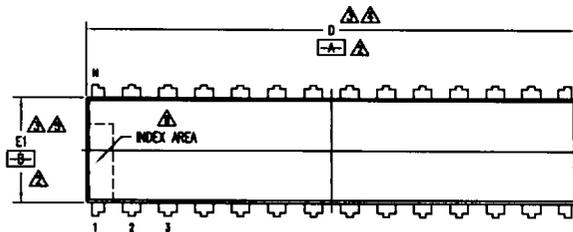
ORDERING INFORMATION

IDT	71B74	S	XX	X	X	
Device Type	Power	Speed	Package	Process/ Temperature Range		
					Blank	Commercial (0°C to +70°C)
					TP	Plastic DIP (300 mil) (P28-2)
					Y	SOJ (Small Outline IC, J-bend) (SO28-5)
					8	Commercial Only, SOJ Only } Speed in ns
					10	
					12	
					15	
					20	

3013 drw 18

PACKAGE DIAGRAM OUTLINES
 PLASTC DIP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27852	04	REDRAW TO JEDEC FORMAT	03/18/85	



SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 3578 Stoner Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 408-8874 TIR: 910-338-8070
DECIMAL	ANGULAR	
±.005	±	
±.0025		
±.0015		
±.001		
APPROVALS	DATE	TITLE
DRAWN Ad	07/18/85	PT 28 PACKAGE OUTLINE
CHECKED		.300" BODY WIDTH PDIP
		.100" PITCH
SIZE	DRAWING No.	REV
C	PSC-4018	04
DO NOT SCALE DRAWING		

079

PACKAGE DIAGRAM OUTLINES
 PLASTIC DIP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27852	04	REDRAW TO JEDEC FORMAT	03/18/96	

SYMBOL	JEDEC VARIATION			NOTES
	AH			
	MIN	NOM	MAX	
A	.145	-	.180	
A1	.015	-	.030	
A2	.120	.135	.150	
D	1.345	1.365	1.385	3,4
E	.300	.310	.325	8
E1	.275	.285	.295	3,5
eB	.310	-	.400	
eC	.000	-	.050	
L	.120	.135	.150	
N	2B			

NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- △ DATUMS \square -A \square AND \square -B \square TO BE DETERMINED AT DATUM PLANE \square -H \square
- △ DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE \square -H \square
- △ DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .010 PER SIDE
- △ DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- △ DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- △ LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .010 MAXIMUM TOTAL PER LEAD
- △ DIMENSION E IS MEASURED ON THE OUTSIDE SURFACE OF THE LEADS AT THE GAGE OF .015 BELOW DATUM PLANE \square -H \square
- 9 ALL DIMENSIONS ARE IN INCHES
- 10 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-085, VARIATION AH

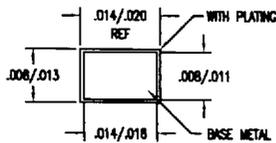
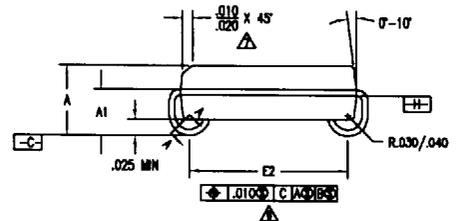
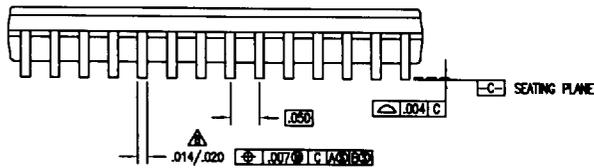
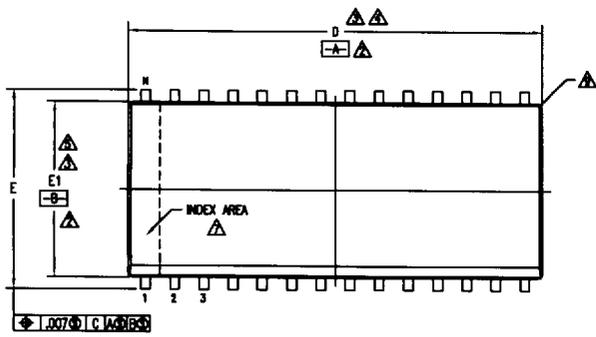
TOLERANCES UNLESS SPECIFIED		 Integrated Device Technology, Inc. 2375 Blunder Way, Santa Clara, CA 95054 PHONE: (408) 752-8116 FAX: (408) 486-8674 TSW 910-338-2070	
DECIMAL	ANGULAR	TITLE PT 28 PACKAGE OUTLINE	
±	±	.300" BODY WIDTH PDIP	
±	±	.100" PITCH	
APPROVALS	DATE	SIZE	DRWG No.
Ad	07/19/96	C	PSC-4018
CHECKED		REV	04
DO NOT SCALE DRAWING			

80

PACKAGE DIAGRAM OUTLINES

SOJ

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27844	03	REDRAW TO JEDEC FORMAT	03/15/95	



SECTION A-A

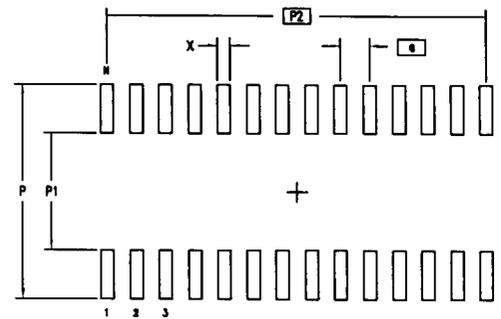
TOLERANCES UNLESS SPECIFIED		 Integrated Device Technology, Inc. 2875 Stoner Way, Santa Clara, CA 95054 PHONE (408) 727-8710 FAX (408) 482-8274 TWR 910-328-2070	
DECIMAL	ANGULAR		
.0005	±		
APPROVALS	DATE	TITLE	
DRAWN AA	03/16/95	PJ 20 & 28 PACKAGE OUTLINE	
CHECKED		.300" BODY WIDTH SOJ	
		.050" PITCH	
	SIZE	DRAWING NO.	REV
	C	PSC-4024	03
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES
SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27844	03	REDRAW TO JEDEC FORMAT	03/15/85	

SYMBOL	SO20-1			NOTE	SO28-5			NOTE
	JEDEC VARIATION				JEDEC VARIATION			
	AD				AF			
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.120	.130	.140		.120	.130	.140	
A1	.078	.086	.095		.078	.086	.095	
D	.500	.506	.512	3,4	.700	.706	.712	3,4
E	.335	.340	.347		.335	.340	.347	
E1	.292	.296	.300	3,5	.292	.296	.300	3,5
E2	.262	.267	.272	6	.262	.267	.272	6
N	20				28			

LAND PATTERN DIMENSIONS



NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS \square -A- and \square -B- TO BE DETERMINED AT DATUM PLANE \square -H-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE \square -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E2 TO BE DETERMINED AT SEATING PLANE \square -C- CONTACT POINT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-088, VARIATION AD & AF

	MIN	MAX	MIN	MAX
P	.362	.370	.362	.370
P1	.196	.204	.196	.204
P2	.450 BSC		.650 BSC	
X	.018	.026	.018	.026
e	.050 BSC		.050 BSC	
N	20		28	

TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, INC.	
DECIMAL	ANGULAR	2870 Stoner Way, Santa Clara, CA 95054	
±	±	PHONE (408) 727-8116	
DIMS.		FAX: (408) 985-8874	
DIMS.		TMR: 610-338-8270	
APPROVALS	DATE	TITLE	
DRAWN	03/15/85	PJ 20 & 28 PACKAGE OUTLINE	
CHECKED		.300" BODY WIDTH SOJ	
		.050" PITCH	
SIZE	DRAWING No.	REV	
C	PSC-4024	03	
DO NOT SCALE DRAWING			