



TDC Review

Report to the TDC Review
Committee

Presented by Myron Campbell



Milestones

- First version JMC96 – April 1994
- Second version JMC96 – May 1995
- Third version JMC96 – February 1996
- Fourth version JMC96 – June 1996
- Final version JMC96 – August 1996
- TDC 16A – 1994
- TDC 16B – 1995
- TDC 96A – 1996
- TDC 96B – 1997
- TDC 96C – 1998
- TDC 96D – March 1999



Status in Summer 2000

- The first order of boards were difficult to get to work. There were problems with vias, most boards had one or more random signal which was not connected. We could deliver about 7 boards per week.
- The last order order of 180 boards were much easier to make work. When not limited by delivery of boards we could produce 45 per week.



Status in Summer 2000

- The boards which were delivered were failing. Additional vias were failing, the boards were blowing buffer chips, and it seemed a new problem was found every week.
- There were different requirements for bringing up the COT – they wanted TDC boards that just worked in order to test the TDC – and for delivering functioning TDC boards – we needed to understand in detail the conditions when problems were seen.



List of Problems

- The list of unsolved problems presented at the last review was:
 - Bad vias
 - Blown buffer chips
 - TDC Crate Hangs
 - Mezzanine timeout
 - Readout errors
- The problems which were discovered since then are:
 - An extra word is read out of the FIFO at the end of block transfer read.
 - Individual boards can hang requiring a VME reset.



ECO 1 – Clock Strobes PAL

- DSP reads and VME reads were not synchronized
- Discovered during initial testing
- The strobes controlling the reads needed to be clocked
- Added a wire to bring the clock to the PAL, generated new PAL code



ECO 2 – L2A0 to TDC0-7

- Channels 0 to 7 were occasionally having extra hits
- Discovered early in testing
- Crosstalk between the clock line and the Level 2 accept line.
- Cut the trace, replace the trace with a wire



ECO 3 – Buffer Chips

- Buffer chips were continuing to fail.
- The previous attempts at fixes were based on a diagnosis of the failure mode by Cypress. A new analysis by Texas Instruments pointed out another possible problem
- There was bus contention during power up while VCC was between 2.4 and 4 volts.
- Add two resistors to pull up the enables on the buffers
- This reduced the rate to a mean time between failures of about 4 years, but the problem still existed



ECO 4 – Buffer Chips

- The buffer chips were continuing to fail but at a lower rate.
- Discovered an additional source of bus contention which occurred during reset. A bus enable signal that was documented as being high during reset was in fact tri-state.
- Added a pull up resistor to disable the buffers during reset.



ECO 5 – Replace cy7c960a

- When a crate was filled with TDC boards the crate would not work after power on.
- This was only discovered after several crates had full complements of TDC boards using the production power supply
- The VCC ramp was slowed when more current was drawn. This exposed a problem in the design of the VME interface chip.
- Replace the chip with a new version



ECO 6 – Change ECO1

- Occasional data corruption was observed if the TDC had VME access while the DSP was processing an event.
- This only occurred when individual TDC's were being monitored for DONE in order to speed up the readout time.
- A write strobe from the DSP was still active after the DSP gave control of the bus to VME. A VME read would then write to static RAM.
- Delay giving control to VME by $\frac{1}{2}$ clock cycle. This required removing ECO 1 and picking up the opposite phase of the clock.



ECO 7 – Fix Read Signal

- If VME was reading out one event in the FIFO while the DSP was processing the next event the data read out was corrupted.
- This was only seen after the DAQ readout was advanced to overlap the processing of one event with the readout of the previous event.
- The incorrect read signal was used to enable the readout of the FIFO. The correct signal was used in the logic. Required cutting one trace and adding a wire.



ECO 8 – Bunch counter L1accept

- Occasionally the bunch counter returned the wrong value.
- This was seen very early on. Several solutions were tried. This was made complicated by the difficulty of reproducing the error in a test stand.
- The Level 1 accept signal to the bunch counter was picking up noise from cross talk with other lines.
- Invert the Level one accept signal. Cross talk never crosses digital threshold



DSP Code

- Some problems have been solved by modifying the DSP code.
- When the FIFO is readout in Block transfer mode the VME interface pre-fetches the next word. The VME master must drop the bus at the time it acknowledges the last read in order to prevent the pre-fetch. The PowerPC controllers do not do this. Consequently the FIFO had one extra word readout.
- Modify the DSP code to wait for FIFO Empty before writing the next event.



DSP Code

- Some boards were seen to hang when the input rate was very high and the DSP was programmed to discard extra hits.
- The code to discard extra hits was a two instruction loop – read the TDC, branch if not the last hit.
- The data lines were oscillating during the time the DSP was pre-fetching the branch instruction while preparing to read the TDC. The code was modified to use a delayed branch.
- We believe this is a design flaw in the DSP. We are in the process of documenting the exact conditions and will consult with engineers at Texas Instruments.



Remaining Problems

- Remove sysreset susceptibility in PAL
 - ECO 6 removed the source of cross talk to the SYSRESET line, and problems seen with occasional resets of the board have disappeared. But the logic is still susceptible to glitches on SYSRESET. Modify the PAL to require SYSRESET for at least one clock cycle
- Fix mezzanine PAL to timeout properly
 - The PAL logic to timeout a read of a mezzanine card when no mezzanine card is installed requires two states to transition on the same clock. One of the inputs to the state is the asynchronous monostable timeout signal.
- Track down source of foul fetch
 - What is wrong with the DSP?



Placing next order

- Will order 200 boards
 - Based on analysis by Cathy
 - 125 LVDS boards
 - 75 ECL boards
- Establish parts acquisition
 - Most parts will be purchased by assembly house
 - We will supply some connectors, programmed logic, and TDC chips
- Modify design
 - All ECO's will be incorporated into new design. Cross talk analysis will be redone. A few corrections will be made to the new boards to improve signal quality.



Placing Next Order

- Manufacture a few boards, assemble
 - Since we have a new design we will have to test with 20 boards.
 - Will change from OPC to white tin copper coating
- Follow with full production
 - Expect full production can start in June.
 - Expect to be able to test and deliver 45 boards per week.

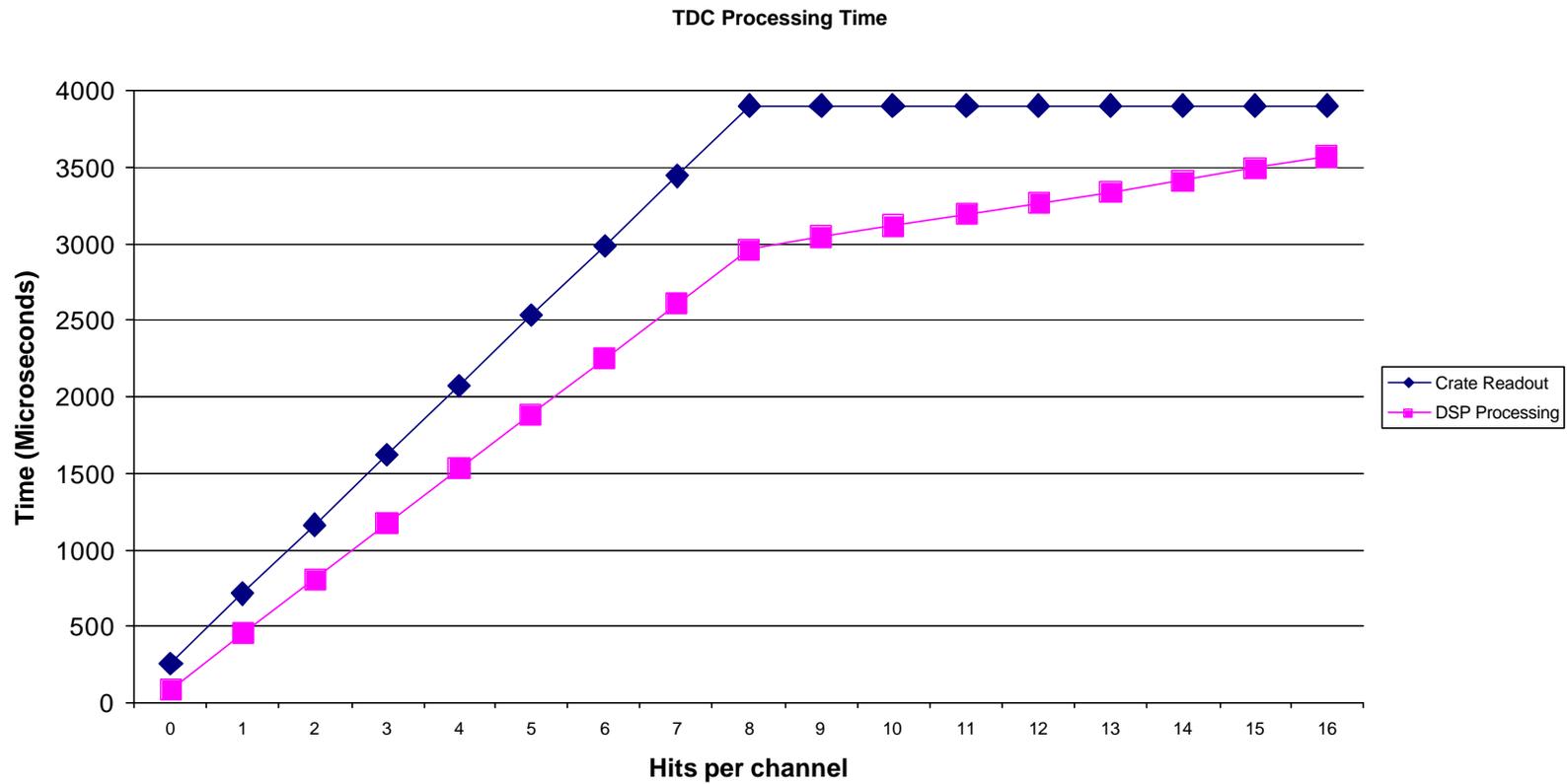


Timing studies

- We have tested the TDC boards in operating modes that were not used in the commissioning run.
- We are issuing a Level 2 accept for event $N+1$ before the data from event N is read from the FIFO.
- The DSP takes time to read and format the TDC data. This takes place on all boards in the crate at the same time. The DAQ system reads from the FIFO one board at a time.
- Have a plot of readout time. Have plotted the number of hits per channel, assumed uniform, and assume 18 TDC cards per crate.



DSP and Readout time





Timing Studies

- The broad stroke picture shows that the time for DSP processing can be hidden behind readout.
- Additional studies are needed with:
 - Diagnostics to accurately measure the time of each processing stage
 - Controlling the number of hits per channel to fixed numbers
 - Allowing the inputs to fluctuate according to a realistic distribution



DAQ Tests

- We believe we have addressed all known problems
- We have about 80 boards in the collision hall with all ECO's and new code
- Request long duration tests with these crates, with inputs connected, low DAC thresholds, in buffered readout mode
- Need careful monitoring and diagnosis of any problem that appears in these tests.



TASK Force

- As a result of the review in September a TDC TASK Force was setup
- The task force met every day
- Allocated where TDC boards would be used
- When problems were seen the conditions for producing the problem were established
- Problems were reproduced in test stands
- Once this was done it became possible to solve the problem
- Make modifications to existing boards
- Testing boards before insertion
- Has served its purpose



Need to Continue Task Force

- Need to follow procedures for getting the remaining boards brought up to the current ECO.
- Need key people who understand the value of following the procedures and penalties for not
- Ron Moore will lead this group
- Switch to weekly rather than daily meetings after the detector rolls in.
- Continue with aggressive tracking and diagnosis of any problems that appear.



Operations Experience

- The Time to Digital Conversion part of the TDC's work very well. Can reconstruct tracks.
- After the boards were installed and not moved they were reasonably reliable – no solid evidence of vias continuing to fail
- Each improvement of the DAQ system uncovered additional problems in the design or layout of the TDC board
- Need to continue to run crates full of boards at high speed.
- Need careful monitoring and diagnosis of any problem that appears in these tests.



Plans for Installation

- Have documented procedures for removing boards, testing boards, and re-installing boards in the system.
- Task force closely coupled to detector groups to set priorities of which TDC boards are installed.



Current Status of Boards

	LVDS	ECL
Installed at B0	187	45
Ready for tracktest	39	0
At PREP wait for modifications	80	12
Ready to ship to Fermilab	4	4
Ready for burnin	10	19
Ready for Calibration	3	3
In Repair	51	50
Really Bad	22	5
Total At Fermilab	306	57
At Michigan, close to shipping	17	26
Bottom Line	323/331	83/106
In transit	9	0