



Director's Review

August 12, 2002

The CDF runIIb Silicon Detector Technical Presentation

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INFN-Padova and Fermilab

For the CDF collaboration



Run IIb Silicon - Outline

- Overview of Goals and Constraints
- Layout
- Stave Concept
- Component Details
- L0 design
- Conclusions



Radiation Damage Issues

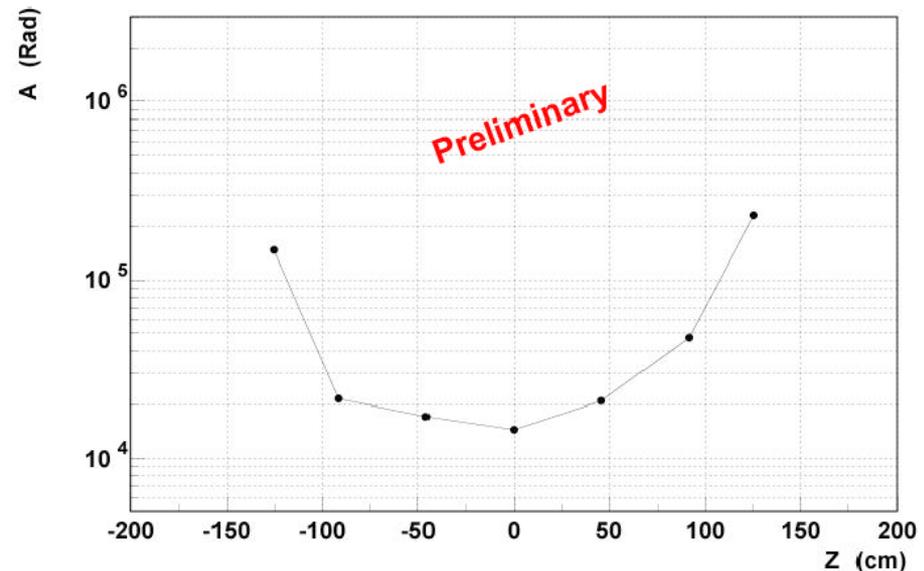
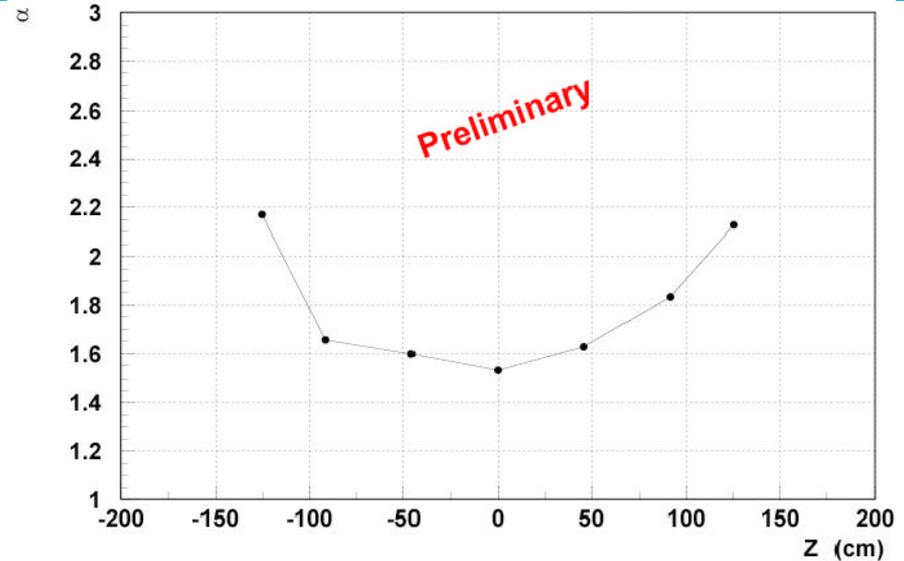
- In fall 2000 a runIIb working group was formed to calculate the longevity of the present Iia silicon detector.
- Based on run Ia and Ib data the group calculated the expected lifetime due to radiation damage of the Iia silicon detector (in table).
- The upper limit on the silicon survival is due to a combination of:
 - ➔ Lack of high voltage operability of double sided silicon sensors
 - ➔ Insufficient radiation hardness of the svx3d chip
 - ➔ Insufficient radiation hardness of the optical readout
 - ➔ Need to operate silicon sensors at lower temperature

CDF	R_{min} (cm)	L (fb^{-1})
L00	1.35	7.4
L0	2.54	4.3
L1	4.12	8.5
L2	6.52	10.7
ISL	20 - 28	>40
DOIMs	14	5.7



RunIIb: radiation damage issues

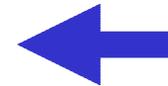
- Leakage current scales with dose linearly
- Predictions used to determine durability of Ila silicon sensors very much valid.
- Early Ila measurements seems to confirming these prediction BUT it is still too early to draw conclusions.
 - Errors are still quite large
- Very important to measure the radial dependence of the dose





Radiation Tolerance Implications

Layer	Radius (cm)	Dose 10^{13} (1Mev neutron cm^{-2} fb)
0	2.1	13.6
1	3.5	5.7
2	5.9	2.3
3	9.1	1.1
4	11.9	0.7
5	14.7	0.5



Predicted dose for runIIb
Silicon (from Ia,Ib data) at
different radii

- To cope with higher doses during runIIb we need:
 - ➔ A radiation hard chip
 - ➔ Single sided sensors
 - ➔ Operate sensors at high voltage (up to 350V)
 - ➔ Keep the sensor temperature low (-5C at L0)
- Present technology allows above specs to be achieved
- Consequences:
 - ➔ Need a new readout chip
 - ➔ Need more silicon
 - ➔ New H/L voltage distribution system
 - ➔ Need to directly cool the silicon



Silicon Upgrade for Run IIb

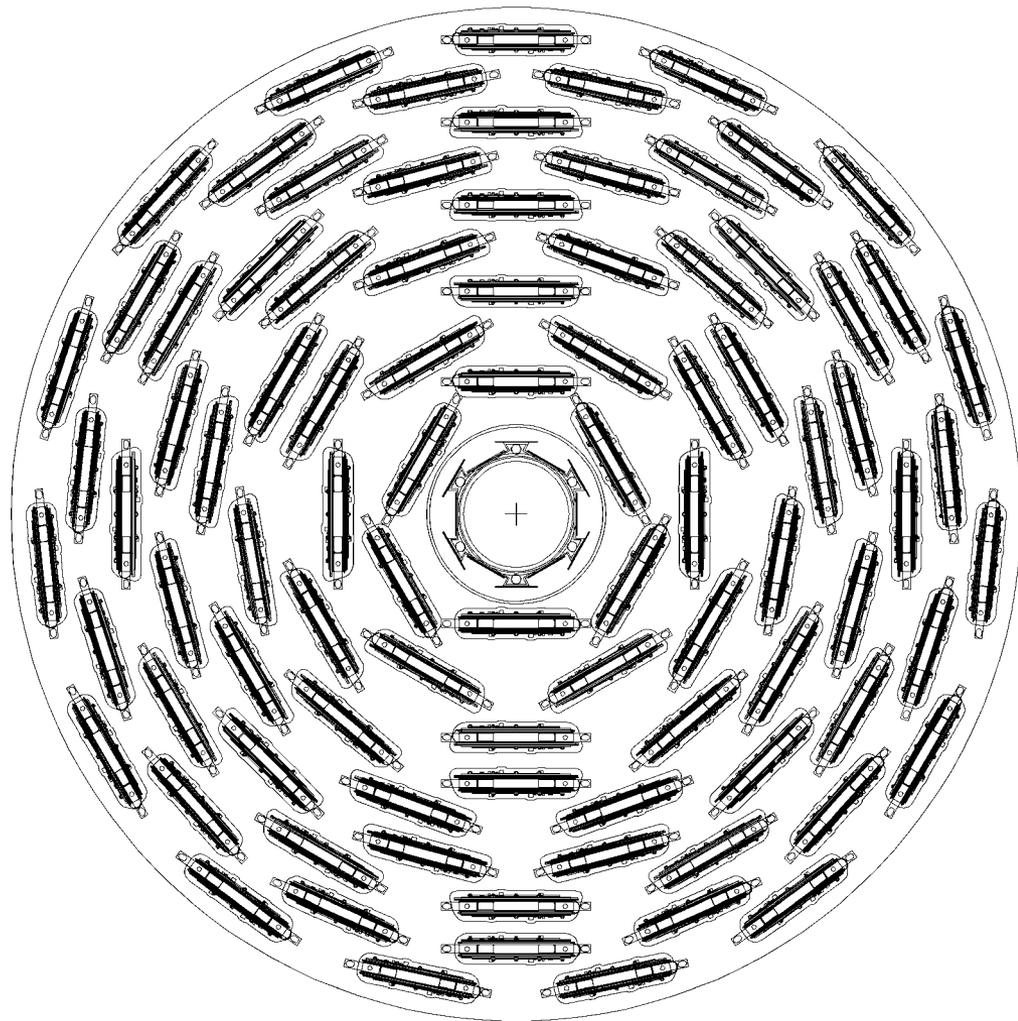
- **Design Goals:**

- Robust, simple, flexible and reliable design
- Minimize the cost
- Match or exceed performance of Run IIa silicon detector
- Minimize changes to infrastructure: DAQ or cooling systems
- Integrate CDF experience from SVX, SVX' and SVXII
- Pursue common solutions with D0:
 - **Svx4 chip**
 - **Technology of silicon**
 - **Direct cooling**
 - **Hybrid technology**
 - **L0 technology**



RunIIb Layout

- Final layout choices are the results of many internal reviews with inputs also from Laboratory committees.
- Main Layout Choices:
 - ➔ 6-fold symmetry
 - ➔ 1 stave design for all 5 outer layers
 - ➔ Fill all space available up to ISL
 - ➔ Maximum flexibility in the choice of Axial/Stereo layers
 - ➔ Innermost layer (L0) similar to the present L00





Run IIb Layout Details

Layer	Fold	Type	Radius (mm.)	pitch/RO (um)	angle	Sensors	Hybrids	#chips
0	12	Axial	21.0 and 25.0	50/25	0	144	72	144
1	6	Axial	35.5 and 43.5	75/37.5	0	72	36	144
1	6	Axial	40.0 and 48.0	75/37.5	0	72	36	144
2	12	Axial	59.5 and 74.75	75/37.5	0	144	72	288
2	12	Stereo	64.0 and 79.25	80/40	1.2	144	72	288
3	18	Stereo	90.75 and 104.5	80/40	1.2	216	108	432
3	18	Axial	95.25 and 109.0	75/37.5	0	216	108	432
4	24	Stereo	119.25 and 133.0	80/40	1.2	288	144	576
4	24	Axial	123.75 and 137.5	75/37.5	0	288	144	576
5	30	Axial	147.5 and 161.5	75/37.5	0	360	180	720
5	30	Axial	152.0 and 166.0	75/37.5	0	360	180	720
Totals						2304	1152	4464
Totals SVXII + L00						864	768	3276
Total Increase						267%	150%	136%
% outer layers						94%	94%	97%

94% of sensors and hybrids are 4-chip



RunIIb Layout

- Emphasys on simplicity and flexibility
- Easy to be mass produced
- Minimum number of parts:
 - 1 hybrid (4 chips)
 - 2 sensors (axial and stereo)

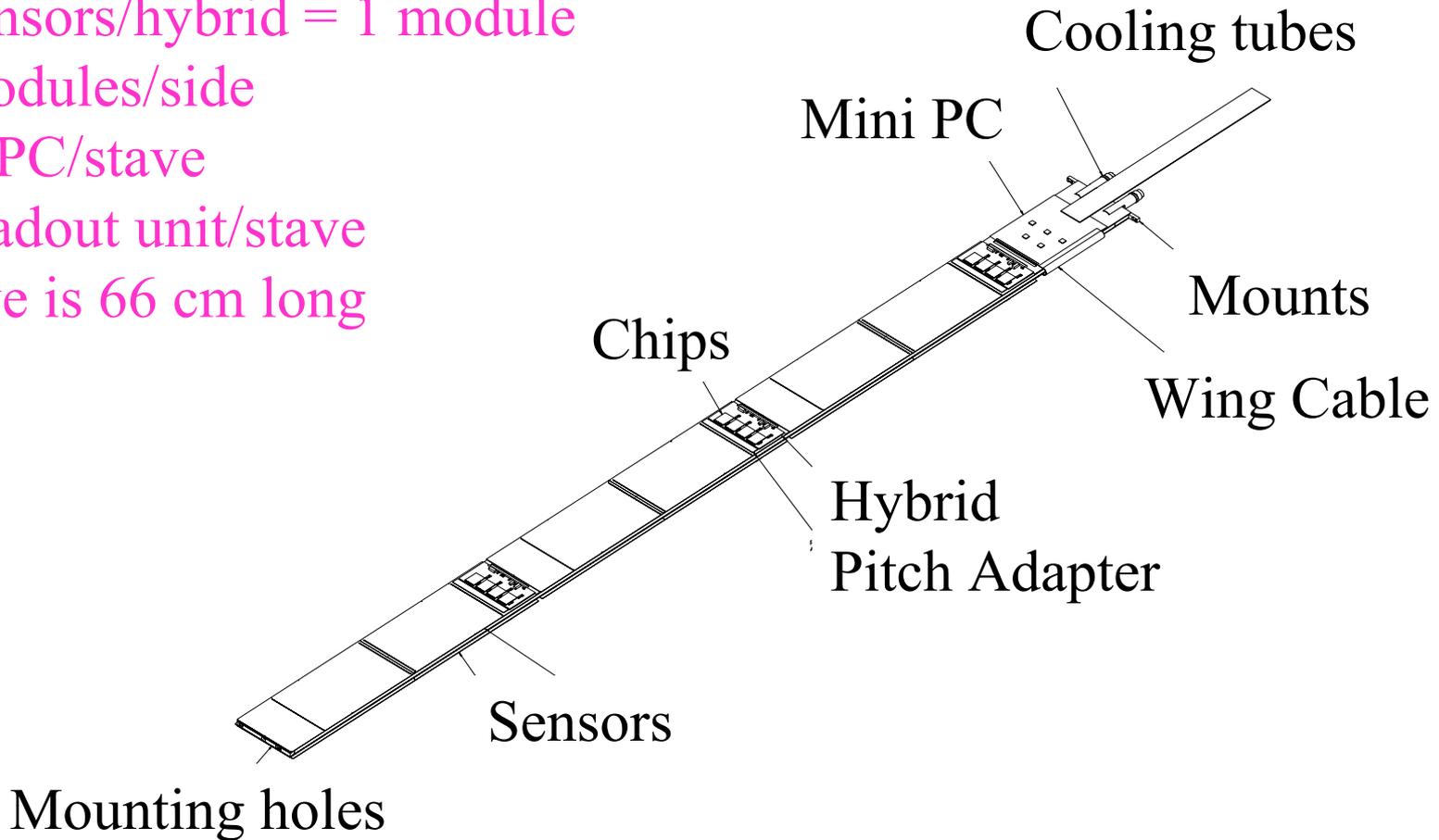
parts	SVXIIa	SVXIIb
hybrids	10	1
sensors	5	2
ladders	5	1

- Single stave design:
 - Minimize R&D
 - Minimize tooling
 - Minimize production time
- Carbon fiber bulk-heads with inserts for precision alignment of staves



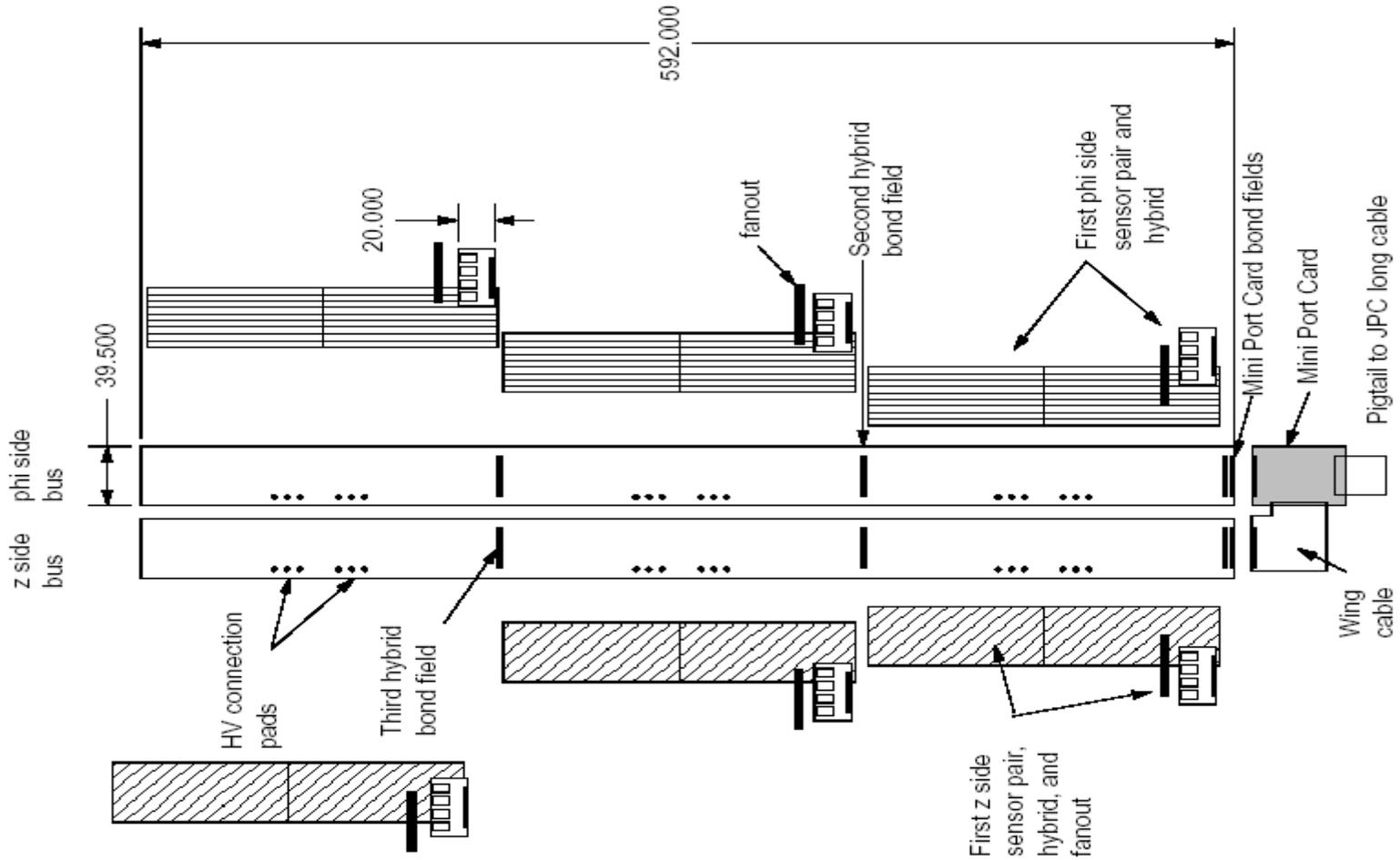
Stave: conceptual view

- 2 sensors/hybrid = 1 module
- 3 modules/side
- 1 MPC/stave
- 1 readout unit/stave
- Stave is 66 cm long



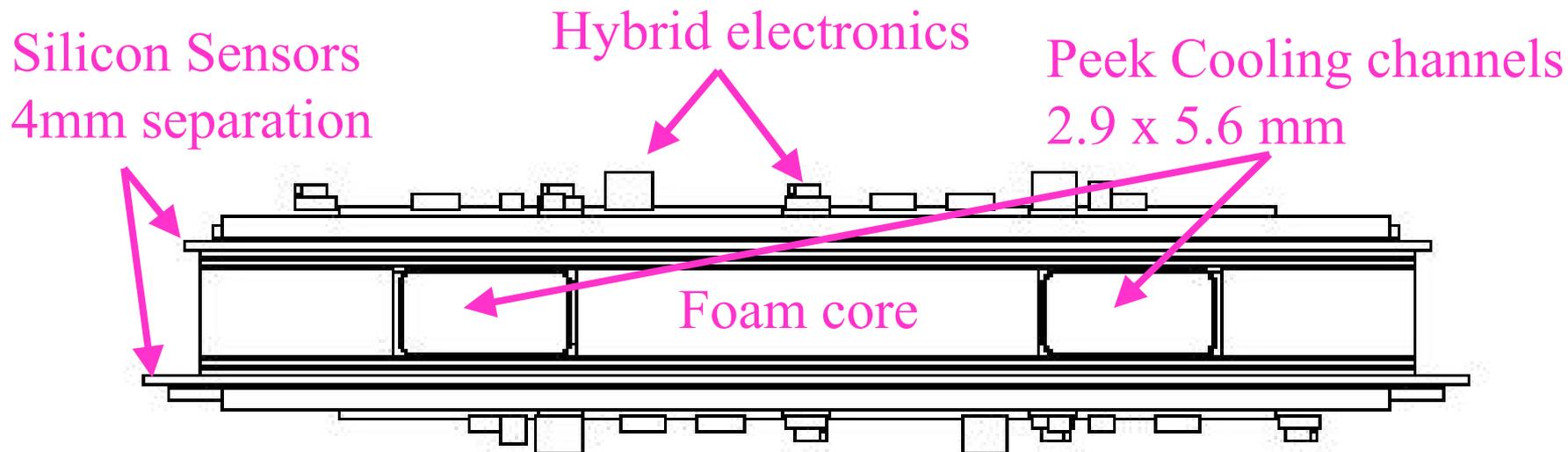


Stave: components





Stave: end view



Material/stave:

- 1.8% RL
- 124 grams

Fraction of Total RL:

- Sensors 39%
- Hybrids 13%
- Bus Cable 17%
- CF/Coolant 29%



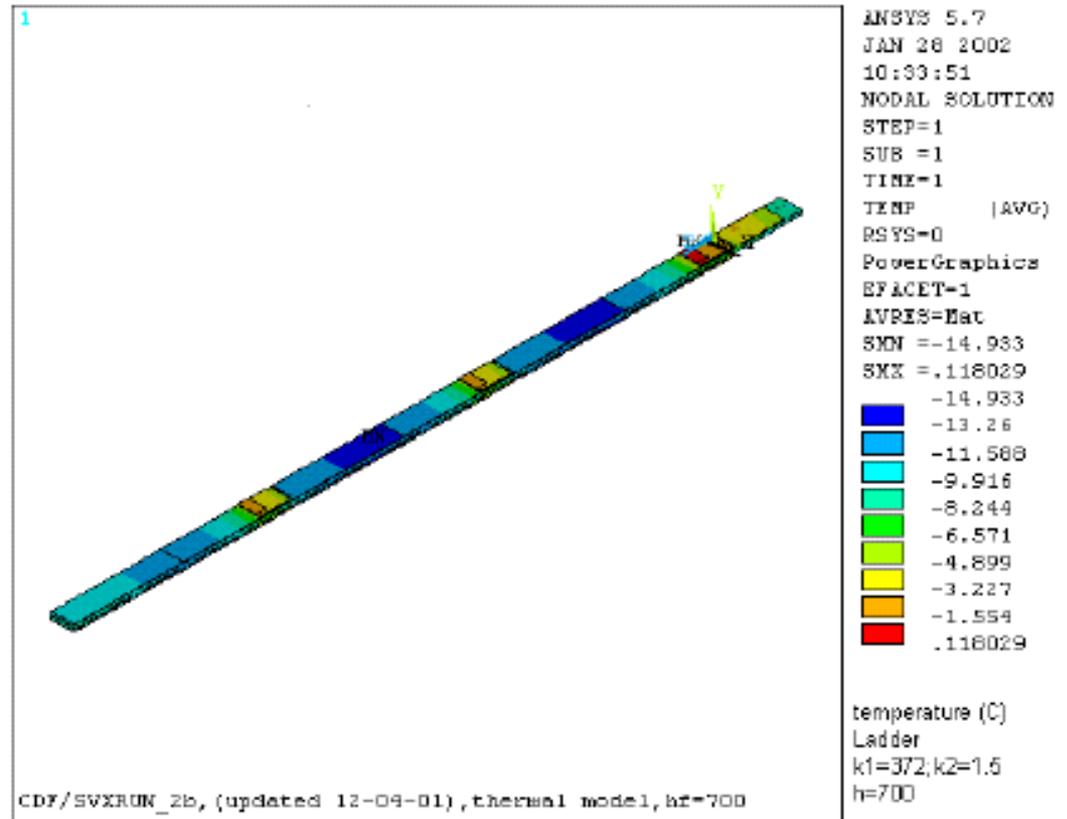
Stave: cooling issues

- Keep silicon cool to limit the amount of noise increase due to leakage current and limit the reverse annealing effect
- Studies of these effects set temperature limits:
 - Layers 4-5: $T < 15^{\circ} \text{C}$
 - Layers 2 and 3: $T < 10^{\circ} \text{C}$
 - Layers 0 and 1: $T < -5^{\circ} \text{C}$
- Requires active cooling of staves
 - Cooling tubes (Peek) integrated into stave structure
- Total heat load very similar to Run IIa $\sim 3 \text{KW}$
- Plan to use existing cooling system with increased glycol concentration (43%) for operation at -15°C



Stave: Cooling Studies

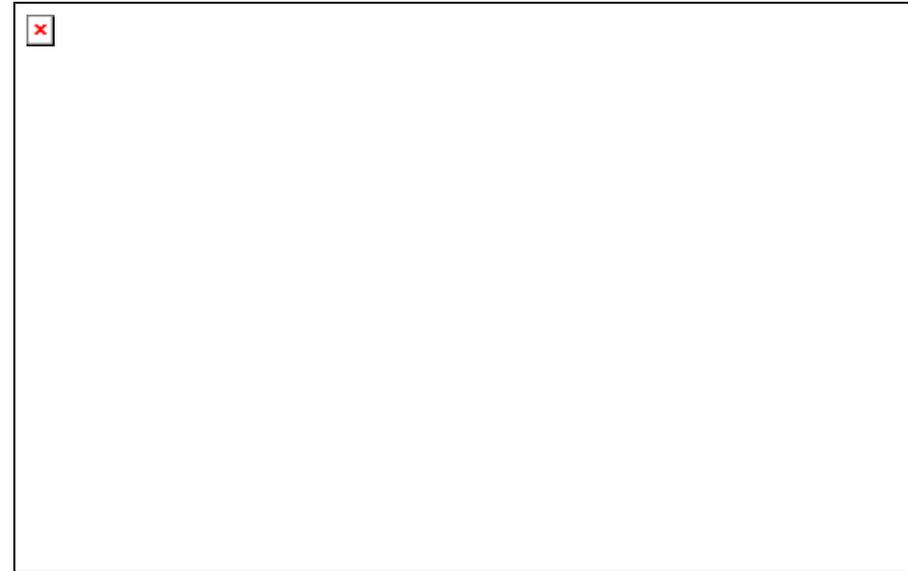
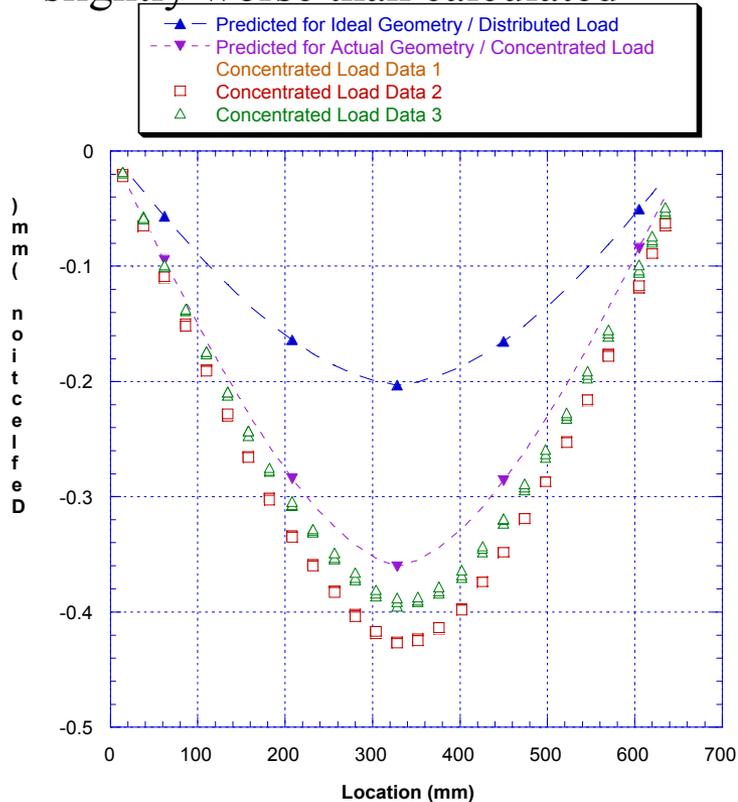
- Heat from chips is spread through BeO hybrid
- Then transferred through multiple adhesive layers, Silicon, bus cable, and CF
- Cooling tube is PEEK 0.1mm thick and 5.6 mm flat area
- Coolant T=-15C
- Convection to +10C gas
- Silicon temp < 0C everywhere
- **Important quantity is average over a strip:**
 - **Axial: -10C**
 - **Shortest Stereo strip: -4C**
- Measurements on prototype stave will be available in the next few weeks.





Stave: more studies

→ deflection measured on prototype stave are slightly worse than calculated

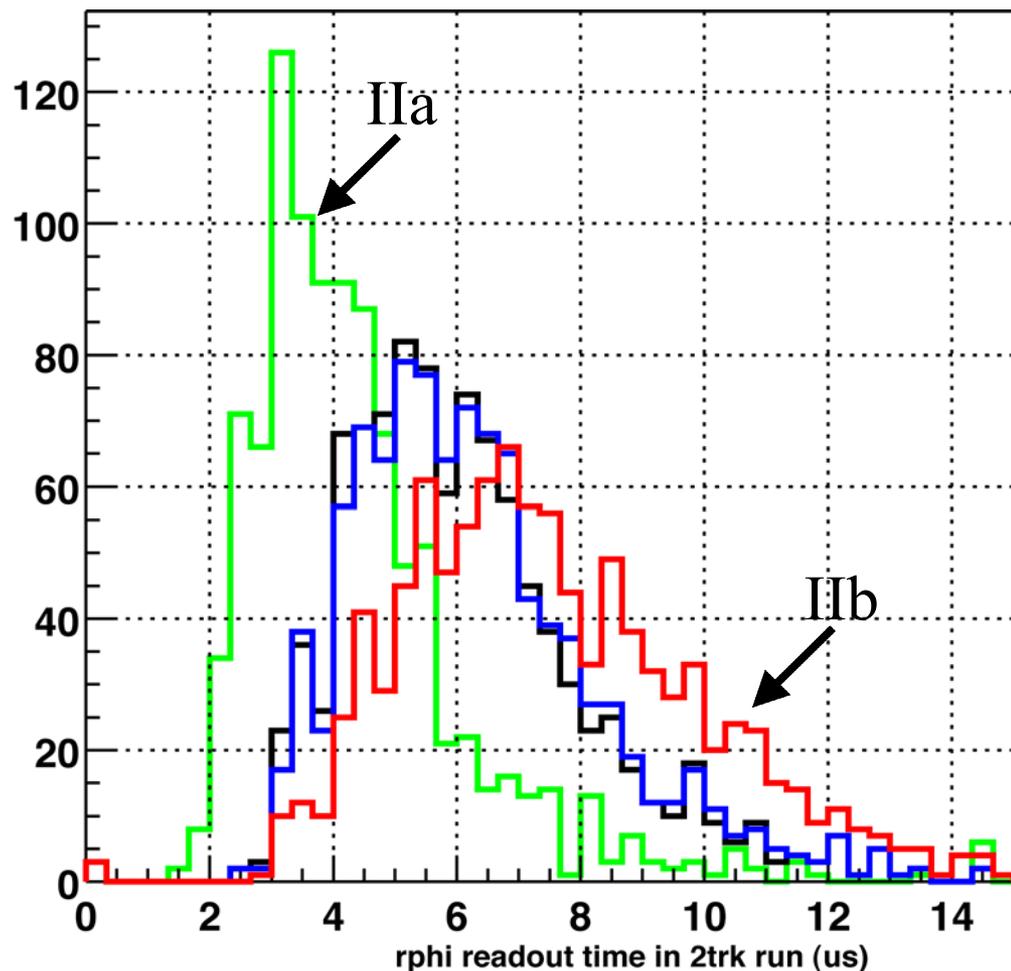


- Several stave core assemblies were fabricated
- Flow characteristics were investigated with coolant under two sets of conditions:
 - Near room temperature with modified coolant to try to match cold coolant properties [points shown in red – viscosity matching not well-achieved]
 - At -15°C with 42.5 wt.% ethylene glycol [hollow points]
- Pressure drop slightly higher than predicted₁₅



Stave: readout studies

- **Each stave is a single readout unit:**
 - Great simplification in the construction of the stave
 - Minimizes the number of cables and DAQ units
 - Worse case is for L1 (red in the histogram)
- Main concern is time required to feed SVT with silicon data which should be kept $< \sim 10\mu\text{s}$
- Studies using real Ila data scaled to match the I Ib configuration indicate that it should not be a problem

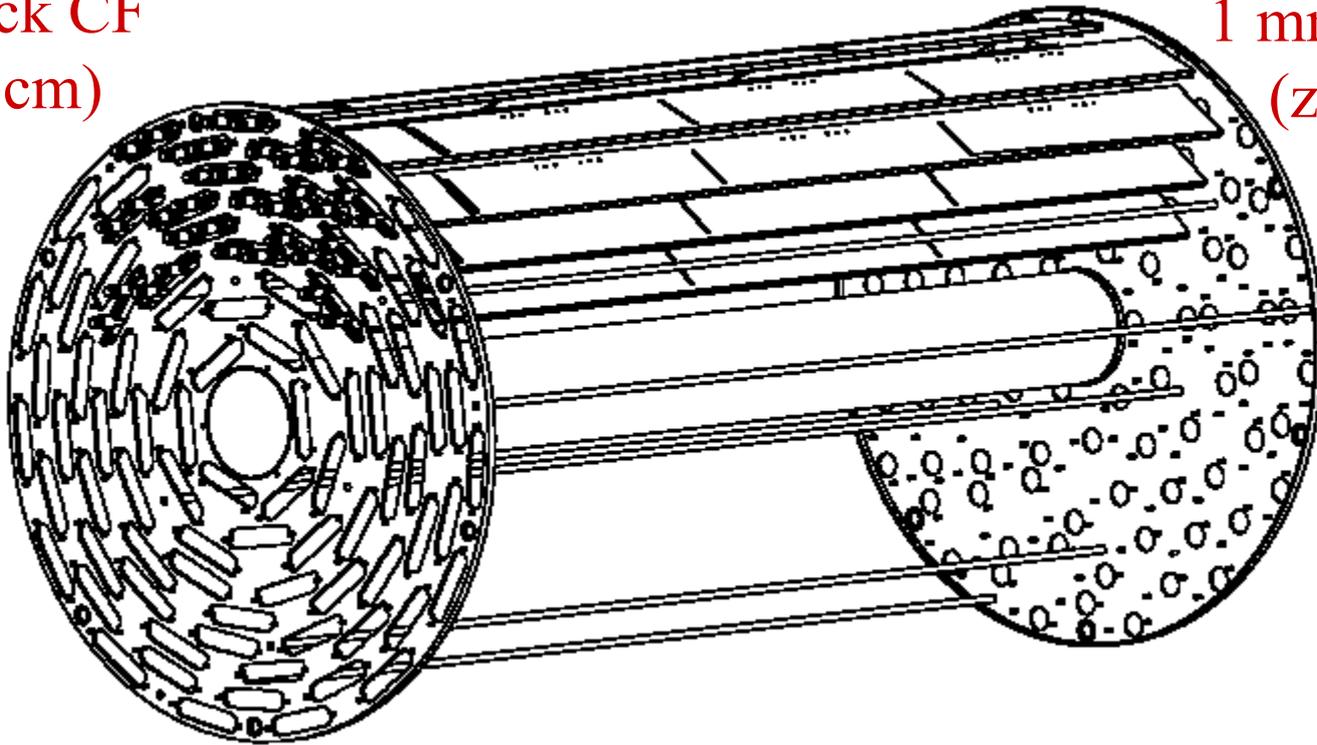




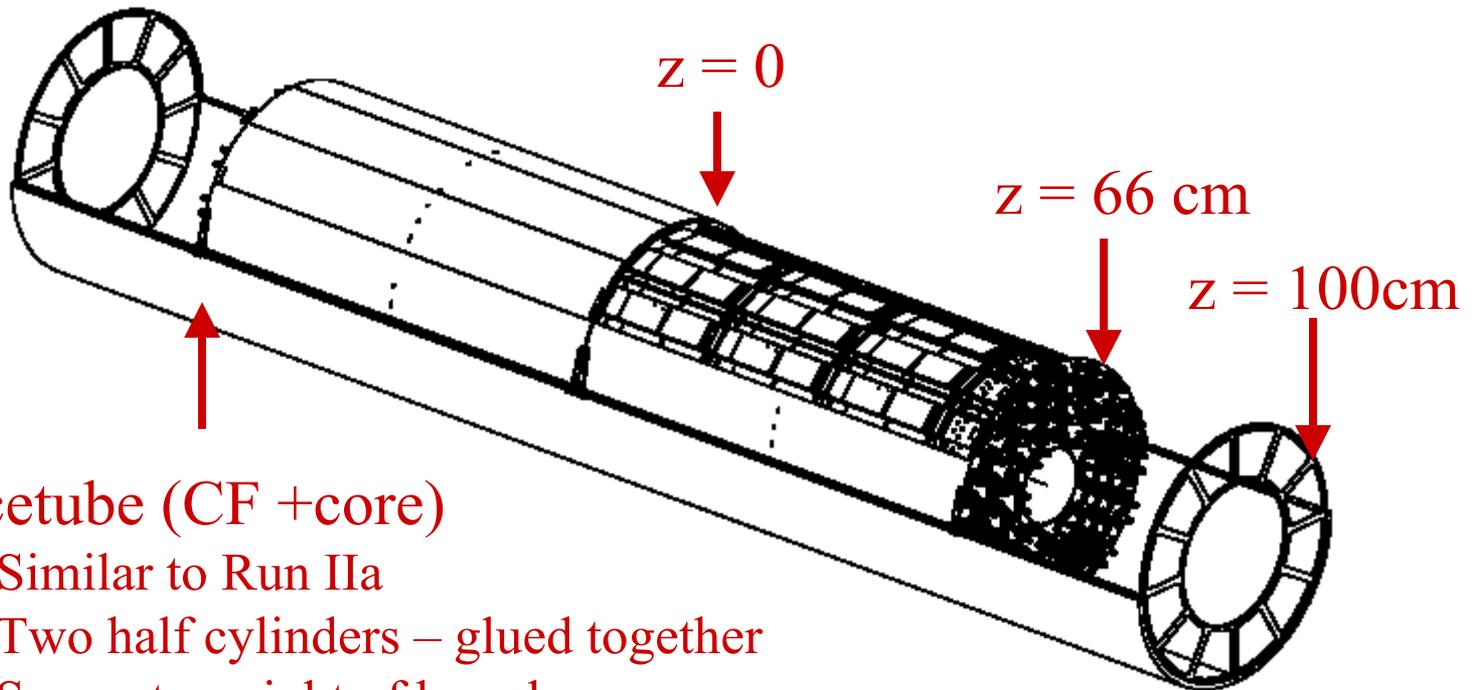
Barrel assembly

Outer Bulkhead
2 mm thick CF
($z = 66$ cm)

Inner Bulkhead
1 mm thick CF
($z = 0$ cm)



Barrel in Spacetube



Spacetube (CF + core)

- Similar to Run IIa
- Two half cylinders – glued together
- Supports weight of barrels
- Attaches to mount points on ISL end flanges



Run IIb Layout Summary

- Uniform stave (ladder) design for $\sim 94\%$ of the detector
 - ➔ L1-5 = 180 staves - only one set of fixturing to develop (SVXIIA had 180 ladders, 5 different sizes, 36 of each size)
 - ➔ L0 ~ L00 type construction
- Small number of different style parts
 - ➔ Only 2 types of hybrids – 4 chip on outer layers, 2 chip on Layer 0
 - ➔ L1-5 have 2 sensor types (axial and small angle)
 - ➔ L0 has 1 type of sensor (L00 in Run IIa had 2 types)
- Construction flexibility
 - ➔ Stave design independent of sensor type (axial-SA, or AA)
 - ➔ Rearrangement of layer types is possible



Run IIb Status –outer layers

- Our r&d effort pivots on the stave tests
- All stave prototype parts are in hand:
 - ➔ Prototype sensors
 - ➔ Prototype Hybrids
 - ➔ Prototype Bus cables
 - ➔ PCB version of the mini Port Card (BeO version expected at the end of August)
 - ➔ Prototype stave cores
 - ➔ Prototype module fixtures are ready and tested
 - ➔ DAQ system ready
- Main point is to verify the noise coupling between the Silicon and the Bus Cable.
- **Expecting results in early October**



Stave: noise studies

- Sensor pick up noise from the bus cable has been studied using svx3d equipped hybrids and a PCB version of the bus cable.
- Many different configurations studied (see figure)
- Noise structure is understood and controlled to tolerable level.
- Need to repeat these measurements with real stave and the svx4 chip

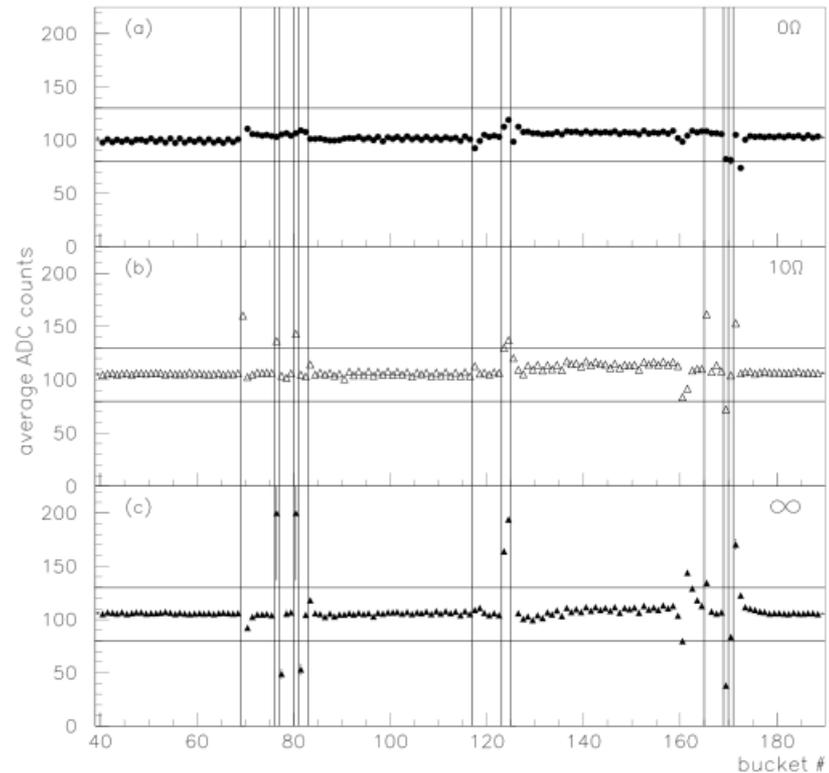


Figure 12: Pedestal values in ADC counts vs. bucket number for different grounding schemes of the aluminum shield: (a) $0\ \Omega$ to AGND (b) $10\ \Omega$ to AGND; (c) floating shield. All measurements are obtained using the mock stave with two sensors.



Silicon Sensors

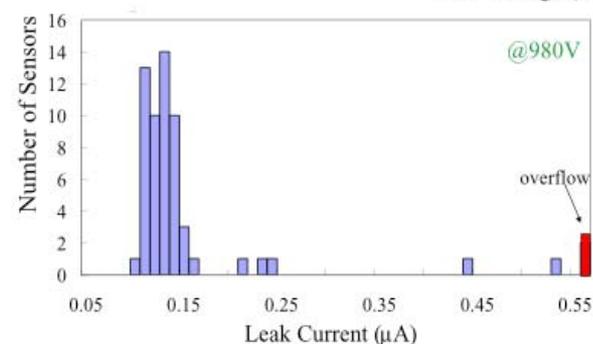
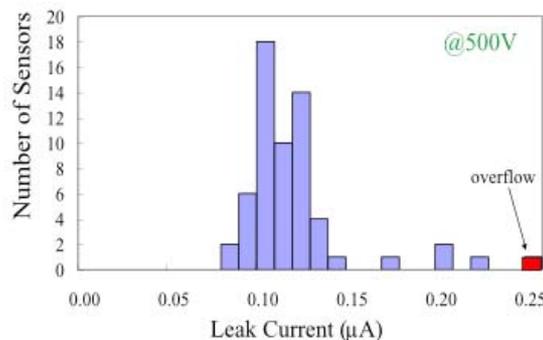
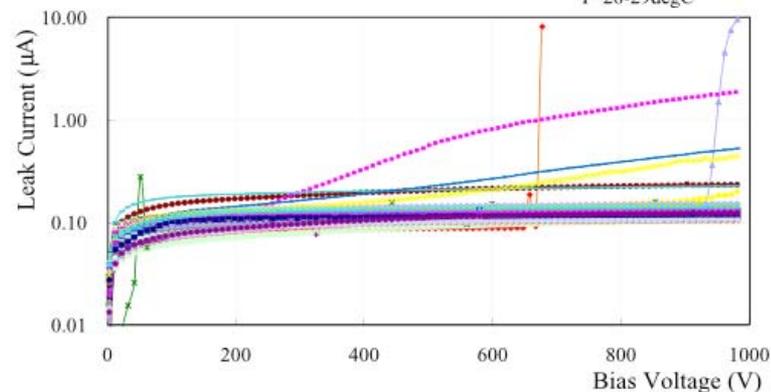
- All detectors are single sided and based on the high voltage operation layout (CMS, ATLAS, L00)

- ➔ Easy to build, test and handle
- ➔ Minimal R&D necessary
- ➔ High yield and a minimum number of problematic channels is expected (<1% in most of the detectors)
- ➔ Prototype (identical to final sensors) already in hand
- ➔ 0% bad channels for grade “A” and 0.07% for grade “B”

SVX2b Outer Axial Sensors (Hamamatsu Photonics)

I-V curves of 60 prototypes, measured by U Tsukuba

2002.7.16
T=28-29degC





SVX4 chip

- **Design Team:**

- **LBL:** Brad Krieger (lead designer), Jean-Pierre Walder (ADC), Henrik von der Lippe (I/O pads), Emanuelle Mandelli (full chip simulation)
- **FNAL:** Tom Zimmerman (preamp & pipeline), Jim Hoff (pipeline logic)
- **U. of Padova:** Stefania Alfonsi (FIFO)

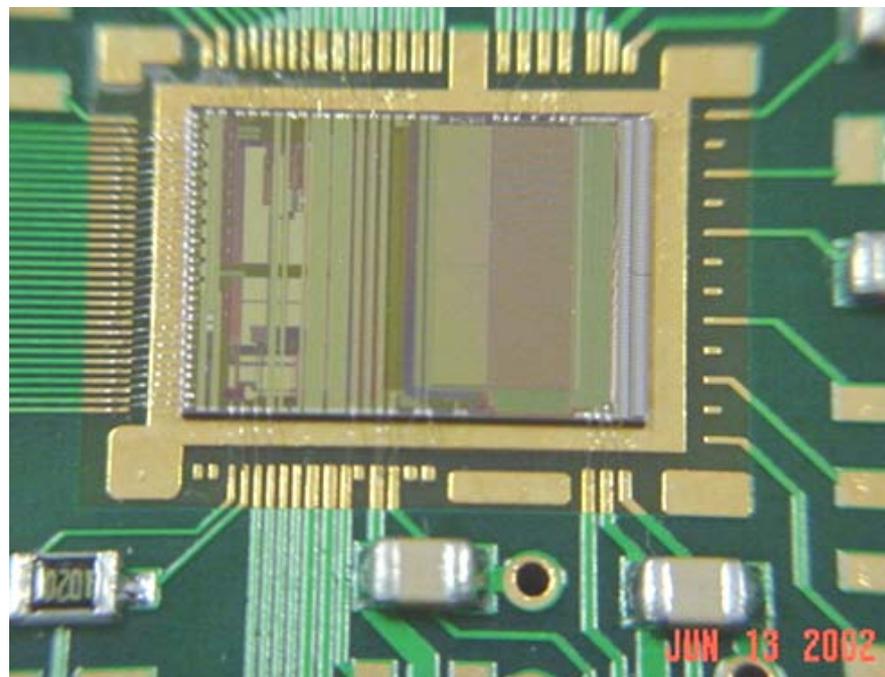
- **Timeline**

- **July 2000:** First SVX4 proposal meeting following studies at LBNL
- **May 2001:** Common CDF/D0 specifications supplied to designers. Preliminary design review.
- **October 2001:** Final Design Review
- **April 2002:** Design submitted for fabrication
- **June 10, 2002:** Wafers delivered to FNAL
- **June 12, 2002:** First chip tested at LBNL, basic functionality verified.



SVX4 chip: Results (1)

- **No serious problems found after 2 months of testing**
(radiation tests still needed)
- **SVX4 as-is could be used to build a detector.**
(assuming no radiation problems)
- **Minor adjustments desirable to declare it a production chip**
 - Eg: set chip ID MSB for full compatibility with existing DAQ.
 - Eg: correct slight pedestal structures, which one could work around, but it's better to fix them.

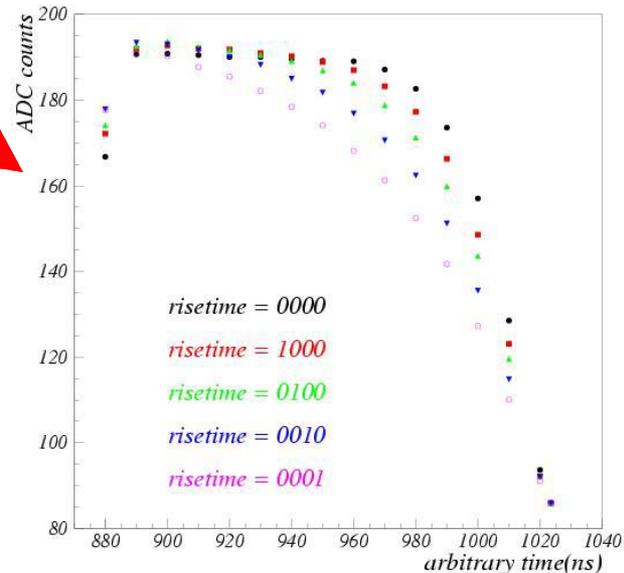
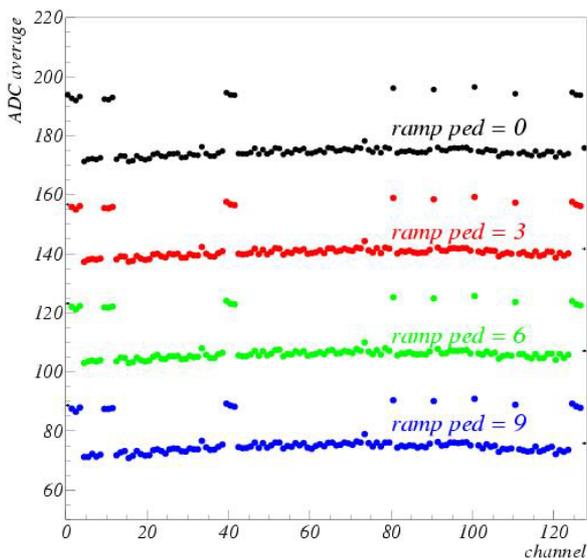




SVX4 Chip: Results (2)

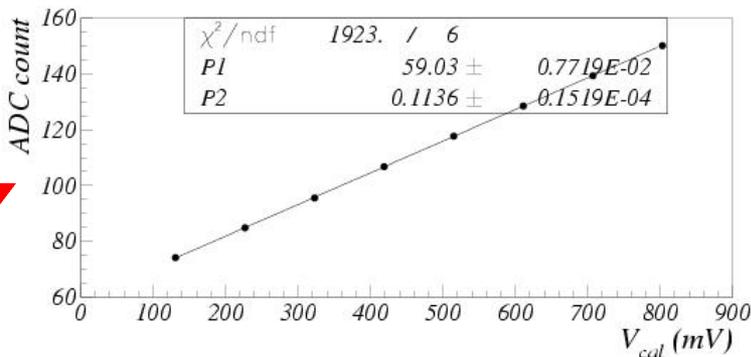
Preamp rise time measured using own chip's ADC agrees with simulation & meets specs

Pedestal adjustment and charge injection work as expected. Slight pedestal structure is understood and can be corrected.



Noise performance meets specs (<2,000e for $C_i=40\text{pF}$)

ADC linearity better than specs



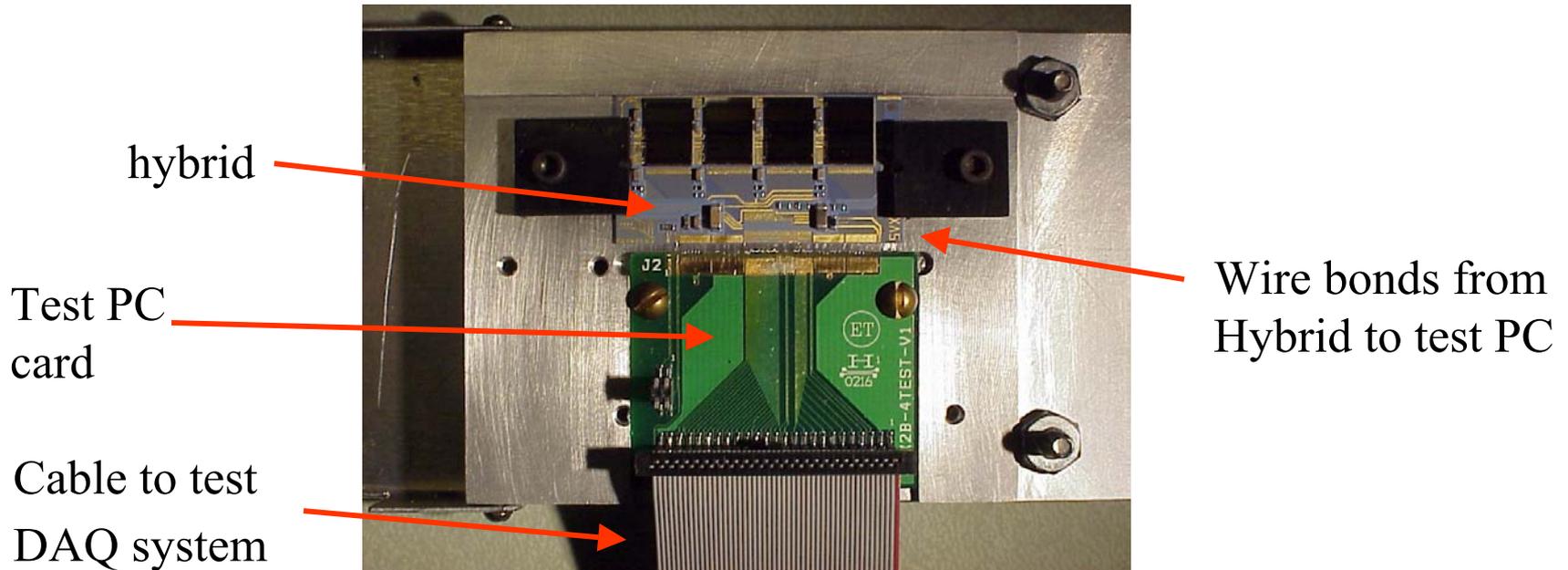


Hybrids

- Only two types of hybrids:
 - ➔ Outer stave layers use a 4 chip hybrid ~1200 required
 - ➔ Layer0 uses a 2 chip hybrid , 72 required
- Both types of hybrids are fabricated on a Beryllium Oxide substrate for improved thermal performance and long radiation length.
- Hybrid layout uses advanced fine pitch technology for reduced area.
- Integrate SVX-II (a) experience into design, materials choices, and components to enhance reliability and simplify fabrication, assembly, and test.
- 4 chip hybrid prototype has been fabricated, 45 parts received
- 12 parts are in various stages of assembly, 4 have undergone basic electrical tests.
- Hybrid appears to work with no apparent problem seen yet.
- **SVX4 chip performance on hybrid same as single chip on test board.**



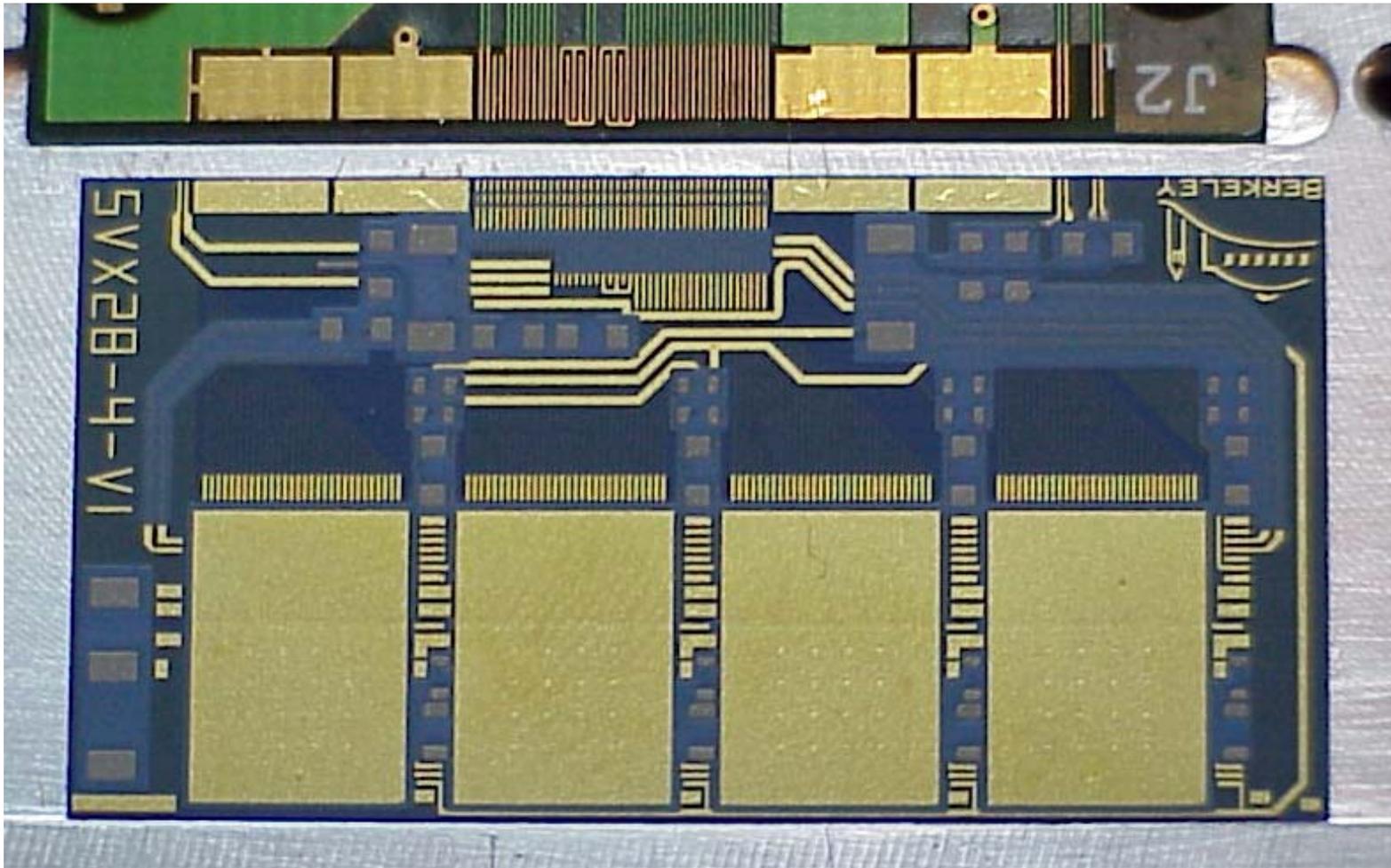
Hybrids: 4 chip hybrid



- Hybrid is bonded and tested on holder plate. Interface is through test PC card (green) which replaces bus cable during test and assembly.

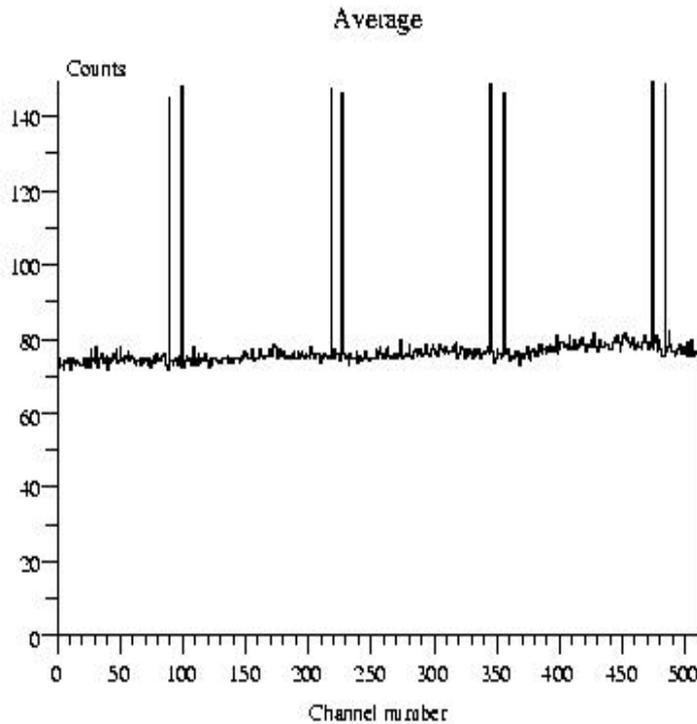


Hybrid: Detail showing bond pads





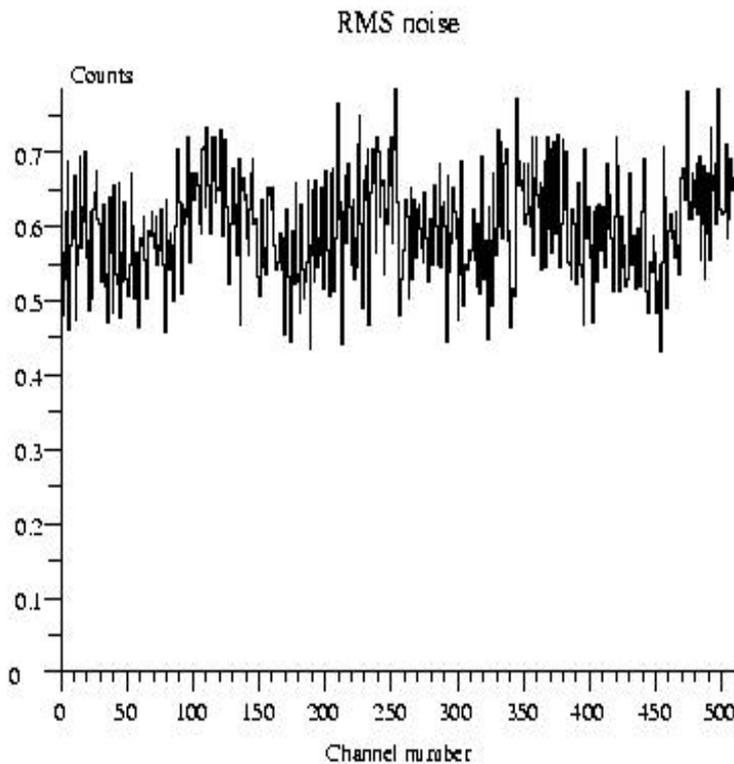
Hybrid: Performance (1)



- Plot shows pedestals for $4 \times 128 = 512$ channels.
- Pedestal level set at initialization.
- High channels have charge injection set by mask register.
- MIP ~ 20 counts



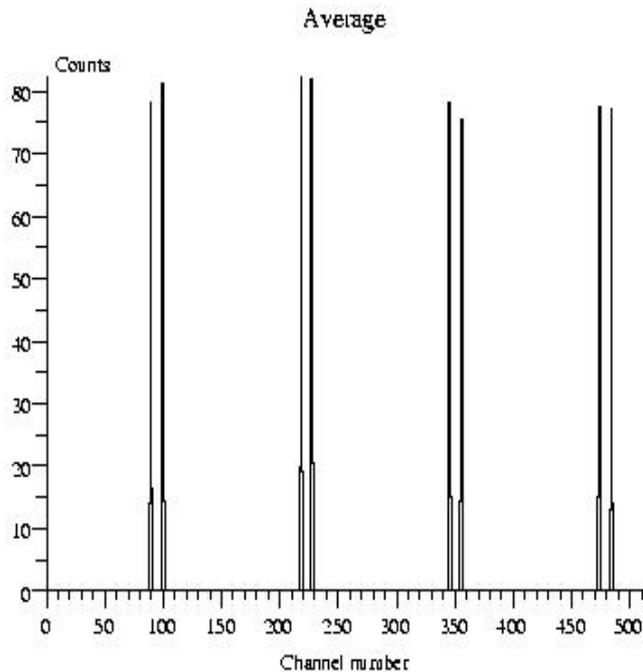
Hybrid: Performance (2)



- Plot shows noise for 512 channels
- Similar noise and gain seen on 1 chip test board ~ 700 electrons
- Noise and Dnoise are the same
- Structure (small) may be related to voltage drop effects already studied for comparators.



Hybrid Performance (3)



- Pedestal distribution for 512 channels with real time (dynamic) pedestal subtraction feature & read neighbors feature activated.
- High channels have charge injection present. Neighbors at ~10 counts.
- Present circuit sets pedestal at 10 counts.



Hybrid: L0 and further plans

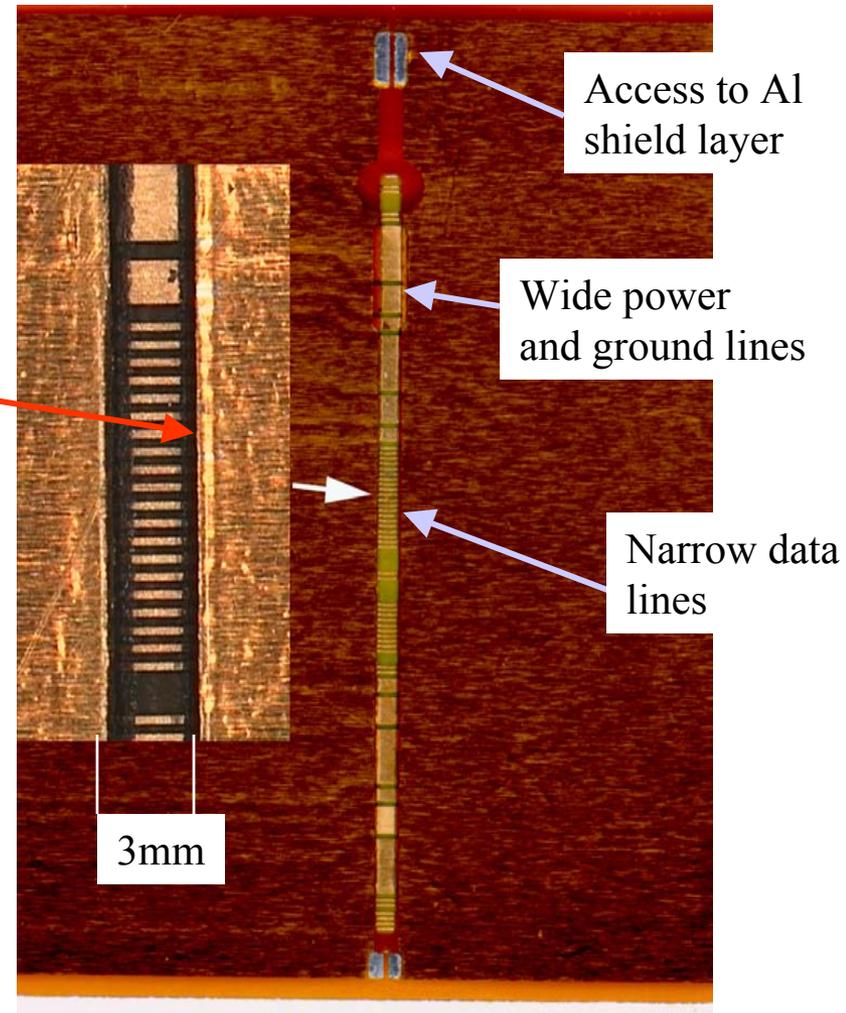
- L0 Hybrids:
 - 2 chip hybrid for Layer 0 has similar design to 4 chip version.
 - Each L0 hybrid is a single readout unit and has a transceiver chip mounted on the hybrid itself (no mini port card for L0)
 - First complete set of prints completed on designed and under review. Expect a few weeks to revise and prepare for prototype submission.
 - parts available in the fall.
- Further plans:
 - complete assembly of additional 4 chip hybrids.
 - These will go to FNAL for integration into silicon and to test staves.
 - Validation of assembly process is under way at LBL.
 - Search for other potential vendors/assemblers is under way.
 - Some small revisions under study to facilitate assembly and test in production.



Stave Bus Cable

- Data and power are provided to hybrids by the laminated stave bus cable.
- Construction is a sandwich of kapton, Copper, and Aluminum, with Gold plated regions for bonding to the hybrid.
- Bus work has very fine pitch (3 mil lines).
- A set of cables were completed by vendor (Cordova) and some problems were found, BUT:
 - ➔ A few cables are good for stave construction
 - ➔ No problem with lithography and fine line work.
- Work underway to address remaining problems
- A second suitable vendor (Altaflex) has also been contacted and a prototype run is planned there soon.

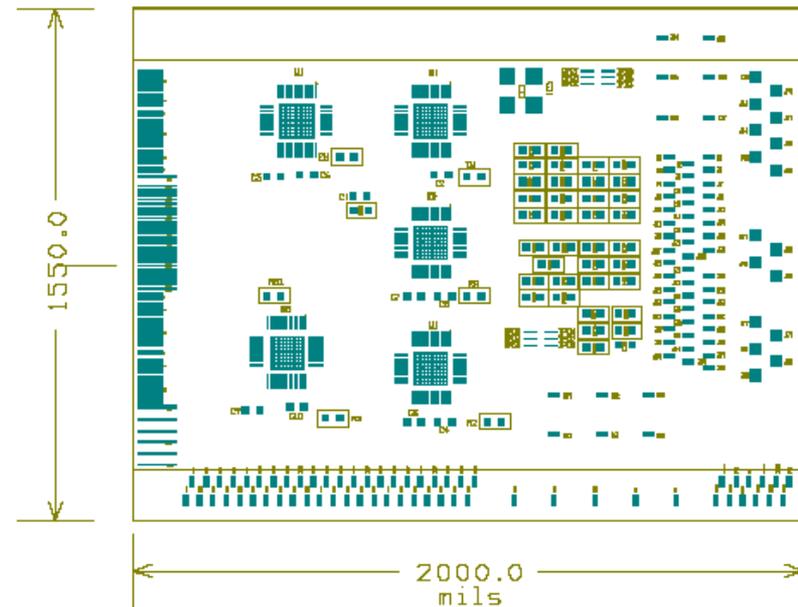
Magnified view





Mini Port Card

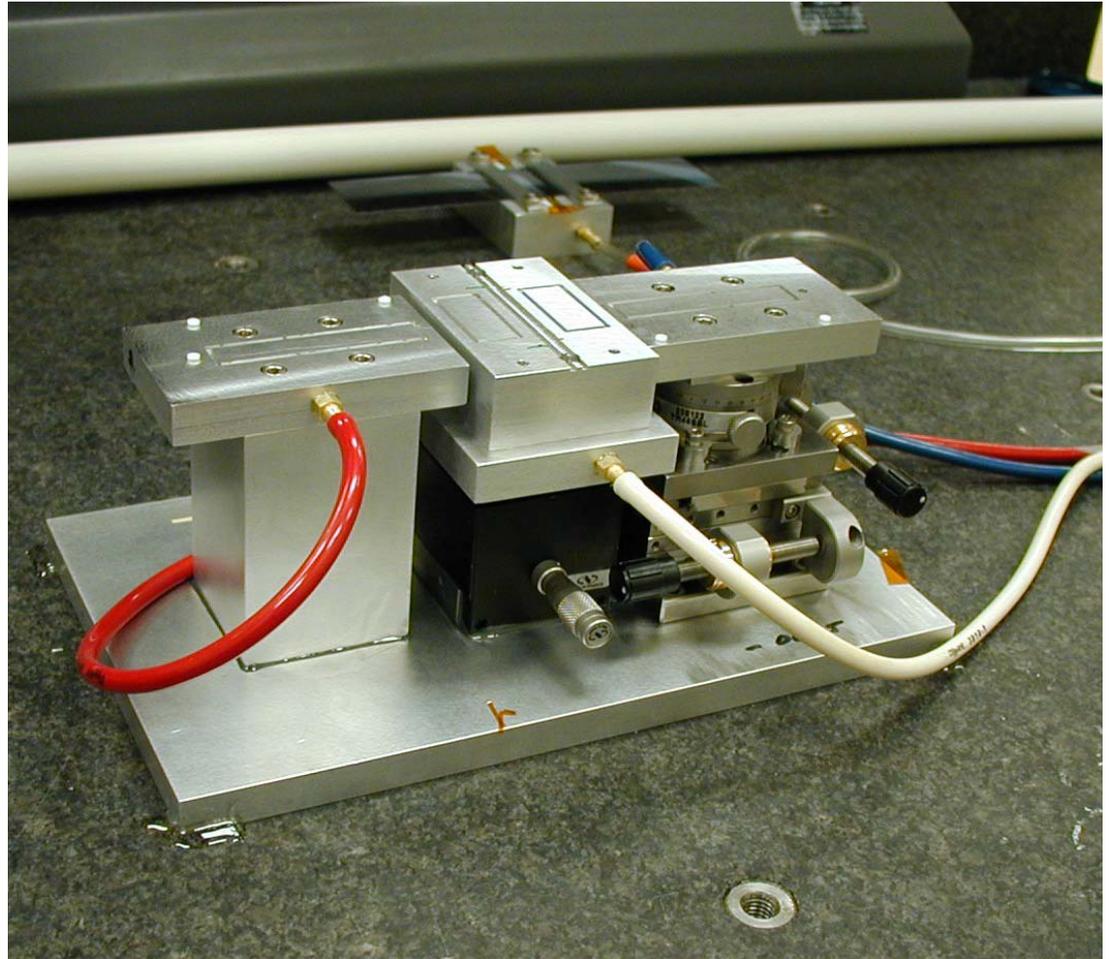
- Uses the same BeO substrate as the hybrid
- Connects to the top and bottom bus cable (directly and via a foldable “wing” cable)
- Controls all data, commands and power going in/out of the stave
- An FR4 version has been produced to allow start of electrical stave tests.
- BeO prototype expected by end of August
- 5 transceiver chips are mounted for data control
- Transceiver:
 - ➔ A new (0.25um) transceiver chip has been designed and submitted to MOSIS
 - ➔ New transceiver simplifies connectivity and eliminates the need for an extra power line
 - ➔ New transceiver fits in the silicon space left over by the svx4 chip
 - ➔ MPC is also compatible with the old transceiver which we have already plenty left over from IIa





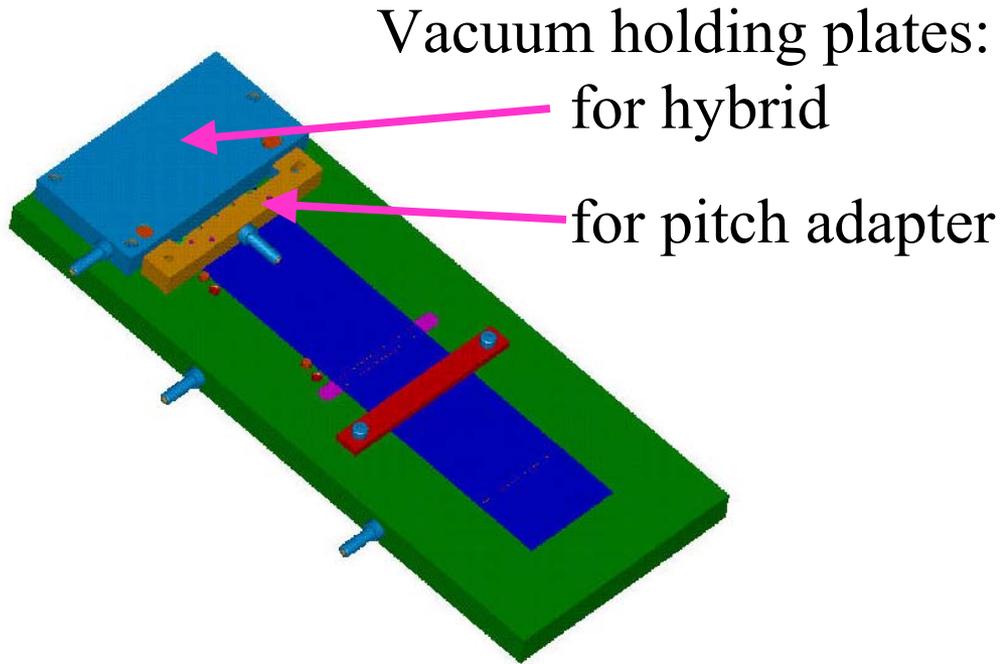
Sensor to sensor gluing fixture

- Similar to L00 style fixtures
- Sensors under vacuum
- Glue applied to area on center block
- Center block is raised to meet sensors
- Block + sensors can be removed for curing
- Frees up fixture for a new module
- Tests found that sensor position is very stable
- Assembly process is fast and reliable

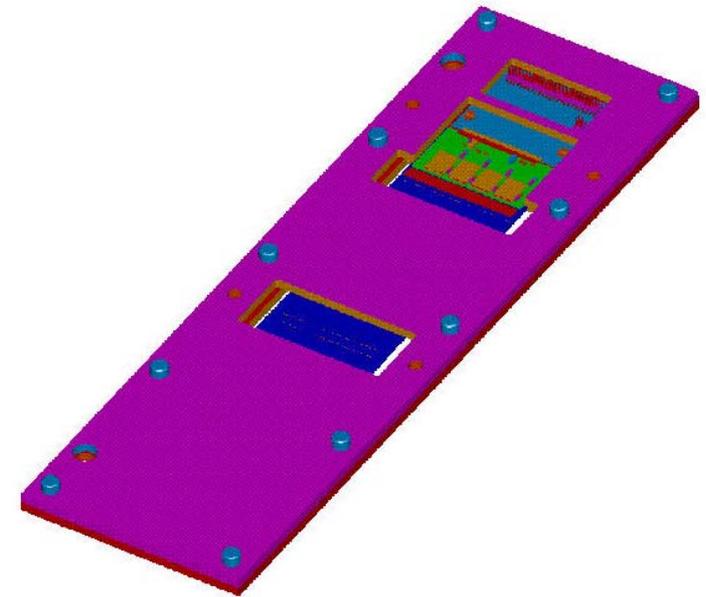




Other outer layer module fixtures



Hybrid and pitch adapter
gluing fixture



Module storage frame



Layer 0 Design

- Inner Layer (L0) follows Run IIa L00 design:
 - ➔ Smallest possible pitch – 25/50 micron pitch
 - ➔ Fine pitch cables connect sensors to hybrids
 - ➔ Hybrids are located out of tracking volume ($\sim z=70\text{cm}$)
 - ➔ Positioned at small radius (2.1 cm)
 - ➔ Hybrids \sim similar to outer layer, but 2 chips
 - ➔ Will be supported by outer barrel (not beampipe)
- Low mass construction is of utmost importance for 1st measurement
- Sensors are identical to L00 sensors
- Cables:
 - ➔ All cables designed and the longest has been fabricated by KeyCom (Japan)
 - ➔ Some technical issues with the L0 cable sorted out BUT yield must be improved
 - ➔ We are pursuing other possible vendors with also the option of splicing the cable.



L0 Layout

Fine pitch cables

- Max. length 59cm
- 100um pitch
- 50um pitch at ends

Hybrids

Cooling tubes

Sensors

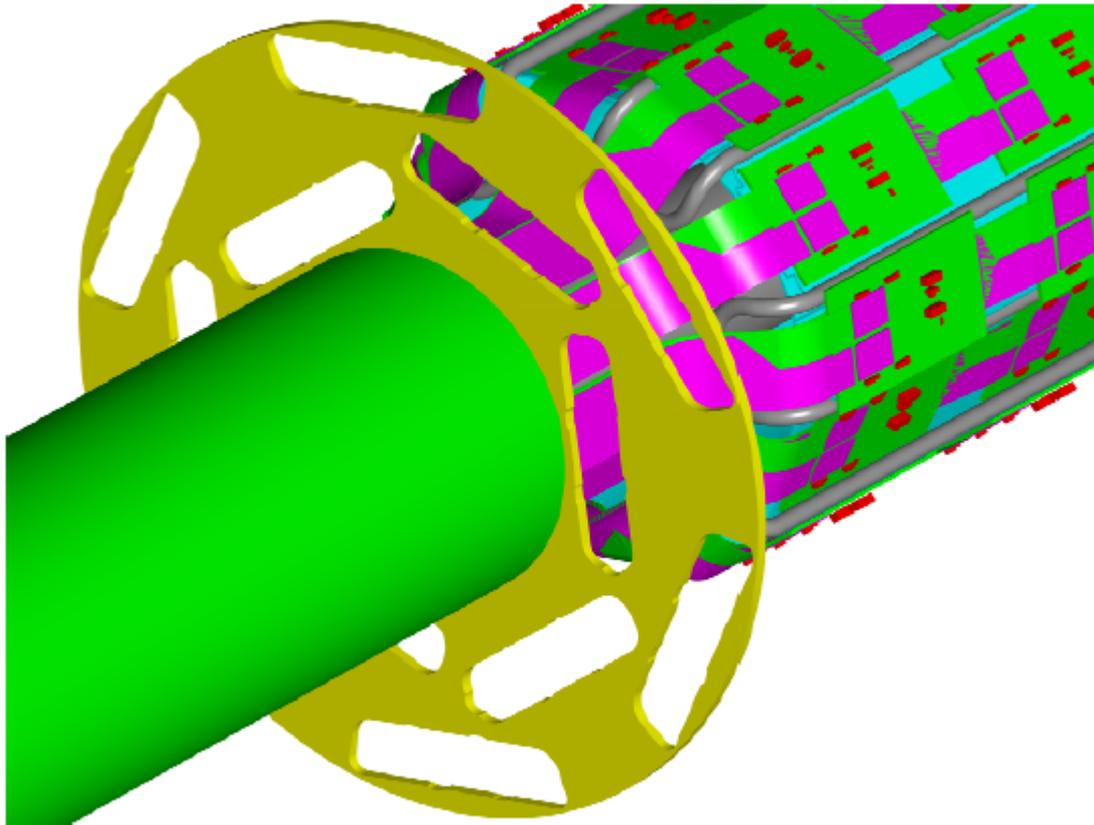
L0 Module -

2 sensors + Fine pitch cables
+ one hybrid = one readout unit

Beampipe and CF support



L0 hybrids and cables



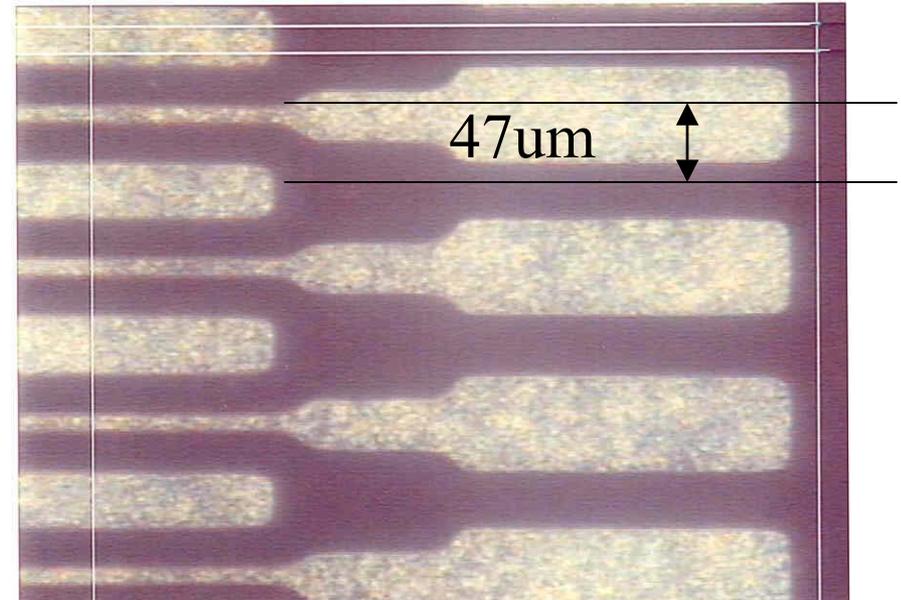
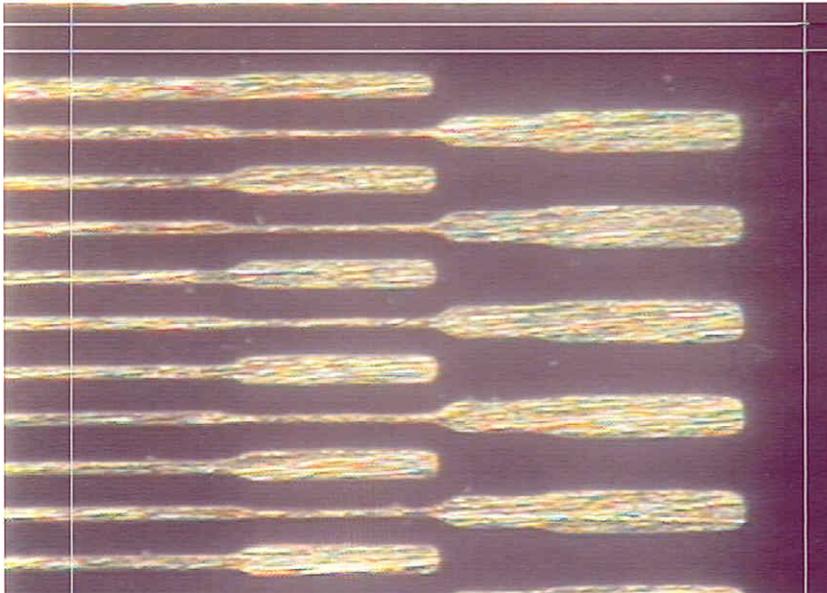
Cable flare out in radius (to $\sim 4\text{cm}$) after passing through bulkhead

Cables from successive modules pass underneath hybrids from lower z modules

Cooling tubes integrated into hybrid support structure



Layer 0: cable



- ➔ Finest pitch is 47um. Substrate is Upilex (50um)
- ➔ New gold deposition process now makes wire bonding acceptable
- ➔ Yield at KeyCom is still a problem
- ➔ We are in the process of contacting other vendors (Dyconex, Altaflex)



DAQ Changes from Run IIa

- ➔ New chip requires changes in front end of DAQ: 2.5V instead of 5V
- ➔ Optical components unavailable and not rad hard:
 - New mini portcards (smaller, minimal active components)
 - New Junction Port Card (now mounted outside the detector => accessible!)
 - New Fiber Transition Modules (with standard electrical TX/RX)
 - Copper cables are outside tracking region - off end of staves
 - A “copper” version of the test stand has been setup and tested!
- ➔ New Power Supplies: off-the-shelf, not custom
- ➔ Number of readout chains (252) much lower than available in existing infrastructure (408):
 - more spare parts will be available ! (important to cope with possible obsolescence of components)
- ➔ SVT can be made to work with Run IIb layout
 - Modifications similar to those already made for L00



Conclusions

- Great effort put into design simplification, ease of construction and low risk technology
- Design relies heavily on experience with previous silicon detectors at CDF (SVX, SVX', SVXIIa, L00 and ISL)
- We expect the total mass in the tracking volume to be below the present value in spite of the increased number of sensors and need for direct cooling
- DAQ simplified, active components are more accessible
- Final testing effort with prototype parts efforts is underway
- Very soon results will be available