



TDC Modification Plans

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January 18th, 2005

Director's Review of CDF Run IIb Upgrade



Outline

- Basic TDC operation
- Advantages of fast-clear capability
- Number of boards requiring modification
- Board modification details
- Project organization
- Schedule
- Labor and cost estimates



Basic TDC Operation

- On L1 accept, each TDC chip (96 total) latches 2 μ s of hit data from corresponding input channel.
- On L2 accept, the on-board DSP reads out the hit data sequentially from the buffers in all 96 TDC chips. The DSP formats the hit data and writes the output into an on-board FIFO accessible via VME.
- The VME crate processor sequentially reads the output data from the on-board FIFOs of all TDC boards within a crate (15-17 boards/crate in COT).



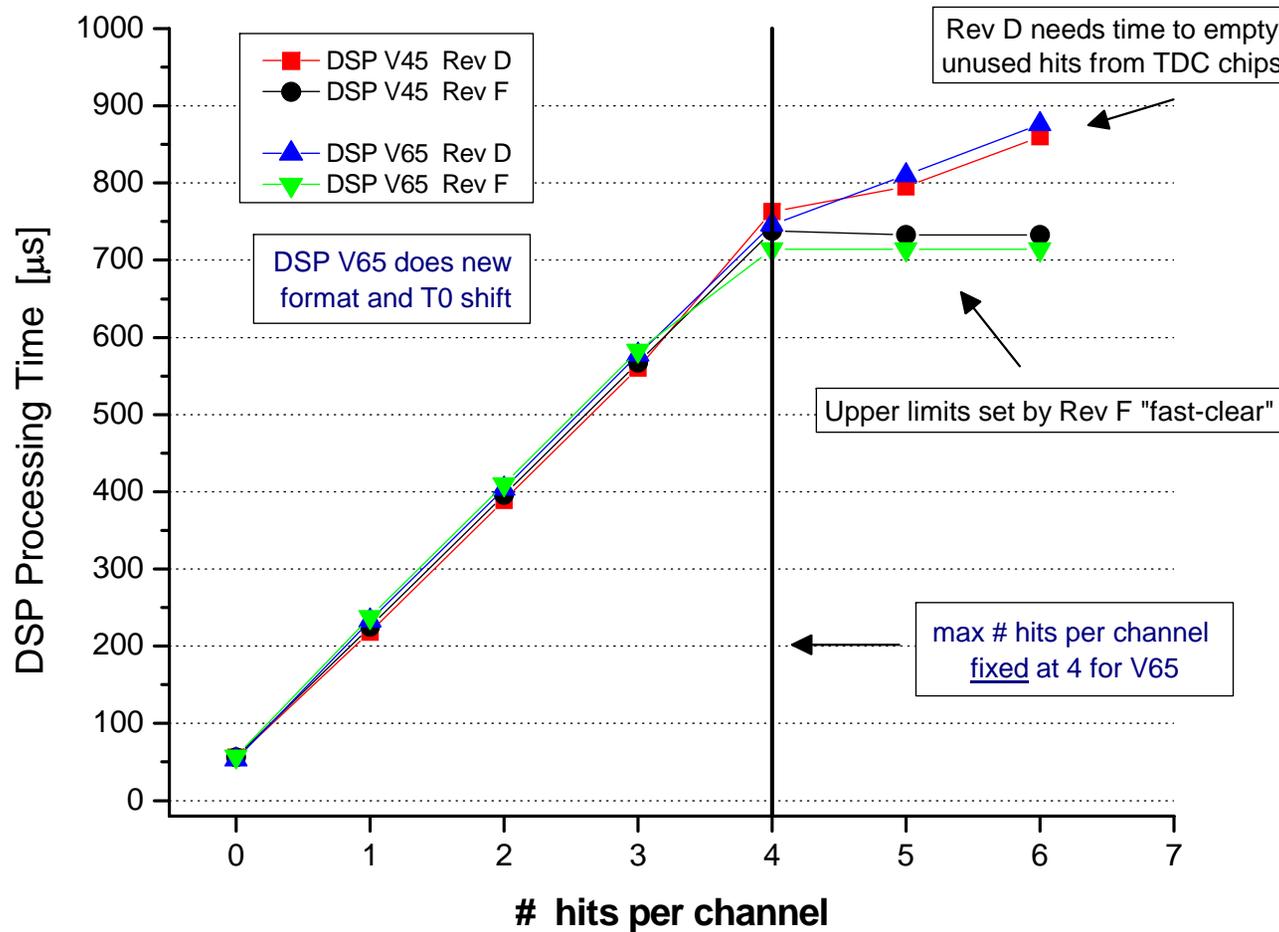
Basic TDC Operation

- The overall readout time for a given TDC crate is determined by the slower of the DSP processing time or the VME readout time which are designed to overlap for sequential events.
- The crate DSP processing time is determined by the processing time of the slowest TDC board in the crate.
- DSP processing time is directly related to the number of hits recorded in the $2 \mu\text{s}$ buffers of each of the 96 TDC chips.



DSP Processing Time

DSP Processing Time vs # hits per channel





Advantages of Fast-Clear

- Since the valid time window for COT hits corresponds to only the first 500 ns of the 2 μ s TDC chip buffers, the time for DSP processing can be reduced if the back end of the buffer which corresponds to hits associated with other interactions can be cleared without having the DSP read out each hit in the buffer.
- The newer Rev. F TDC boards include this functionality by default, but the older Rev. D TDC boards require modification.



Review Committee Recommendations

From Run IIb TDC review committee report (9/28/04)

- CDF should immediately begin modifying spare TDC boards with the fast clear option. The installation of modified boards can be staged, but it is important to understand the scope, timescale, and success rate of this modification.
- To improve the spares pool, consideration should be given to the feasibility of modifying all Rev. D TDCs with the fast clear option.



Current Distribution of COT TDCs

COT Superlayers	Number of Boards	Board Types
1-4	111	Rev. F
5-6	90	Rev. D
7-8	114	Rev. D

Rev. F boards have fast-clear capability by default.
Rev. D boards require modification.



Number of Boards to Modify

- From studies of COT hit occupancies and TDC readout rate measurements, we find that superlayers 5 and 6 require fast-clear functionality to maintain a 1 kHz readout rate for a luminosity of 4×10^{32} (keeping the DAQ deadtime below 5%).
- We estimate that superlayer 7 will most likely meet this specification without the fast-clear functionality but this estimate does not have a large safety margin.
- From an operational standpoint, a single pool of spare boards is easier to maintain.



Number of Boards to Modify

System	Rev. D boards
COT SL 5-6	90
COT SL 7-8	114
Hadron Timing	21
EM Timing	12
Spares (~25%)	63
Total	300

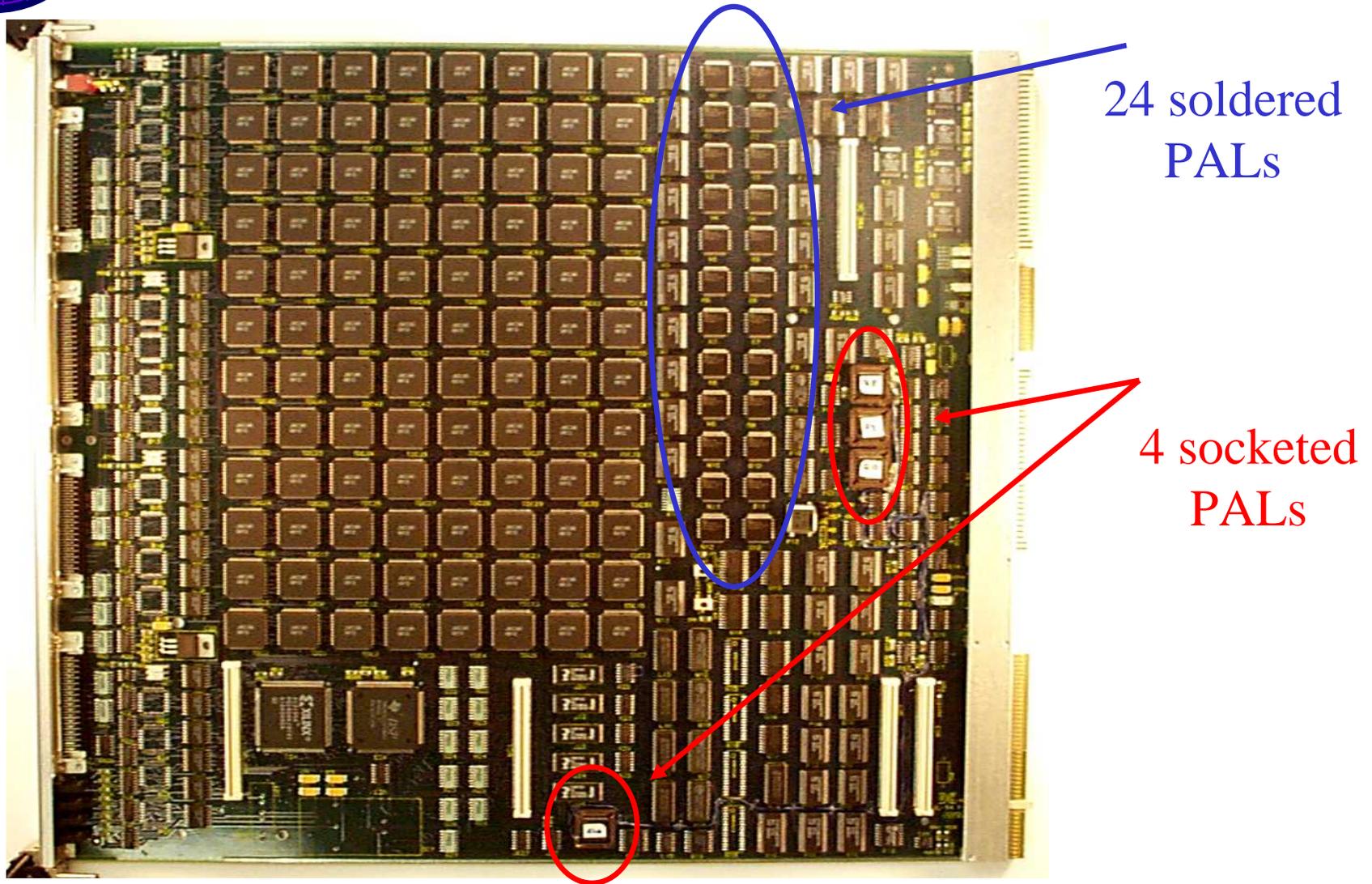


Board Modification Steps

- Remove 24 soldered PALs from board
- Clean and re-program each PAL
- Lift two pins on each PAL and re-attach to TDC
- Run 22 jumper wires between lifted pins on PALs
- Lift two pins on another chip and run four longer wires
- Remove four socketed PALs and re-program



Board Modification

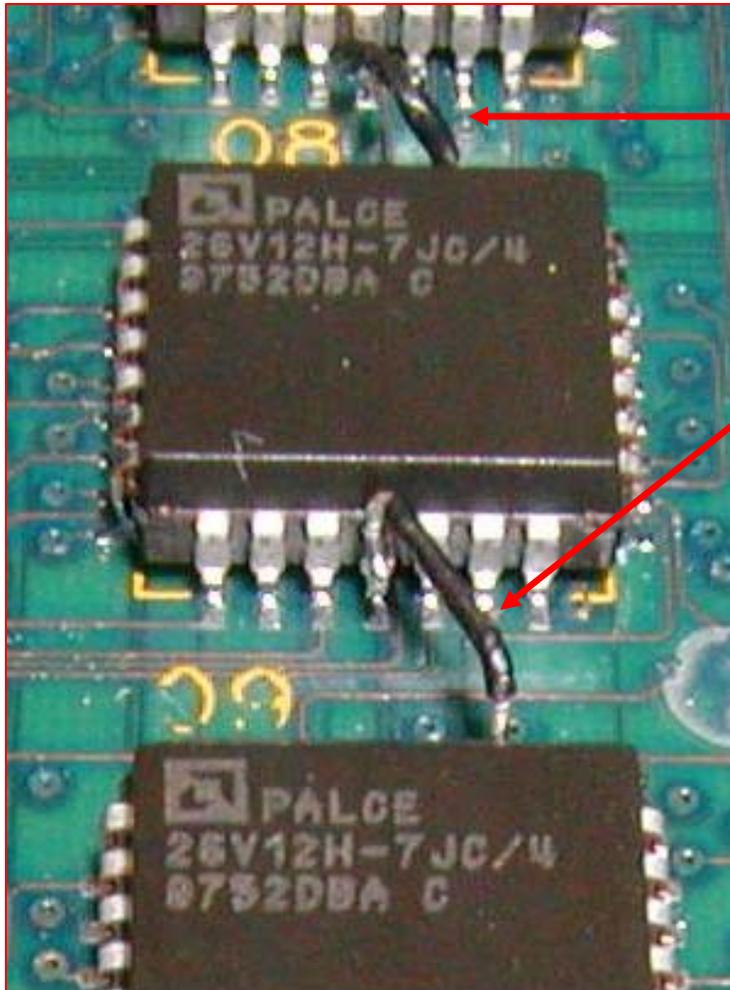


24 soldered
PALs

4 socketed
PALs



Board Modification



Jumper wires
between PALs



Modification Time

- PREP time estimate (based on one board modification)

Modification Step	Time Estimate
Remove 24 soldered PALs	1.0 hours
Clean pads on TDC board	1.5 hours
Clean PAL pins and re-program	3.5 hours
Re-solder PALs to TDC board	2.5 hours
Attach 22 PAL jumper wires	1.5 hours
Attach four long wire connections	1.0 hours
Re-program 4 socketed PALs	1.0 hours
Total	12.0 hours



Organization

- **Project Management – Eric James (Fermilab-PPD)**
- **Project Coordination - PREP**
 - Send and Receive boards to/from Michigan
 - Basic quality control testing
 - Tracking of boards through existing database.
- **Board Modification – PPD Technicians (Bob Jones)**
 - Board Modification on WH 13th floor.
 - PAL re-programming on WH 14th floor.



Organization

- **Board Testing and Calibration – Michigan Technicians**
 - Complete board testing.
 - Calibration using standard setup at Michigan.
- **Additional Testing and Installation – CDF Physicists**
 - Trigger mezzanine card testing (XFT upgrade) - Baylor & Illinois.
 - Burn-in testing on 1st floor prior to installation – Duke, Michigan, and Texas A+M



Modification Plan

- Plan to modify groups of 10 boards
- One week to modify boards on Wilson Hall 13th floor
- One week to test and re-calibrate boards at Michigan
- One week for additional testing at CDF
- One week for 1st floor burn-in testing at CDF



Boards on Detector

- We have an initial spare pool of 60-80 boards that we can use to get started.
- Once this pool is depleted, we will need to start cycling through boards currently installed on the detector.
- In order to accomplish this goal, we will need roughly eight hours of access time per month. We assume that we will be able to obtain this time parasitically, but if not we may need to request additional access time.



Boards on Detector

- Plan to minimize effect on operations with burn-in tests.
- Note that our “best” (large-via) boards are installed on the detector, and we do not want to simply replace these.



Schedule

- Project start on January 10th, 2005
- Estimate 29 weeks to modify 300 boards
- Board installation complete on July 27th, 2005
- Board modification complete on August 3rd, 2005
- Board testing complete on August 24th, 2005

Project Milestones in Green



Fermilab Labor

- **PPD technical support (Bob Jones' group)**
 - 10 boards/week * 12.0 hours/board = 120 hours/week
 - 3.5 full-time technicians for 29 weeks
- **PREP technical support**
 - 1.0 hour/board for quality control tests
 - 1.0 hour/board for shipping, receiving, and DB entry
 - 10 boards/week * 2.0 hours/board = 20 hours/week
 - 1 half-time technician for 29 weeks



Michigan Labor

- **University of Michigan technical support**
 - 0.5 hour/board to reprogram FLASH memories
 - 2.5 hour/board for calibration
 - 2.0 hour/board for pulsing and burn-in testing
 - 10 boards/week * 5.0 hours/board = 50 hours/week
 - 1.5 full-time technicians for 29 weeks
- **Note that the technicians at Michigan are also responsible for fixing broken TDC boards and maintaining spare pools for each board version.**



CDF Labor

- **XFT mezzanine card testing**
 - 10 boards/week * 2.0 hours/board = 20 hours/week
 - Physicist support from Baylor (1 PD) and Illinois (1 PD + 1 GS).
- **Burn-in testing and Installation**
 - 10 boards/week * 1.0 hours/board = 10 hours/week
 - Physicist support from Duke (2 GS), Michigan (1 GS), and Texas A+M (1 GS)



Cost Estimate

Cost Category	Amount
Fermilab Labor	\$228,378
Fermilab Material & Supplies	\$15,917
Michigan Testing/Calibration	\$38,462
Michigan Teststand Equipment	\$32,886
Total	\$315,643