



CDF Run IIb Trigger & Data Acquisition Upgrades

Peter Wilson

Fermilab

January 18, 2005



Run IIb Trigger/DAQ Upgrades

Outline:

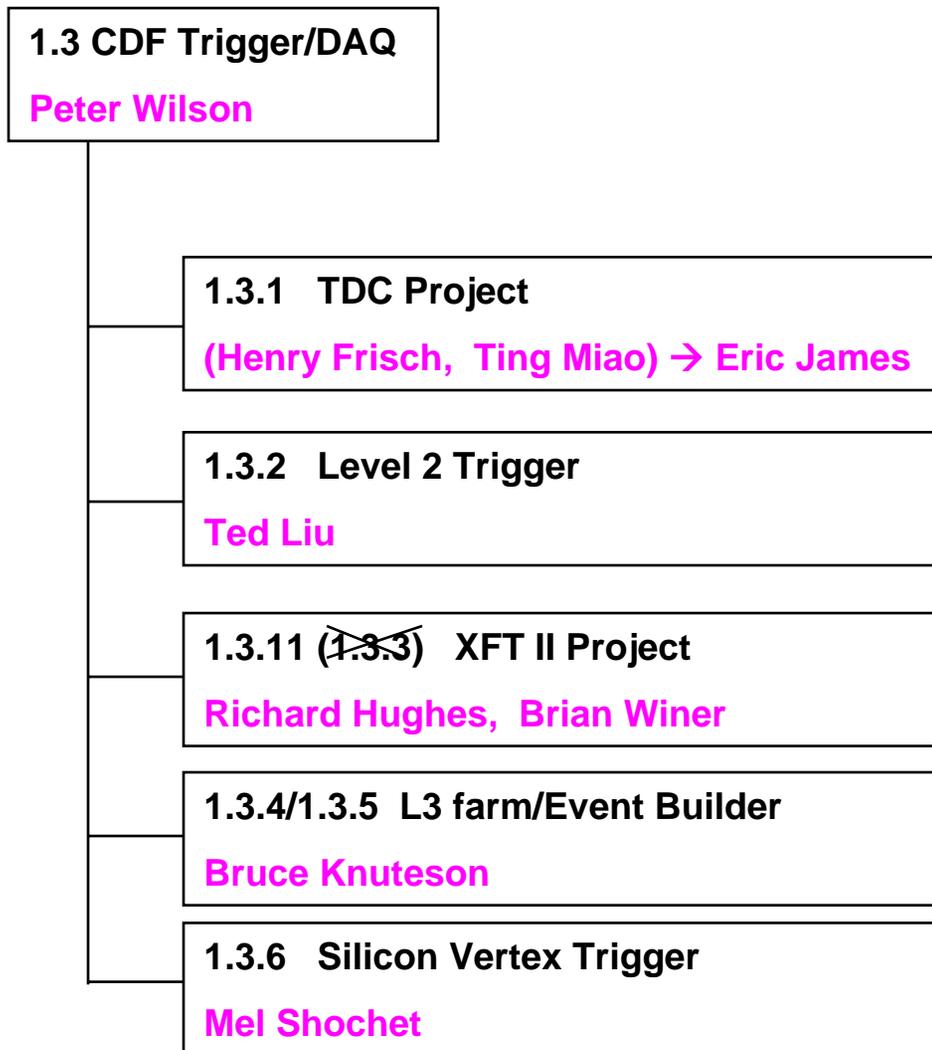
- **Brief Project Overview**
- **Sub-project Status** →
 - **Results of internal reviews**
 - **Blue subprojects will have separate talks**
- **Schedule**
- **Cost**
- **Conclusion**

The upgrades:

- 1.3.1 TDC replacement**
 - **Central tracker readout**
- 1.3.2 Level 2 trigger**
 - **Level 2 decision crate**
- 1.3.11 XFT upgrade**
 - **Level 1 track trigger**
- 1.3.4 Event builder**
- 1.3.5 Level 3 Processor**
- 1.3.6 SVT**
 - **Level 2 silicon vertex trigger**



Trigger/DAQ Management





DAQ/Trigger Specification

Run IIa vs IIb

	Run IIa Specification	Run IIa Achieved	Run IIb Specification
Luminosity	8.6×10^{31}	9.0×10^{31}	30×10^{31}
L1 Accept	45 kHz	25 kHz	30 kHz
L2 Accept	300 Hz	350 Hz	1000 Hz
Event Builder	75 MB/s	75 MB/s	500 MB/s
L3 Accept	75 Hz	80 Hz	100 Hz
Rate to Storage	20 MB/s	20 MB/s	40 MB/s
Deadtime Trigger	5%	10%	5% + 5% †

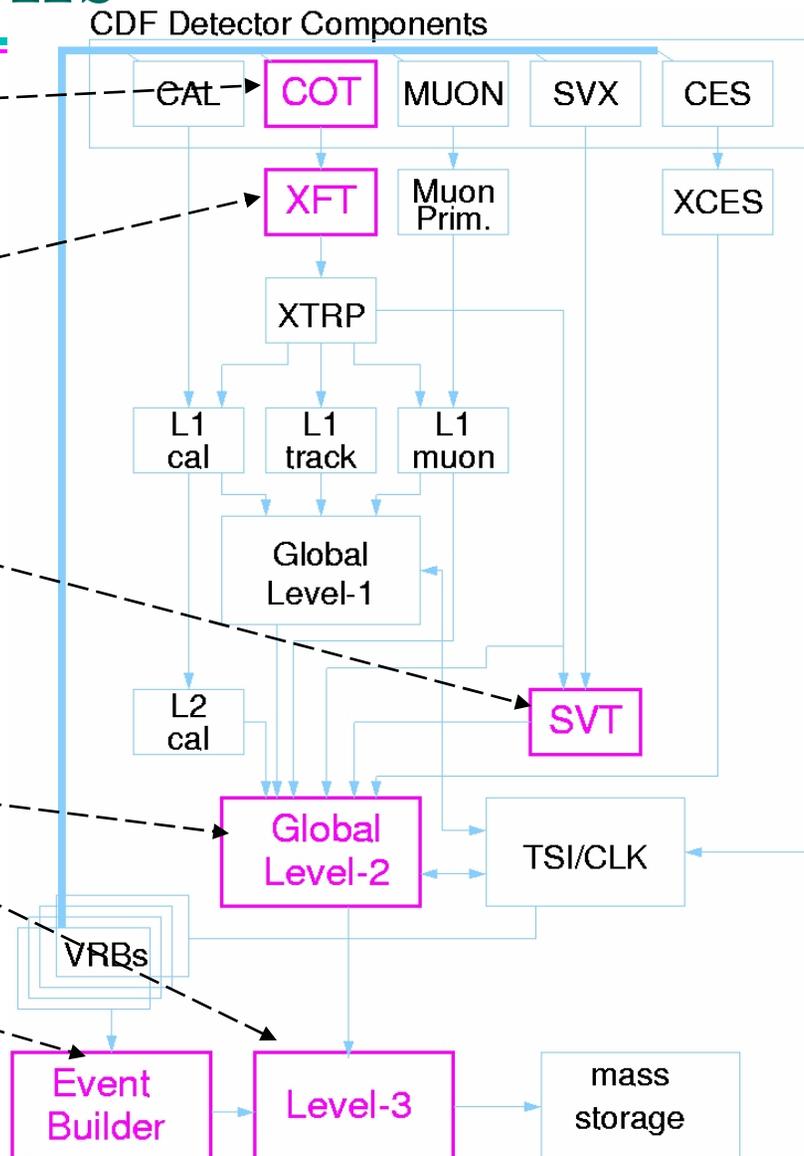
- Run IIa L1A not achieved due to higher than specified Silicon Readout + L2 Trigger execution times

† Assume ~5% from readout and ~5% from L2 processing



Trigger/DAQ Upgrades for Run IIb

- COT TDC upgrade
 - Readout rate insufficient (L2 Accept)
- COT Track Trigger Upgrade
 - L1 trigger rate reduction needed
 - Complexity of events (occupancy)
- Silicon Vertex Trigger upgrade
 - Occupancy demands higher processing speed
- L2/L3 trigger upgrades
 - Processing speed/modernization
- Event builder upgrade
 - Throughput increase needed
 - L2 accept rate is insufficient





Recent Reviews and Workshops

Since the July 2004 Director's review each sub-project has been through an internal review.

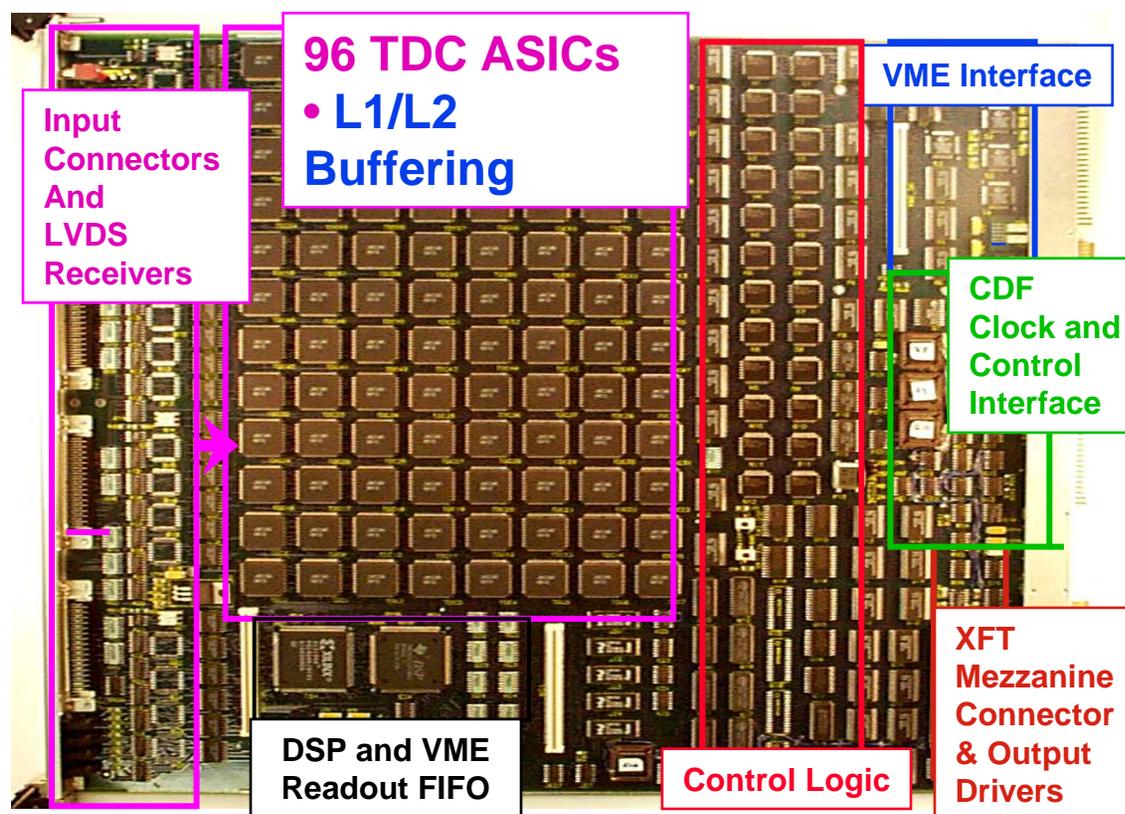
- 1.3.1 COT TDC
 - TDC Production Decision Review – Sept 28, 2004
- 1.3.2 L2 Trigger Decision
 - Installation Readiness Review – Sept 27, 2004
 - **Organized by CDF Operations Department**
- 1.3.11 L1 Track Trigger (XFT)
 - Progress Review – December 8, 2004
- 1.3.4 Event Builder
 - Progress Review – December 17, 2004
- 1.3.6 L2 Silicon Track Trigger (SVT)
 - Progress Review – January 4, 2004



Run IIa TDC Limitations

At time of Sep. 2002 DOE Review

- On-board hit processing (DSP) Time grows with # of hits
 - $t = 1200\mu\text{s/event}$ for SL1 (4 hits/ch) at $4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$
- VME Readout (16 TDCs/crate)
 - Read sequentially with one block transfer/card ($\sim 14\text{MB/s}$)
- VME to Event Builder limited to 12MB/s
- 2002 Internal review recommended pursuing replacement





Run IIb TDC-II Design

Altera Stratix FPGAs
(48chan/chip)

840MHz Diff LVDS inputs
TDC: Serial to 10bit parallel conversion (1.2ns/bit)
L1/L2 Buffering, hit processing + Readout (CBLT)
XFT Hit Generation

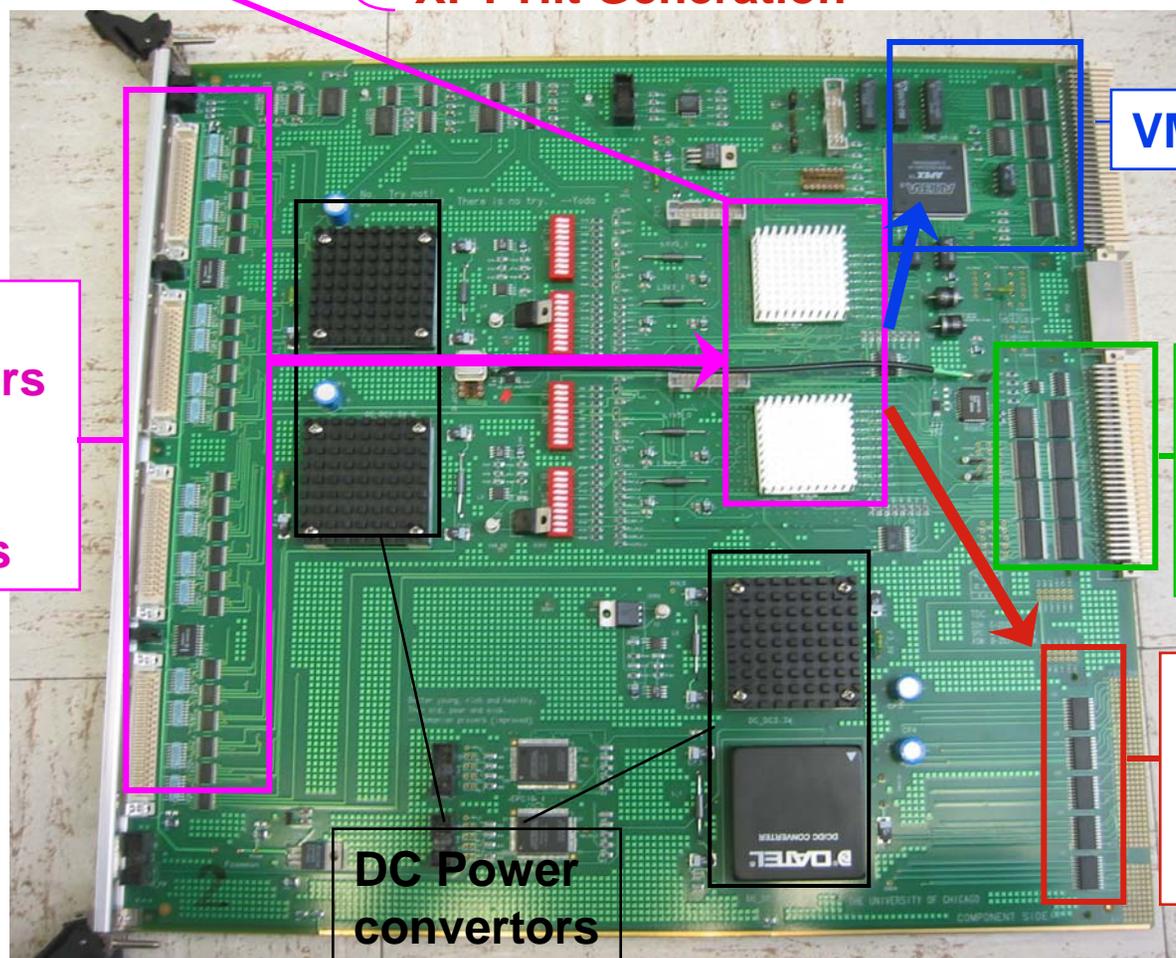
VME Interface

Input
Connectors
And
LVDS
Repeaters

CDF
Clock and
Control
Interface

Trigger
Output
Drivers
(to XFT)

DC Power
convertors





TDC Production Decision Review – Sept 28, 2004

CDF RunIIb Trigger, DAQ upgrades

P. Wilson Jan 18, 2005 slide - 9

- Performance Review of the existing TDCs recommended as decision point by July 2004
Director's Review
- TDC Committee: Eric James, Bruce Knuteson, Nigel Lockyer, Jim Patrick, Kevin Pitts (chair), Bob Wagner
- Paraphrased charge:
 - **Determine whether or not to proceed with the production run of the Run 2b (“Chicago”) TDC.**
 - How well would the existing (“Michigan”) TDCs perform if retained?
 - If installed, how well would the TDC-II perform?
 - Would the enhanced performance of TDC-II be utilized?
 - What are the relative risks for the two options?



TDC Performance Review

- Run 2a TDC
 - DSP execution now about factor of 2 faster than in 2002
 - New compressed data format (TDC-II format), halves the data volume
 - Measured performance of 5% deadtime at 1kHz with 3 hits/channel (inner layer occupancy expected at $4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$)
 - Need to implement Fast Clear function on TDCs in SL5,6 (already on SL1-4) to keep these from taking longer than SL1 ($L > 2 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$)
 - **Will meet the Run 2b readout specification**
- Run 2b TDC-II
 - 5 preproduction boards received in September pass tests
 - Implemented 64 bit VME transfer (was 32bit like rest of FE/Trig)
 - In bench tests 18MB/s (32bit VME) → 36MB/s
 - Can achieve 2kHz with less than 5% deadtime
 - **Exceeds all Run 2b specifications**
- Rest of DAQ/FE not expected to achieve much greater than 1kHz



TDC Review Outcome

- The review committee recommended retaining the current TDCs for the remainder of the run
 - Motivated by risk associated with commissioning a new system
 - Installation time will require an 8 week shutdown, followed by commissioning period during Tevatron operations.
 - Further bandwidth Improvement from TDC-II not likely to be utilized
- Modifications of the current TDCs are needed (outer layer modules), talk by Eric James
- Closeout TDC-II project by end of January 2005



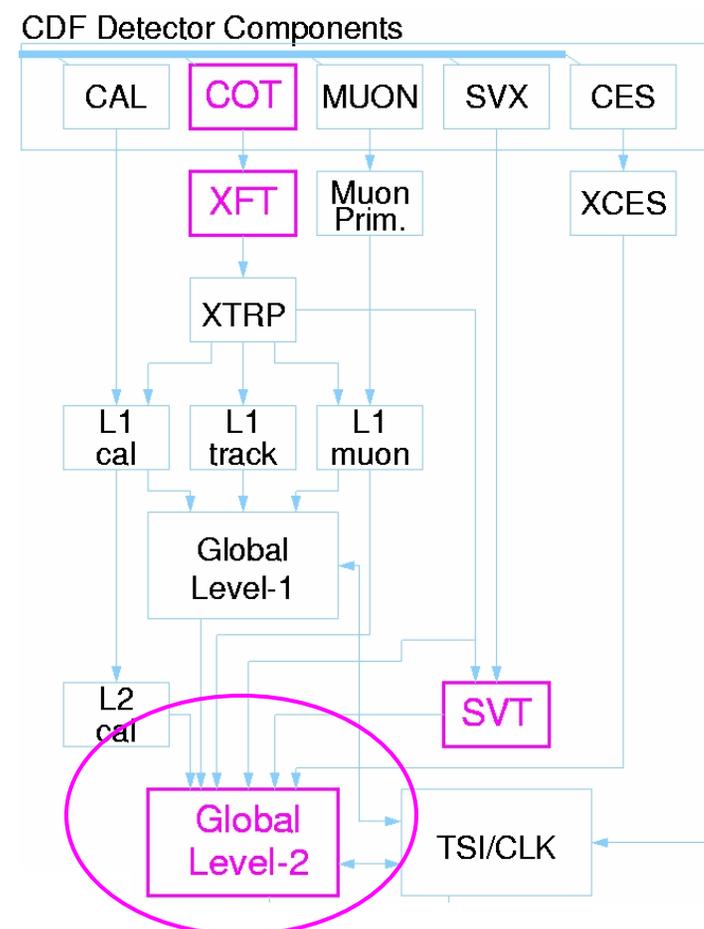
TDC-II Closeout

- ✓ Assemble and checkout of 35 preproduction TDCs (12/05)
- Limited full crate (16-18 boards) tests nearing completion
 - ✓ Measure readout bandwidth (>36MB/s)
 - Verify correct synchronization with detector clock and control signals
 - Complete tests by end of January
- Test with detector during shutdown cancelled
- No plan to use TDC-II boards for CDF operation, will be stored pending another application
 - Total of 3360 TDC channels (96/board) with 1.2ns/bit binning
- Will not implement “Virtual VRB” which would have brought COT TDC data into the Upgraded Event Builder
 - Would have been parallel path to existing VRBs
 - Will add VRB crates to distribute VRB load (Talk by Bruce Knuteson)



Level 2 Decision Crate

- Receive data from 7 preprocessors and make L2 decision in processor
 - L1 Trigger, Calorimeter, Cal. Isolation, ShowerMax (electrons) , Muon, L1 Track (XFT), L2 Silicon Tracking
- Run 2a decision crate:
 - 6 flavors of interface board
 - Decision in DEC Alpha processor on VME board
 - Data to processor on MagicBus
- In 2002, CDF internal review recommended replacing Alphas for Run Iib
- Upgrade with PULSAR board as universal interface
 - LINUX PC(s) replaces Alpha
 - CERN S-LINK replaces MagicBus
 - Test and Commission parasitically with copies of inputs to existing system





L2 Trigger Readiness Review

CDF RunIIb Trigger, DAQ upgrades

F. Wilson Jan 18, 2005 slide - 14

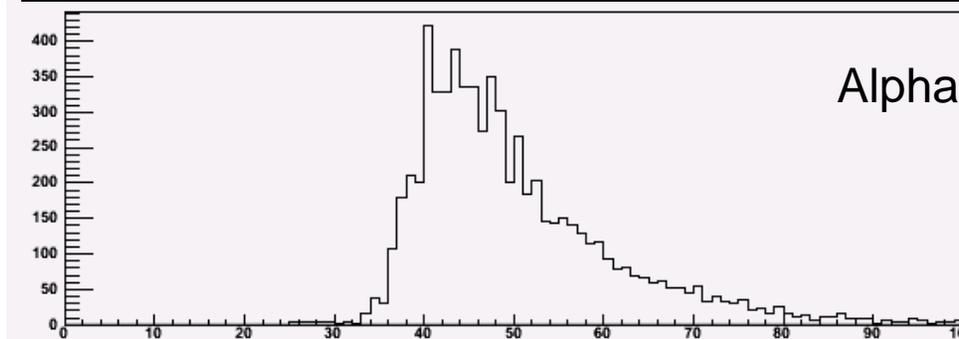
27 September 2004

- Organized (& chaired) by Camille Ginsburg for Operations Dept
- Evaluated status of all hardware, firmware, software and operational support plan
- At time of review had operated parasitically for 2 weeks of beam with 4 (of 7) subsystems
 - ✓ Same trigger decision (event by event) as existing system
 - ✓ Faster execution time though not yet optimized
 - Hardware, firmware and software in place for Cluster, Isolation and ShowerMax but not fully debugged.
- Review Findings/Action Items
 - Solve clustering/Isolation issues with experts of upstream systems
 - Debug signal splitting for ShowerMax
 - Apply more effort on integration of software with online/DB
 - Schedule follow-up review for late-January/early-February
 - Milestones of ready for operations: L3 – February 28, L2 - April 1



L2 Timing Measurements

Overall L1A to L2 Decision latency

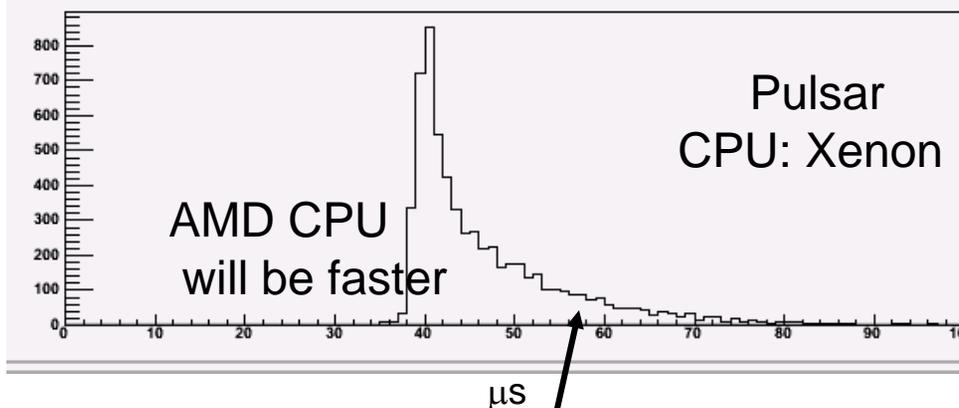


Before optimization as fast as existing Level2

Timing measurements will guide optimization.

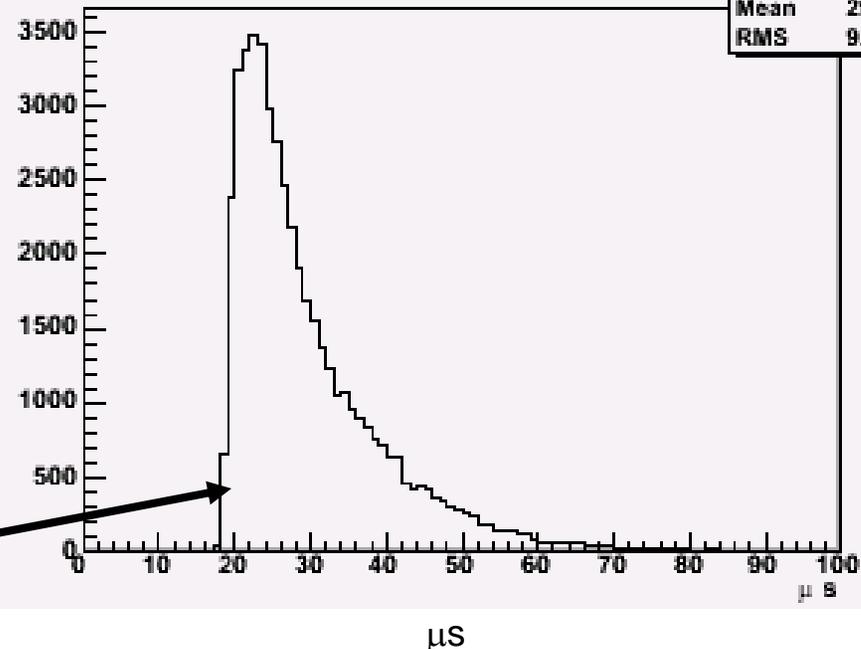
Goal: latency nonSVT < SVT

1AtoL2A/R PulsarSVT (prev)



Tail due to SVTProcessing (to be addressed by SVT upgrade)

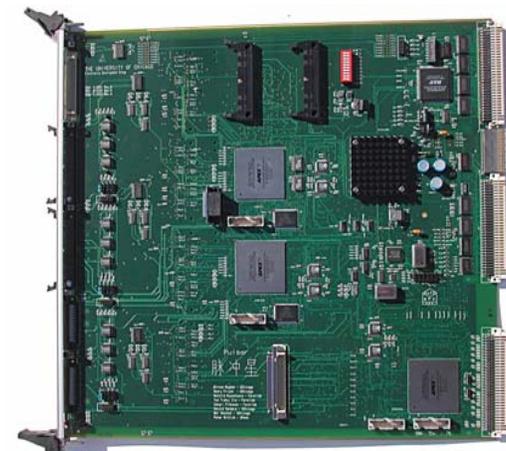
Start SVTIn (prev evt) (all)





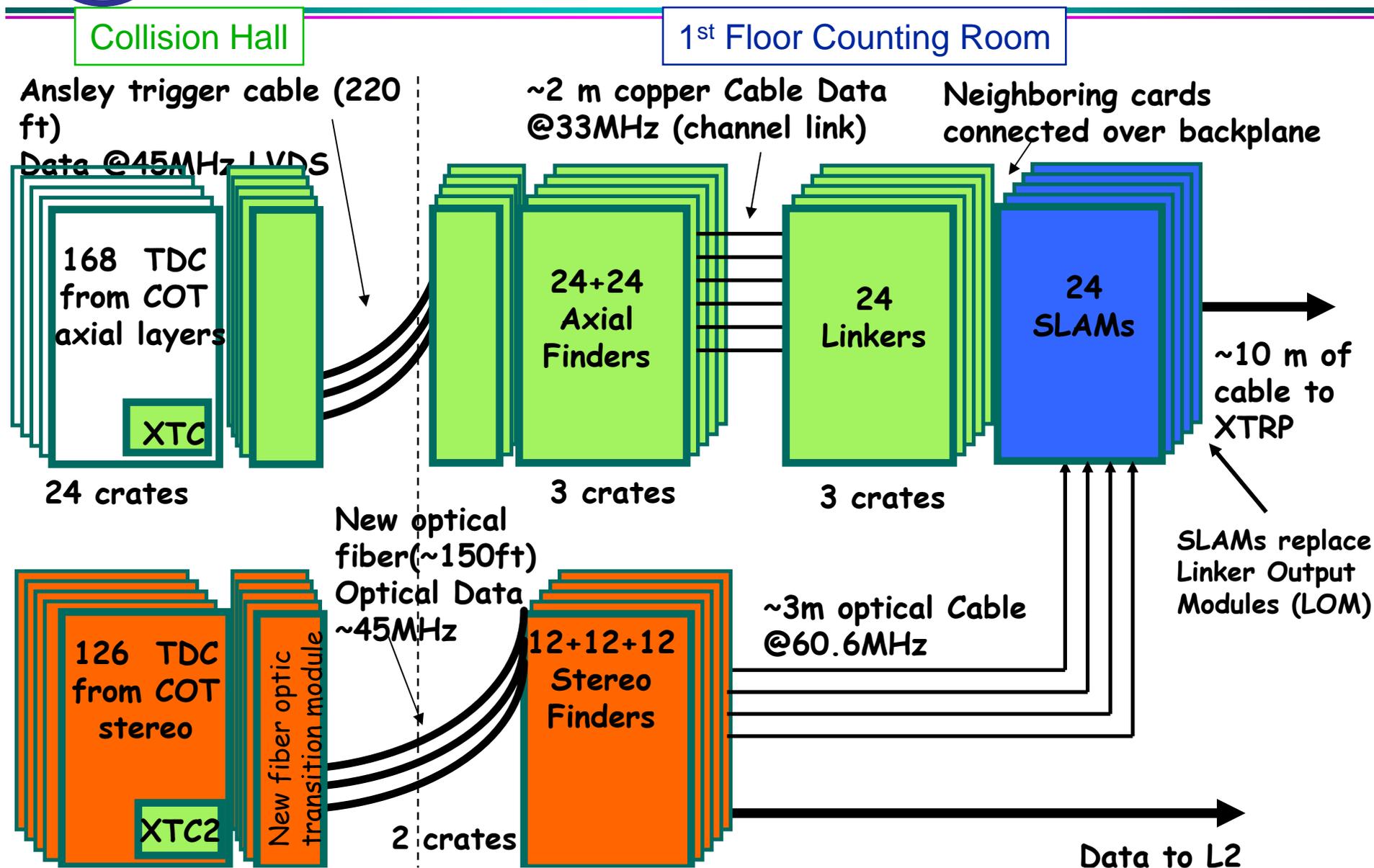
L2 Trigger (Pulsar)

- Since Readiness Review:
 - Solved Cluster/ISO firmware problems
 - Software Interface to Online/DB nearly complete
 - Fully automated configuration/operation near completion
 - ShowerMax data split successfully
 - Firmware performance improved (few μ sec faster)
 - Online Monitoring code in place
 - Expect full system tests w/shift crew control
 - w/o beam week of Jan 16
 - With beam by week of Jan 23
 - Run throughout February to fully validate system
- To ensure firmware support for system debugging/optimization during early operation, extended contract engineer (Sakari Pitkanen) through remainder of FY2005 (\$72K).
 - Brought PPD engineer (Steve Chappa) into SVT Pulsar Hit Buffer firmware project, will provide long term Pulsar firmware expertise





L1 Track Trigger (XFT) Upgrade





XFT Progress Review (12/8)

- Committee: Evelyn Thomson (Chair), Jim Patrick, Jonathan Lewis, Michael Schmidt, Harold Sanders, Jane Nachtman
- Covered technical status of hardware and firmware, plans for integration testing and related software
 - Details in Talk by Richard Hughes

XFT Committee conclusions:

- Excellent progress in last 6 months
- Schedule is tight:
 - Hardware needed before shutdown well along, must keep to schedule
 - No time for significant revisions before production on any design.
- Pipeline Timing (latency into SLAM) is a big concern



XFT Review Recommendations

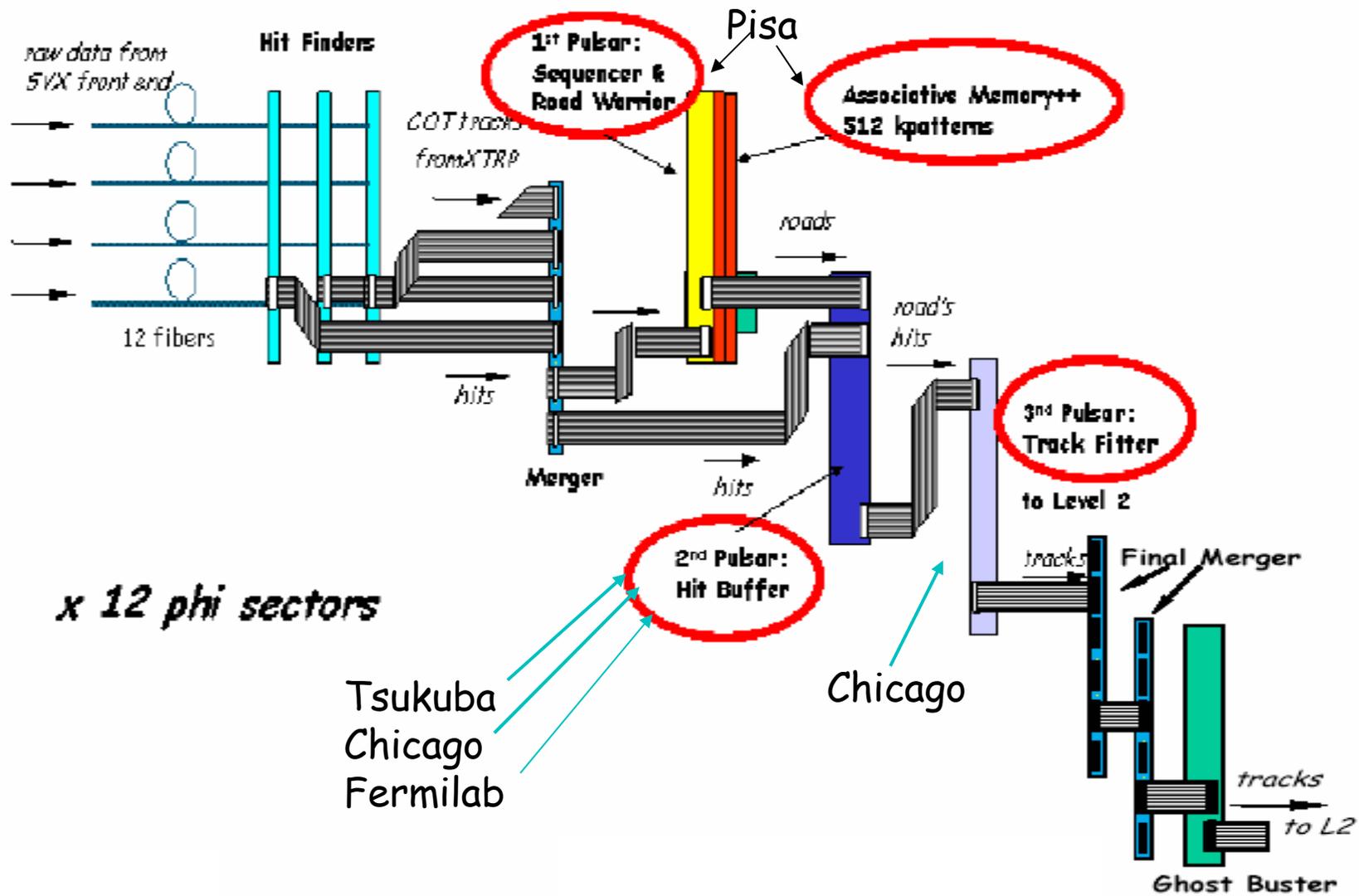
CDF RunIIb Trigger, DAQ upgrades

P. Wilson Jan 18, 2005 slide - 19

- Complete firmware and fully simulate ASAP to ensure that system will work as designed
- Develop a detailed plan for individual board testing and integration tests (eg Finder + SLAM).
- Identify additional personnel or reassign:
 - Physicists dedicated to software, testing, commissioning (ie Postdocs)
 - Manager to coordinate system testing and commissioning



The Upgraded SVT





SVT Progress Review (1/5)

- Committee: Bill Ashmanskas, Matthew Jones, Ted Liu, Jonathan Lewis – Chair, Steve Nahn
- Covered technical status of hardware and firmware, plans for integration testing and related software
- Details in talk by Mel Shochet
- SVT committee conclusions:
 - Excellent progress on hardware at Pisa and Chicago
 - Very good progress on firmware development
 - Track fitter and AMS/RW likely to be ready before August 2005 shutdown
 - Hit Buffer firmware schedule not realistic, less likely to have finished testing before the shutdown
 - Significant software development still needed



SVT Review Committee Recommendations

CDF RunIIb Trigger, DAQ upgrades
P. Wilson Jan 18, 2005 slide - 22

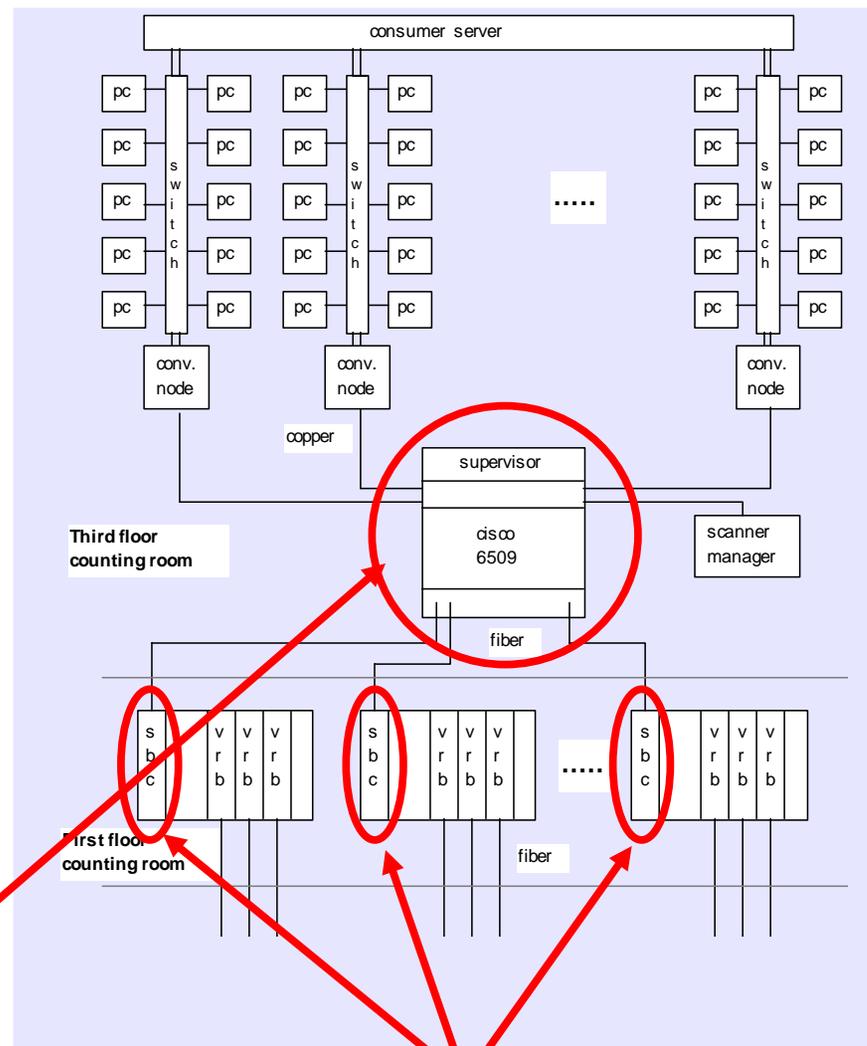
- Establish a vertical slice test at CDF by early February 2005 and maintain through to the installation and commissioning of the upgrade
 - Should parasitically use hits from the existing system
 - Each board should be added to vertical slice as available
- Establish a more detailed software development plan
 - Designate coordinators for main areas of software development preferably from experienced members of the SVT group



Run IIb Event Builder Upgrade

	RunIIa	Run IIb
Rate:	300Hz	1kHz
Event size:	250kB	500kB
Throughput:	75MB/s	500MB/s

SCPU:	MVME2600	VMIC7805
SCPU OS	VxWorks	Linux
Switch:	ATM	Cisco 6509 (gigabit ethernet)



new Cisco 6509 switch
new software (much less than IIa)

new VMIC 7805 boards (SCPUs)



Event Builder Progress Review

(12/17)

CDF RunIIb Trigger, DAQ upgrades
J. Wilson Jan 18, 2005 slide - 24

- Committee: Bill Badgett, Guillermo Gomez-Ceballos, Steve Nahn - Chair, Jim Patrick, Mel Shochet
- Covered technical status of software development and system testing, plans for integration testing, installation and commissioning.
- Committee conclusions:
 - Excellent progress, the system is very likely to be ready for use before the August 2005 shutdown



EVB Review Committee Recommendations

CDF RunIIb Trigger, DAQ upgrades
P. Wilson Jan 18, 2005 slide - 25

- Plan for testing of full system with FE crates and beam starting as soon as possible to avoid unexpected gotchas with real data
- Reconsider error handling strategies
 - Store information for diagnosis and stop the system to debug
 - Work on system recovery to make it faster
- Should proceed with re-arrangement of VRB crates to balance loads on VME backplanes
 - Rearrange Silicon Layer 00 and ISL to bring occupancy down to less than 20kB/event/crate
 - Add DAQ VRB crates to bring maximum occupancy down to <math><28\text{kB/crate}</math> at



Engineering/Technician Labor

- At the time of the July 2004 review there were several labor issues about which we were concerned. These have been addressed.
- SVT
 - EE - Steve Chappa from PPD has moved from TDC project to Hit buffer firmware. Expect him to become a resident expert on Pulsar firmware.
- XFT
 - Issues with layout technician handled, did not delay project
 - CP - Rod Klein is moving over from TDC-II teststand software to Finder teststand software



Project Milestones

L2 Decision

L2 Silicon Track Trigger (SVT)

Name	Forecast	Baseline	Variance	2004				2005				2006						
				2004		2005		2006										
				Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2					
Begin production of Level2 Pulsar system	11/12/03	11/12/03	0 wks	◆														
Pulsar Hardware Ready for Installation	8/20/04	8/31/04	-1.4 wks				◆											
Pulsar Level 2 subproject ready for installation	2/28/05	4/1/05	-4.6 wks							◆								
Begin AMS Design Work	8/2/04	9/1/04	-4.4 wks				◆											
Begin Track Fitter Design	8/2/04	9/1/04	-4.4 wks				◆											
Begin Ampchip Production	11/22/04	1/10/05	-5.8 wks							◆								
Begin AMS Mezzanine Card Production	11/11/04	1/14/05	-8.2 wks							◆								
Hit Buffer Firmware Complete for Board Test	6/14/05	6/23/05	-1.6 wks															◆
Track Fitter Firmware Complete for Board Test	3/31/05	6/28/05	-12.6 wks															◆
AMS Firmware Complete for Board Test	4/14/05	8/19/05	-18 wks															◆
SVT ready for installation	8/9/05	8/25/05	-2.4 wks															◆
Ready for Accelerator Shutdown 2005	7/27/05	8/8/05	-1.4 wks															◆
Finish Run 2b Trigger DAQ project	9/22/05	9/30/05	-1 wk															◆
Data Acquisition and Trigger Upgrades Ready for	9/22/05	1/17/06	-15 wks															◆

- ◆ Baseline Date
- ◇ Forecast Date
- ★ Actual Date

Green milestones are needed before 2005 shutdown



Project Milestones

Event Builder

L3 Computers

Name	Forecast	Baseline	Variance	2004				2005				2006						
				2004		2005		2006										
				Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2					
Arrival of the prototype Event Builder hardware	3/31/04	6/3/04	-9 wks		★	◆												
Event Builder Production Readiness Review	6/2/04	10/4/04	-17 wks			★			◆									
Arrival of the Event Builder hardware	10/15/04	10/15/04	0 wks						◆									
Finish Event-Builder Upgrade	6/29/05	7/28/05	-4 wks															◆
Arrival of 15 PCs from the vendor	5/20/05	3/23/05	8.4 wks															◆
Arrival of 70 Level3 and 15 DAQ PCs from the vendor	8/15/05	8/15/05	0 wks															◆
Arrival of 140/20 PCs from the vendor	8/15/05	8/15/05	0 wks															◆
Finish Purchase of Computers for Level3/DAQ systems	9/6/05	9/6/05	0 wks															◆
Ready for Accelerator Shutdown 2005	7/27/05	8/8/05	-1.4 wks															◆
Finish Run 2b Trigger DAQ project	9/22/05	9/30/05	-1 wk															◆
Data Acquisition and Trigger Upgrades Ready for	9/22/05	1/17/06	-15 wks															◆

- ◆ Baseline Date
- ◇ Forecast Date
- ★ Actual Date

Green milestones are needed before 2005 shutdown



DAQ/Trigger Summary

- All projects are on track for completion before the end of FY2005
 - Upgrade L2 Decision and Event builder should both complete before Summer 2005 shutdown
 - Still a major effort to complete XFT, SVT and TDC modifications but all should be able to complete before Sept 30, 2005
- Cancellation of Run 2b TDC-II project has lead to a new project to modify existing TDCs which should complete before the end of the 2005 shutdown.



Summary – Installation Strategy

- Installation and commissioning will occur as each subsystem becomes available
 - Essentially all can be tested parasitically or with quick change-over for tests
 - Exception is SVT which will have a vertical slice test parasitically prior to installation
- Expected transition to operations:
 - Level 2 Decision – March 1, 2005
 - Event Builder – between May and August 2005
 - COT TDC – Winter 2005 - Oct 2005
 - Compressed data format within 2 months
 - Modified TDCs by end of 2005 shutdown
 - L1 Track Trigger (XFT) – Oct 2005 – Early 2006
 - L1 fake rate reduction first (Finder + SLAM)
 - Additional L2 rejection with stereo tracking early 2006
 - L2 Silicon Track Trigger (SVT) – Fall 2005



Additional supporting Slides



Supporting Documentation

- CDF Run IIb Technical Design Report
- Report from DAQ review Oct 2003
- TDCs
 - Specification for Run 2b TDC
 - CDF6998 – Run IIB TDC-II Address Space
 - CDF6999 – TDC-II Design and Specification – Run IIB TDC for the COT
 - May 2004 Production Review Report
- L2 Trigger
 - PULSAR Web page (documentation, schematics, BOM): <http://hep.uchicago.edu/~thliu/projects/Pulsar>
 - CDF6259: “Run IIb Upgrade for CDF L2 Decision Crate”
 - Nov 2004 Production Readiness Review Report
- XFT
 - CDF7039 XFT Upgrade Options and Studies
 - CDF6059 Specifications for the Upgraded XFT System for High Luminosity Running in Run 2
 - May 2004 Review Report
 - June 2004 Review Report
- SVT
 - CDF7064 Silicon Vertex Trigger Upgrade
 - Review report from June 2004 review
- EVB
 - Report on Prototype test results – April 2004
 - Report on review by DAQ Experts – April 2004



CDF Trigger/DAQ Labor

- TDC Modification
 - Fermilab(PHYS+TECH), Michigan(ENG+TECH+PHYS), Duke(PHYS), Texas A&M(PHYS)
- XFT
 - Ohio State(ENG+PHYS+TECH), Illinois (ENG+PHYS+TECH), Purdue (PHYS), Fermilab (ENG+TECH), Baylor (PHYS), Davis (PHYS)
- Level 2
 - Fermilab(ENG+PHYS+TECH), Chicago(ENG+PHYS+TECH), Penn(ENG+PHYS+TECH)
- SVT
 - Pisa(ENG+PHYS+TECH), Chicago(ENG+PHYS+TECH), Fermilab(ENG+PHYS), Ferrara(PHYS), Sienna(PHYS), Tsukuba(PHYS), LBNL(PHYS), Rome(PHYS), Wisconsin(PHYS)
- EVB/L3
 - MIT(PHYS), Fermilab(ENG)