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## **Time to Digital Converter Module for Run IIB of the Fermilab TeVatron Collider**

### **System and Performance Requirements**

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#### **ABSTRACT**

In Run IIB, occupancy in CDF's Central Outer Tracker (COT) is expected to be higher than the existing TDCs can handle without substantial dead time. The higher occupancy comes primarily from the need to handle higher luminosity at 396 nsec bunch spacing, but also from higher than anticipated rates in the COT even at low luminosity. We need to replace these TDCs.

In addition to creating readout problems, the higher occupancy degrades the performance of our hardware track finder, the eXtremely Fast Tracker (XFT). The new TDC is required to address this issue by making higher resolution hit data available to the XFT.

To speed development, avoid major re-work of the cable plant, and to reduce coupling of the TDC schedule to that of other systems, the replacement TDC is required to be compatible with the existing TDCs. In particular it must be able to send data to the XFT in the same low-resolution form presently used. Switch to higher resolution data must be possible by re-programming the TDC.

It is anticipated the existing TDCs will be used in all systems except the COT. Therefore, the specifications given here are specific to the COT.

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## I. INTRODUCTION

The existing COT TDC system is packaged in VME and consists of 315 JMC96 modules distributed over 20 crates. Each TDC module provides 96 channels of multi-hit leading edge and trailing edge time information. In order to minimize the amount of work involved and maximize use of the existing investment, the replacement TDC modules shall be VME modules with input connectors and signal levels compatible with the JMC96. They shall also make use of the same back-plane control lines as the JMC96, and use the same output connectors (on the auxiliary back plane) and signal levels for sending information to the trigger system. The specifications detailed in this note, describe a TDC module with the following global characteristics:

1. Packaging A 96 channel VME module that is "plug compatible" with the JMC96 TDC module.
2. Mode Multi-hit with leading edge and trailing edge timing for each input channel measured relative to the CDF clock.
3. Control Blocks of data multiply buffered in response to control signals from the trigger and data acquisition systems.

## II. DATA ACQUISITION AND TRIGGER SPECIFICATIONS

### A. General Readout Scenario

Each crate contains, in addition to the TDC modules, a "Tracer" module that communicates control signals – in particular, Level 1 and Level 2 accept information – from the higher level system to the individual TDC modules in the crate over the VME backplane. Each crate also contains a "Crate CPU"; this, together with the Tracer, is responsible for reading out the TDCs. The Crate CPU also initializes the TDCs, including downloading information to it (e.g., compression maps).

Data from the detector is sampled each beam crossing and a subset is delivered by a dedicated path to a Level 1 Trigger system. The Level 1 Trigger is a pipelined device that renders a decision every beam crossing for the crossing approximately 5.5 microseconds. This Level 1 trigger latency implies that the detector TDC data must be stored in a pipeline during the 5.5 microsecond decision process. If the Level 1 trigger decision is negative, data falls out the end of the pipeline without being stored. If the Level 1 trigger decision is positive, the TDC transfers the data in the region of interest to one of four "Level 1 buffers" while a Level 2 trigger performs further analysis of the event. It is the responsibility of the trigger system to specify which Level 1 buffer to use.

If the Level 2 decision is positive, a Level 2 Accept and buffer ID are delivered to the TDC. Data from the specified Level 1 buffer is then transferred to an output buffer for later readout by the Tracer and crate CPU. Maintaining a separate output buffer makes the Level 1 buffers available more quickly and reduces the system dead time. If the Level 2 decision is negative, the Level 1 buffer is overwritten by a later Level 1 trigger without being transferred to the output buffer,

The Level 2 decision time is 10–20  $\mu$ sec, while the readout time must be < 500  $\mu$ sec. The expected Level 1 Accept rate is ~50 KHz, and the expected Level 2 accept rate is ~1 KHz.

## **B. VME Input**

The TDC must accept the following signals sent by (existing) “Tracer” modules across the VME backplane.

**Level 1 Accept:** Indicates that the Level 1 trigger has fired and data from the time window of interest in the pipeline should be saved in a Level 1 buffer. It may be assumed that Level 1 Accept as received by the TDC is precisely timed and should be used as a time reference.

**Level 1 Buffer:** Two bits that indicate into which of the four Level 1 buffers the TDC data should be saved. The TDC should assume the address is valid and not do any internal buffer management. The higher level system will keep track of which buffers have valid data.

**Level 2 Accept:** Indicates that one of the data blocks in a Level 1 buffer is part of an event that has been accepted by the Level 2 trigger. The corresponding data should be copied to a separate output memory buffer.

**Level 2 Buffer:** Two bits that indicate which of the four Level 1 buffers has been selected by the Level 2 Accept. The TDC should assume the address is valid and not do any internal buffer management. The higher level system will keep track of which buffers have valid data.

**Test Pulse:** For calibration, the TDC shall receive differential PECL signals from the VME backplane, convert this to differential ECL, and send it out the four front panel connectors (and from there on to the on-chamber electronics). Delay across the backplane, from the backplane to the front panel connector, and of the cable to the chamber must be measured as part of the overall system calibration. However, swapping TDC modules must not require re-doing this calibration; therefore, the module-to-module variation in delay must be  $< 0.5$  nsec.

In addition, the Tracer sends a **Level 2 Reject** and buffer ID indicating that any formatting of the specified buffer may be aborted as it will in fact not be read out. Use of this signal is optional.

## **C. VME Output**

**Busy:** Asserted when the TDC is in the process of copying one of the Level 1 buffers to an output buffer, signifying that the Level 1 buffer is not currently available and the TDC may not receive another Level 2 Accept during this time. The status of this output should be reflected in a bit in a control and status register. To minimize cable plant and make the event readout process more efficient, it is recommended that the individual busy signals be wire-or'ed onto one unassigned VME backplane line. The status of the wire-or'ed Busy line will then be available to the crate fanout module and the readout controller.

**Data Output Buffer:** Data from events accepted by the Level 2 trigger shall be copied to an output buffer separate from one of the four Level 1 buffers. This output buffer shall either be a FIFO, or, if implemented as a number of fixed length buffers, a VME read

operation should automatically give the first filled data buffer. The following items list minimal requirements on the output buffer.

Length

- capable of storing data from at least 8 events.
- large enough to store approximately 8000 hits within the desired time window integrated over all events.

Functionality

- The output buffer shall be writeable via VME
- Patterns to be sent to the trigger system shall be writeable via VME.
- The status of the buffer (full etc.) shall be available in a VME control and status register
- A VME control and status register operation shall be provided for reset of the output buffer.
- The Level 2 buffer ID number shall be stored in either the first or last word of the record for a cross check

Format

- Data will be compressed using Huffman compression. The map (Huffman tree) will be down-loaded to the TDC and will *not* be included in the readout. There will be a separate map for leading edges and widths.
- Number of 32-bit words to be transferred will be available with a single VME read.
- Data will be read as a single block transfer per TDC.

End of Record

- on readout, an appropriate end of data signal shall be generated after all data in an event has been read.

#### ***D. Front Panel Signals***

The TDC must accept pseudo-LVDS input signals supplied by (existing) “Repeater” boards. These are current-source outputs requiring  $\sim 50 \Omega$  pull-up to  $> 1V$ . The effective termination between pairs is about  $100 \Omega$ .

The TDC must also supply  $-3V@120mA$  power for the repeater board at each of the four front-panel connectors. Calibration pulses (picked off from the backplane) must be sent as differential ECL.

#### ***E. VME Functionality***

The TDC must conform to all mandatory requirements given in CDF Note 2388.

#### ***F. Dead Time***

**Level 1 Accept:** There shall be no dead time associated with a Level 1 Accept. The TDC shall deal with Level 1 Accepts on consecutive crossings (132 nsec).

**Level 2 Accept:** Busy time shall be  $< 100$  microseconds in duration assuming 500 hits in the desired time window provided space is available in the output buffer. If the output buffer is full, then the copy operation shall stall and Busy shall remain asserted until space becomes available (presumably because data is read by the readout controller).

**Readout:** There shall be no dead time associated with readout of the output buffer. Readout shall be able to occur simultaneously with time measurement operations of the TDC.

### III. TIME MEASUREMENT PERFORMANCE REQUIREMENTS

#### A. Specifications

1. Average Precision (including effects of non-linearity):
  - a) RMS error on time of Level 1 Accept: < 0.3 nsec  
This error is correlated among all channels in the TDC
  - b) Total (hit – reference)) RMS error: < 0.42 nsec
2. Minimum Input Pulse Width: < 10 nsec (<5nsec option ... see discussion below)
3. Double Pulse Resolution: < 10 nsec
4. Selectable range:  
The size of the region of interest from the L1 pipeline shall be selectable in increments of ~50 nsec from a minimum of 150 nsec to a maximum of 300 nsec.
5. Multiple Hits per Channel: 4 within the selected region of interest (prefer up to 8 hits)
6. Multiple Hits per TDC:  $4 \times 96 = 384$  within the selected region of interest
7. Duty Factor and Cross Talk:  
Ability to record hits on all channels simultaneously with input rates of 16 MHz of 20 nsec width signals. The change in measured time shall be less than 0.25 nsec RMS as a function of input rate and number of active channels.
8. Channel to Channel Matching:  
Slope < 0.05%  
Pedestal  $\pm 4$  nsec
9. Pedestal Stability:  
< 100 psec/ $^{\circ}$ C  
< 1 nsec long-term drift
10. LVDS Input Termination variation shall be less than 10%

#### B. Discussion

##### 1. Average Precision

It is assumed here that the TDC is a digital device that records the particular time bins in which chamber and reference signals occurred. It is important to distinguish the error in measuring the chamber pulse that from the shared reference signal. If a 12-wire superlayer is considered as providing a single measurement of a track, the error due to the TDC, assuming 1 nsec bins, would be

$$1 / \sqrt{12} \times 1ns / \sqrt{12} = 0.083ns \quad \oplus \quad 1ns / \sqrt{12} = 0.29ns$$

per-hit error

shared error

which is dominated by the measurement of the reference signal. This is, of course, a over-simplified picture, and the actual affect of reference-time error is not so dramatic. Never the less, care should be taken to minimize this correlated error. This was done in Run-I (by LeCroy 1879 TDC modules) by a “phase bit” (shared across the TDC) giving an additional bit of accuracy on the reference time.

Alternatively, phase-locking the TDC's internal clock to the CDF clock can virtually eliminate this error. We assume this will be done in the new TDC design so the correlated error term is a secondary issue.

The chamber resolution is 150  $\mu\text{m}$  per wire; at a drift velocity of 50 micron/nsec (our present standard), this corresponds to 3nsec. However, to retain the option of changing gas mix (which may prove useful for aging, independent of speeding up the drift velocity), we need to allow for drift velocity up to 100 micron/nsec; then the chamber resolution translates to time resolution of 1.5nsec per hit. If we want the TDC binning to degrade the resolution by no more than 5%, the required RMS error on the TDC measurement is 0.48nsec. We have set the requirement slightly lower to allow for some residual correlated errors.

### **3. Minimum Pulse Width**

At present, pulses of width  $< 10$  nsec are (almost) never used in track. However, in a faster drift gas, useful pulses may be narrower. Therefore it would be preferable to have the TDC able to accept narrow pulses. The ASDQ which feeds the TDCs generate  $>4$ nsec pulses, so there is no need to accept pulse widths below that.

On the other hand, keeping narrow pulses increases the data volume, so a cut software-switchable between 5nsec and 10nsec would be ideal.

### **4. Double Pulse Resolution**

This quantity refers to the time between the end of one pulse and the start of the next. The ASDQ pulse shaping takes  $\sim 10$ nsec to recover sufficiently to give good timing information on the next pulse, therefore we require the TDC be able to accept such a pair of pulses.

### **5. Multiple Hits per Channel**

The innermost superlayer of the central tracker will see of order 3 tracks hits per wire in a typical psi event at 1 E32 luminosity and 396 nsec bunch spacing. Some of these hits will merge in the TDC, on the other hand some will break into multiple pulses. The specification for 4 hit per channel capability is, therefore, probably fine but leaves less room to spare than we might like. Again, a down-loadable cutoff (up to 8) would be ideal.

### **6. Duty Factor and Cross Talk**

The innermost superlayer of the central tracker will have a rate of about 16 MHz per wire at 2E32 luminosity. 20 nsec is a lower bound on probable pulse widths using a fast gas.

## **IV. TRIGGER SIGNAL REQUIREMENTS**

The TDC must be able to supply the same trigger signals as (existing) XTC boards.

- Multiplex four channels to one differential output.
- For each channel, supply two bits indicating presence of signal in the "early" and "late" time. The meaning of "early" and "late" should be programmable.

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