CDF Run IIb Calorimeter, Trigger & Data Acquisition Upgrades

Kevin Pitts
University of Illinois
for the CDF Collaboration

September 24, 2002

Calorimetry Upgrade

Steve Kuhlmann, Level-2 Manager

Joey Huston, Level-3 Manager Preshower

Dave Toback, Level-3 Manager EM Timing

Preshower/Crack

- University of Tsukuba
- INFN (Pisa, Rome)
- JINR (Dubna)
- Argonne National Laboratory
- Michigan State University
- Rockefeller University
- FNAL

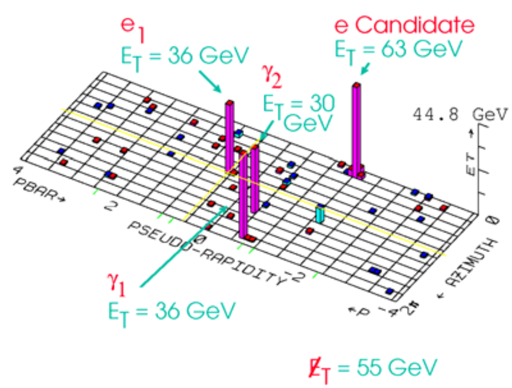
Electromagnetic Timing

- Texas A&M
- INFN (Frascati)
- University of Chicago
- University of Michigan
- Argonne National Lab
- FNAL

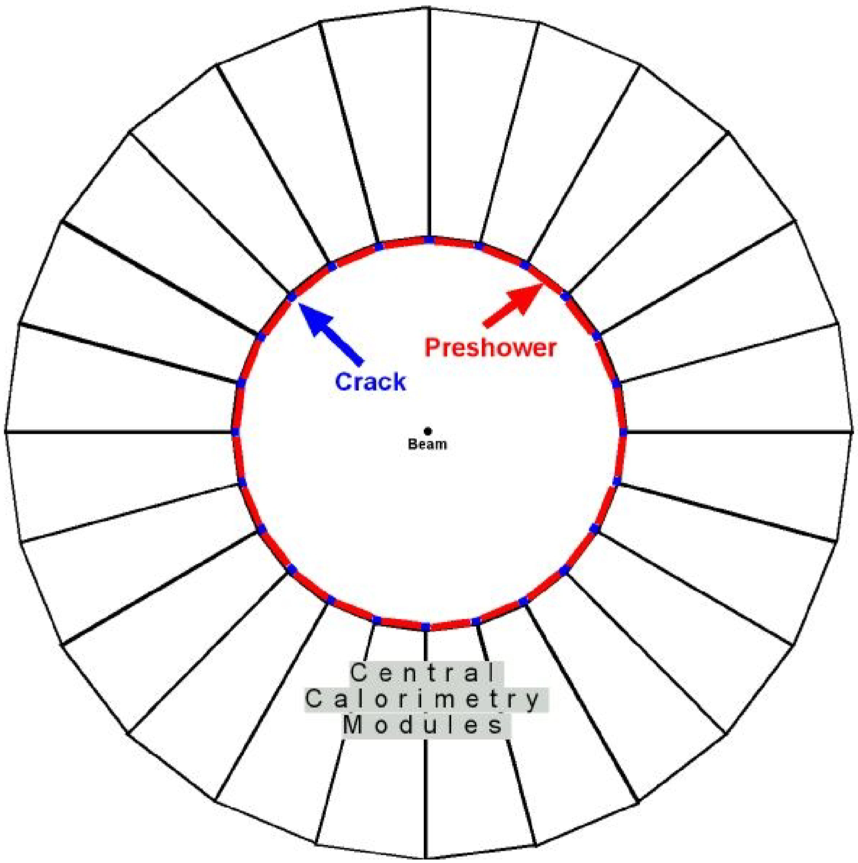
Calorimetry Upgrade Motivation

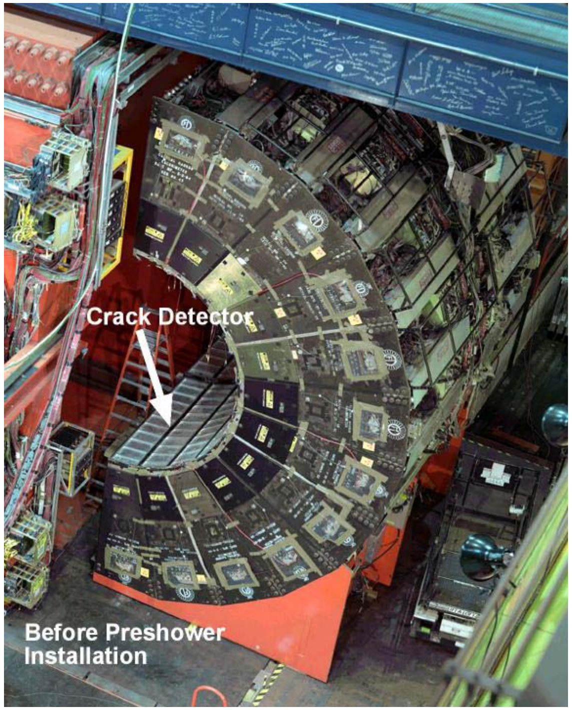
- Maintain capabilities of current Preshower detector, used in over 100 papers.
- Preshower expected to suffer high occupancy and aging effects in Run IIB.
- Preshower and Crack detectors expected to provide 5-10% Jet Energy Resolution improvement, part of the 20-30% needed improvement for the Higgs search.
- Electromagnetic timing needed to reject photon backgrounds from cosmic rays, in new physics searches such as SUSY.

$ee\gamma\gamma\not{E}_T$ Candidate Event

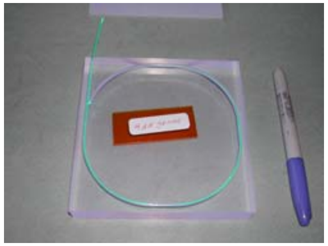


Preshower/Crack Detectors

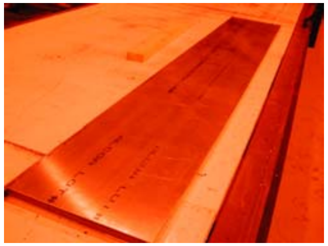




Preshower/Crack Design



- 2 cm Dubna scintillator for Preshower, tile and groove cut at FNAL



- Aluminum shells, full-scale mechanical prototype built at ANL

- Prototypes being assembled and tested at ANL and Pisa

Preshower/Crack Design

- Prototype clear fiber bundle built at MSU

- R5900 16-channel PMTs, tested at Tsukuba and Rockefeller

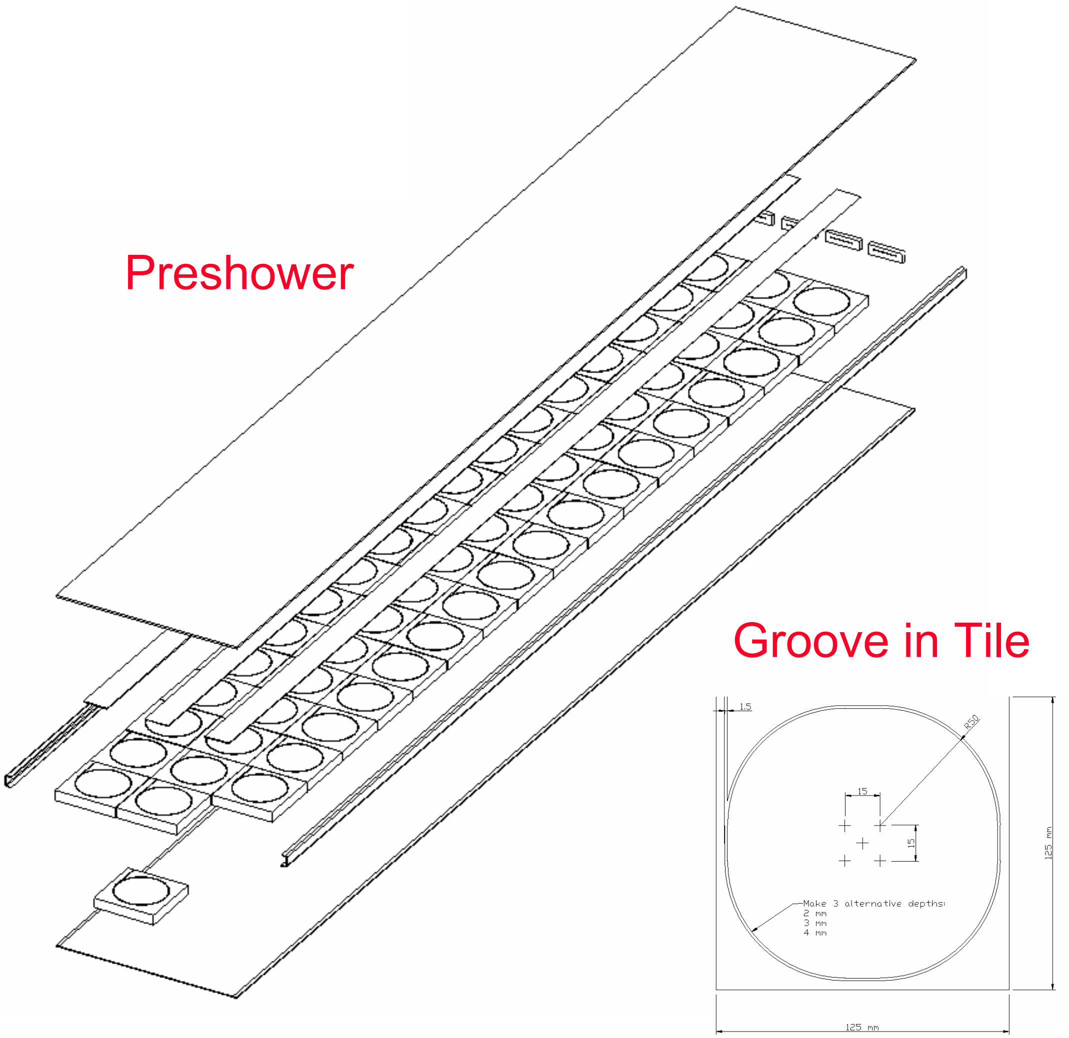
- Output of phototube box similar to current MSU design

- Reuse existing electronics except for new transition board

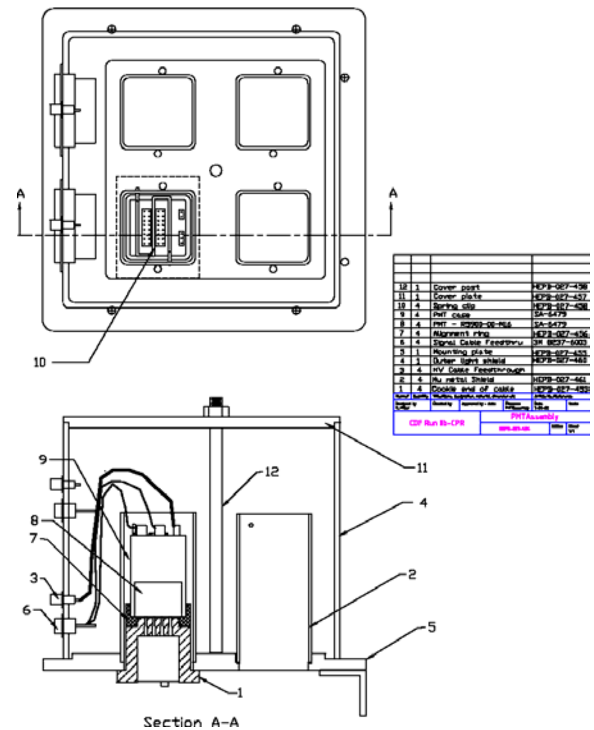
Preshower/Crack Diagrams

Preshower

Groove in Tile

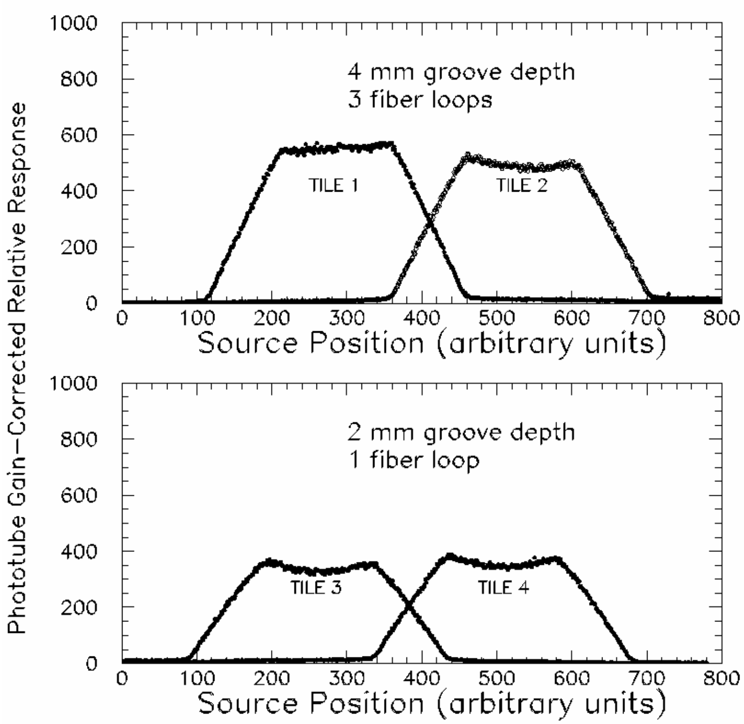


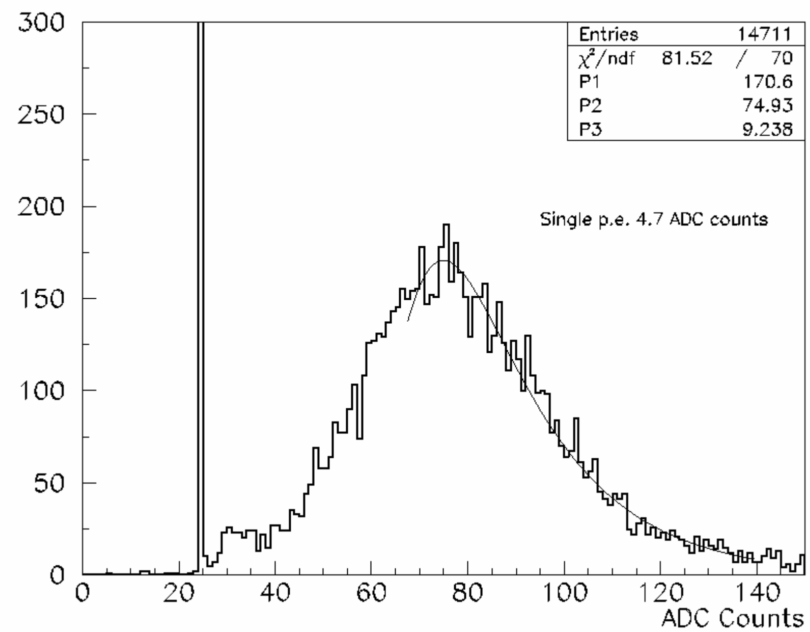
Preshower/Crack PMT Box



Preshower R+D Tests

One-Tower Prototypes built and tested at ANL and Pisa, uniformity and light yield better than specifications. Full-scale prototypes will be built.

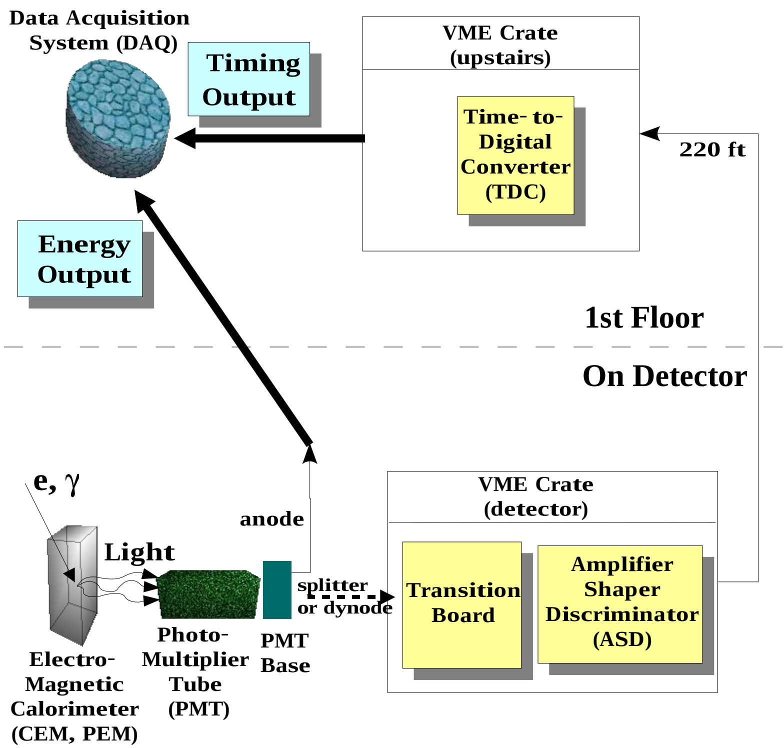




Electromagnetic Timing

- Virtually identical to existing system on hadron calorimeter
- Re-use electronics and well-established technologies
- Add splitters for CEM. PEM already readout-ready
- Build more ASD's
- Recycle TDC's, crate and tracer. Purchase new power supply and processor
- Make cables and connectors

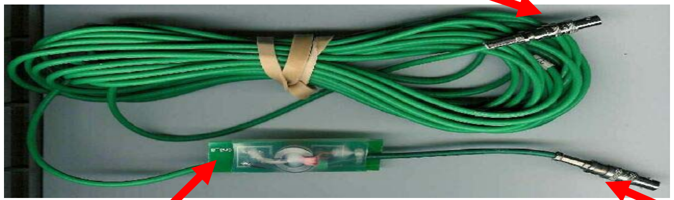
CDF EM Timing Project



Splitters for the CEM

- CEM energy readout cards measure charge. Splitter is purely inductive so it doesn't change the charge collected in any noticeable way.
- ~15% of voltage goes on the secondary to the ASD to fire the TDC

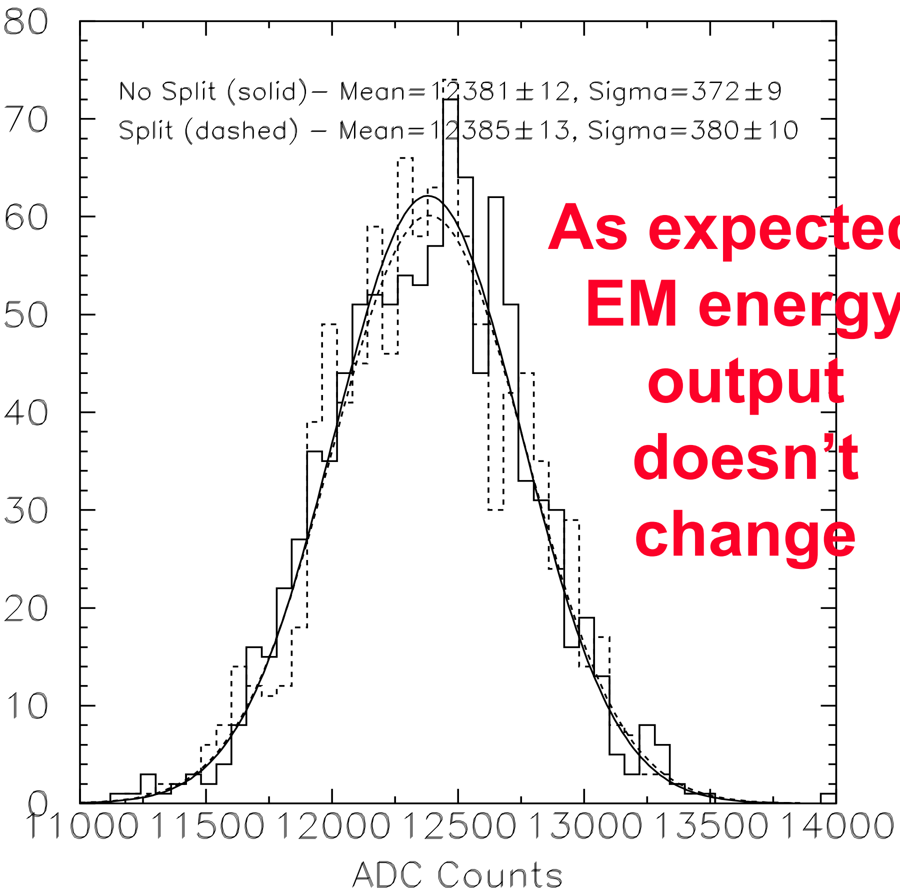
Male LEMO to ASD transition board



Female LEMO to ADMEM input (on back)

Male LEMO to PMT anode

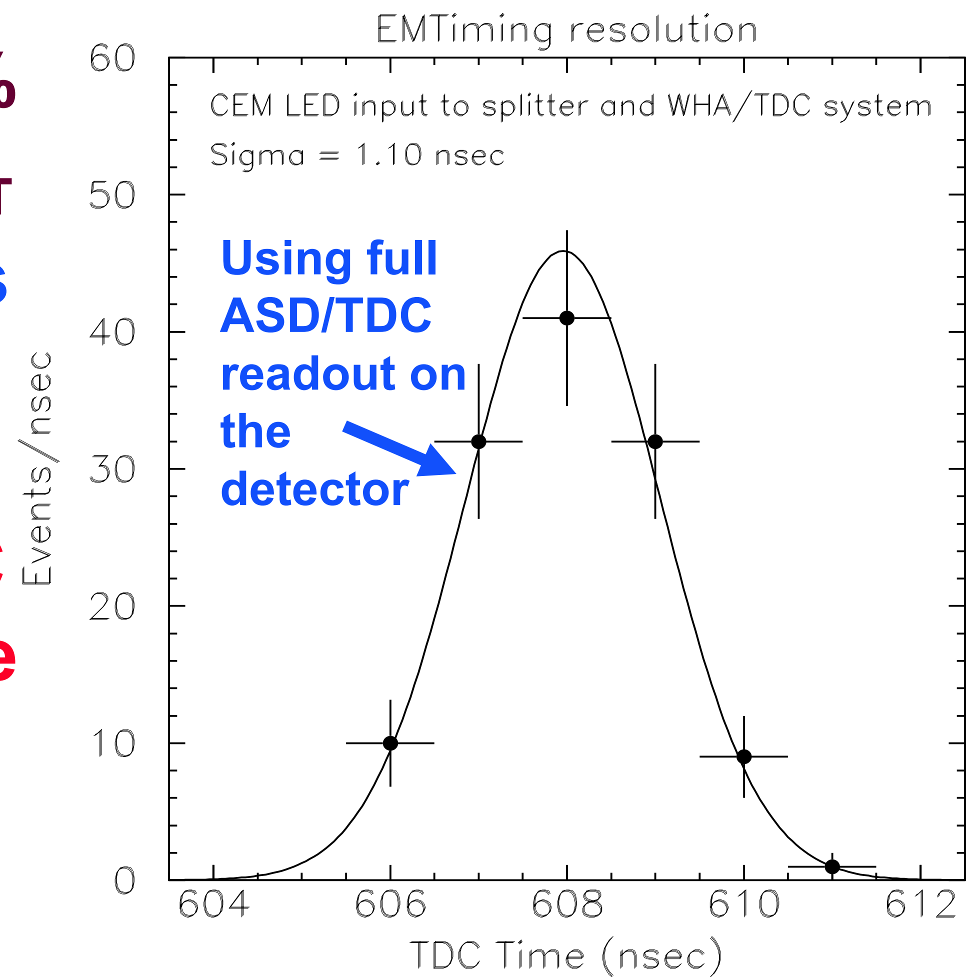
Prototype response at 40 GeV



As expected, EM energy output doesn't change

Splitter characteristics

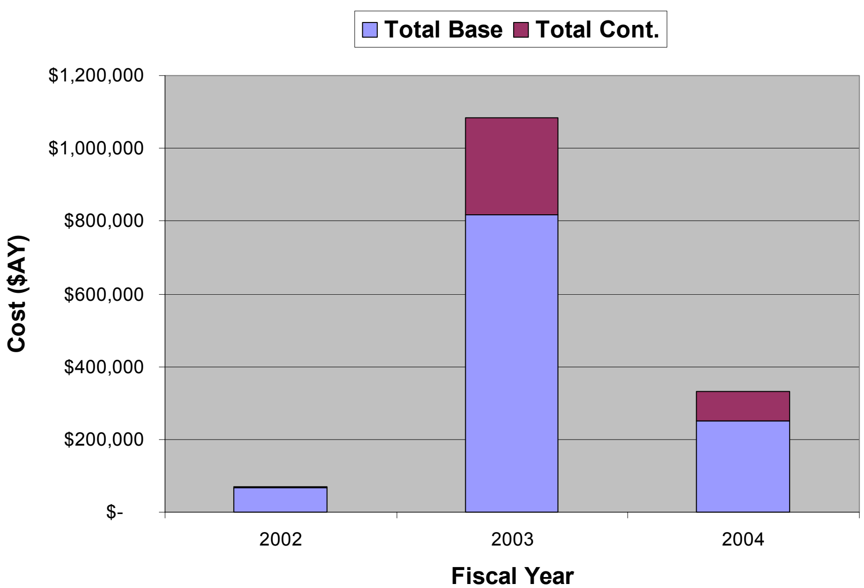
- ASDs fire with 100% efficiency at high E_T
- Timing resolution is ~1.1nsec (1.0 from TDC)
- No evidence of TDC misfiring from noise
- No evidence of noise going to ADMEM's



Total Calorimetry Costs

AY $	2002	2003	2004	2005	2006	Totals
Total Base(incl R&D)	$ 66,793	$ 816,279	$ 249,837	$ -	$ -	$ 1,132,909

- 73% Preshower
- 27% Timing



AY $

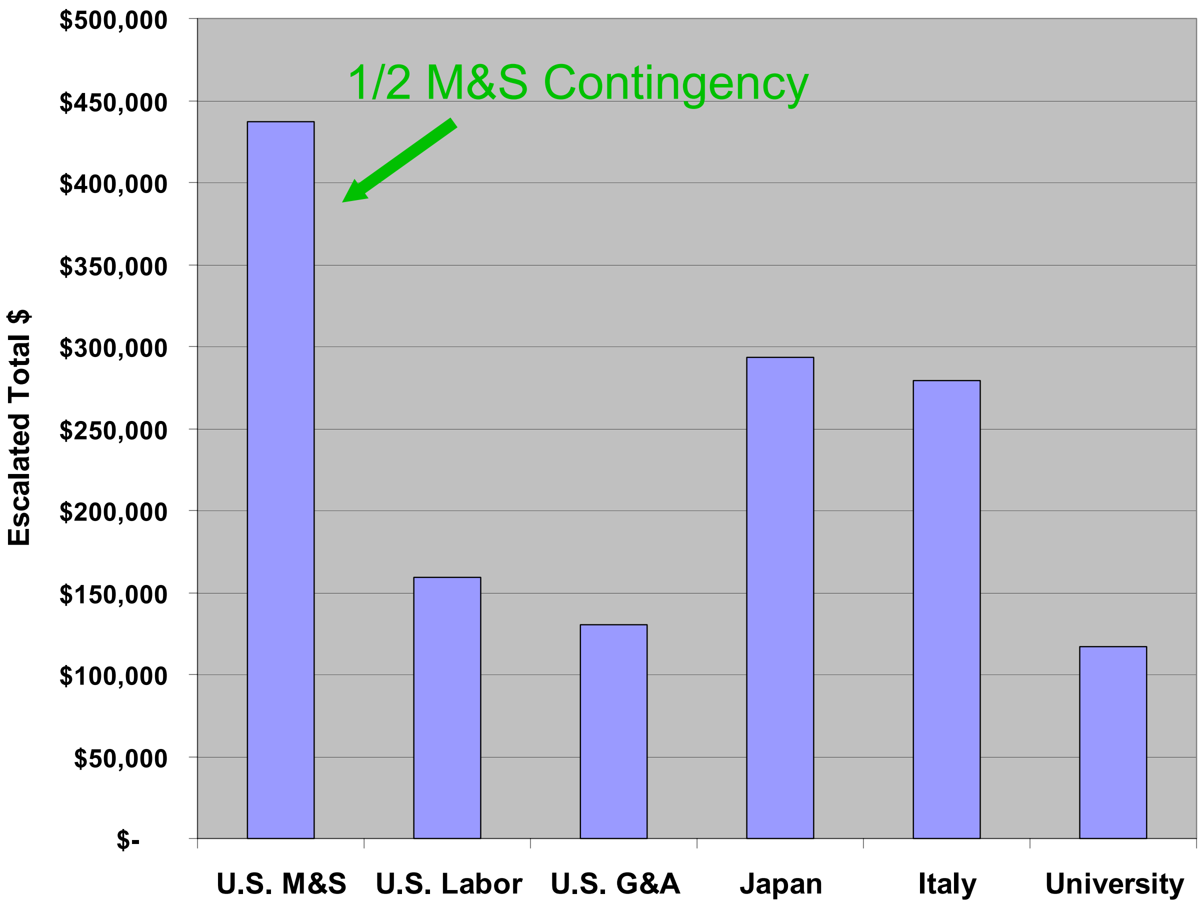
M&S	$	940,855
Labor	$	118,543
G&A	$	73,511
Total Base	$	1,132,909

Total Cont. – $363 K AY

Total Cost + Cont –

$1,496 K AY

Funding Sources



U.S. M&S	$	437,231
U.S. Labor	$	159,550
U.S. G&A	$	130,113
Japan	$	293,540
Italy	$	279,290
University	$	117,061

U.S numbers include contingency

Calorimetry Level 3 Milestones

First phototube order placed	Mon 2/17/03
ASD->TDC Cables ready for installation	Fri 4/4/03
CEM Splitters ready for installation	Fri 4/11/03
Prototype Testing Complete	Thu 5/15/03
1st WLS fiber holder finished	Mon 7/14/03
PEM Harnesses ready for installation	Tue 9/2/03
All cables done and ready for installation	Tue 9/2/03
1st CPR module finished and tested	Tue 9/16/03
VME Crate ready for installation	Tue 10/7/03
First set of phototubes tested	Wed 10/29/03
1st CCR module finished and tested	Tue 11/11/03
ASD/TB ready for installation	Wed 1/7/04
Downstairs components ready for installation	Wed 1/7/04
TDC boards ready for installation	Wed 1/7/04
Upstairs components ready for installation	Wed 1/7/04
All EMTiming components ready for installation	Wed 1/7/04
Second set of phototubes tested	Fri 2/27/04
50% CPR Detectors Tested	Thu 3/11/04
50% CCR Detectors Tested	Fri 6/4/04
Final CPR Detector Tested	Mon 8/30/04
Final CCR Detector Tested	Mon 8/30/04
Final set of phototubes tested	Wed 10/13/04
End of Central Preshower Project	Wed 10/13/04
End of Calorimetry Project: Level 3	Wed 10/13/04

Calorimeter Summary

- CDF Calorimeter Upgrades needed to do the physics of Run IIB, including the Higgs and New Physics searches involving Photons.
- Hardware choices made to minimize costs, minimize R+D, and minimize technical risks.
- Upgrades should be finished and ready to install by the end of 2004.

Calorimeter Summary

- CDF Calorimeter Upgrades needed to do the physics of Run IIB, including the Higgs.
- Hardware choices made to minimize costs, minimize R+D, and minimize technical risks.
- Upgrades should be finished and ready to install by the end of 2004.

Run IIb Trigger/DAQ Upgrades

Outline:

- Motivation
  - Run IIb physics goals
  - Trigger strategies
- Specific projects
  - Specific issues
  - Design
- Cost
- Schedule
- Conclusion

The upgrades:

1.3.1 TDC replacement
- Central tracker readout

1.3.2 Level 2 trigger
- Level 2 decision crate

1.3.3 XFT upgrade
- Level 1 track trigger

1.3.4 Event builder

1.3.5 Level 3 processor
- Data acquisition

1.3.6 SVT
- silicon vertex trigger

Motivation

- The DAQ/Trigger upgrades presented here are driven exclusively by our Run IIb trigger and data acquisition needs to carry out our high-p_T physics program

- Our current level of understanding is based upon
  - **Run IIa data: $\mathcal{L} \leq 2\text{x}10^{31}\ \text{cm}^{-2}\ \text{s}^{-1}$, ~1 interaction per crossing**
  - **Run I data: $\mathcal{L}$ ~2x$10^{31}\ \text{cm}^{-2}\ \text{s}^{-1}$, ~2 interactions per crossing**

- We are extrapolating to Run IIb
  - **$\mathcal{L} = 2\text{x}10^{32}\ \text{cm}^{-2}\ \text{s}^{-1}$ w/396ns bunch spacing (~5 int/beamX)**
  - **$\mathcal{L} = 5\text{x}10^{32}\ \text{cm}^{-2}\ \text{s}^{-1}$ w/132ns bunch spacing (~5 int/beamX)**
  - **Due to significant uncertainties in extrapolation, and a desire to be prepared for success, we have evaluated our system for: $\mathcal{L} = 4\text{x}10^{32}\ \text{cm}^{-2}\ \text{s}^{-1}$ w/396ns bunch spacing (~10 int/beamX)**

Trigger Strategy

- Focus on Higgs & high p_T searches
  - Know that triggers needed for these modes will allow for many beyond Standard Model searches
- General requirements:
  - High p_T electrons and muons
    - Associated *WH*/*ZH* modes, also $t \to Wb$
  - Missing E_T triggers
    - *ZH* with $Z \to \nu\bar{\nu}$, modes with taus
  - *b*-jet triggers
    - $H \to b\bar{b}$, *b*-jets tagged by displaced tracks
  - Calibration triggers
    - $Z \to b\bar{b}$, $J/\psi \to \mu^+\mu^-$, photons

Run IIb Trigger Table

trigger path	σ_{L1}(nb)	σ_{L2} (nb)	σ_{L3} (nb)
High E_T electron	1,500	170	30
Plug electron + missing E_T	771	55	10
High P_T muon (CMUP)	1,773	200	8
High P_T muon (CMX)	1,773	200	8
2 high pT *b*-jets	10,840	200	10
missing E_T + 2jets	163	126	13
jets	6,500	42	12
missing E_T	overlap	163	3
Photons	overlap	50	15
$J/\psi \rightarrow \mu^+\mu^-$	850	38	10
High P_T jets	19,000	60	17
hadronic top	overlap	50	5
di-τ	5,000	50	4
missing E_T+τ	overlap	50	4
High E_T photons	13,500	110	21
dileptons, trileptons	1,000	190	45
total	**59,200**	**1904**	**215**
rate @4E32	**25kHz**	**750Hz**	**85Hz**
rejection factor	**~100**	**~33**	**~9**

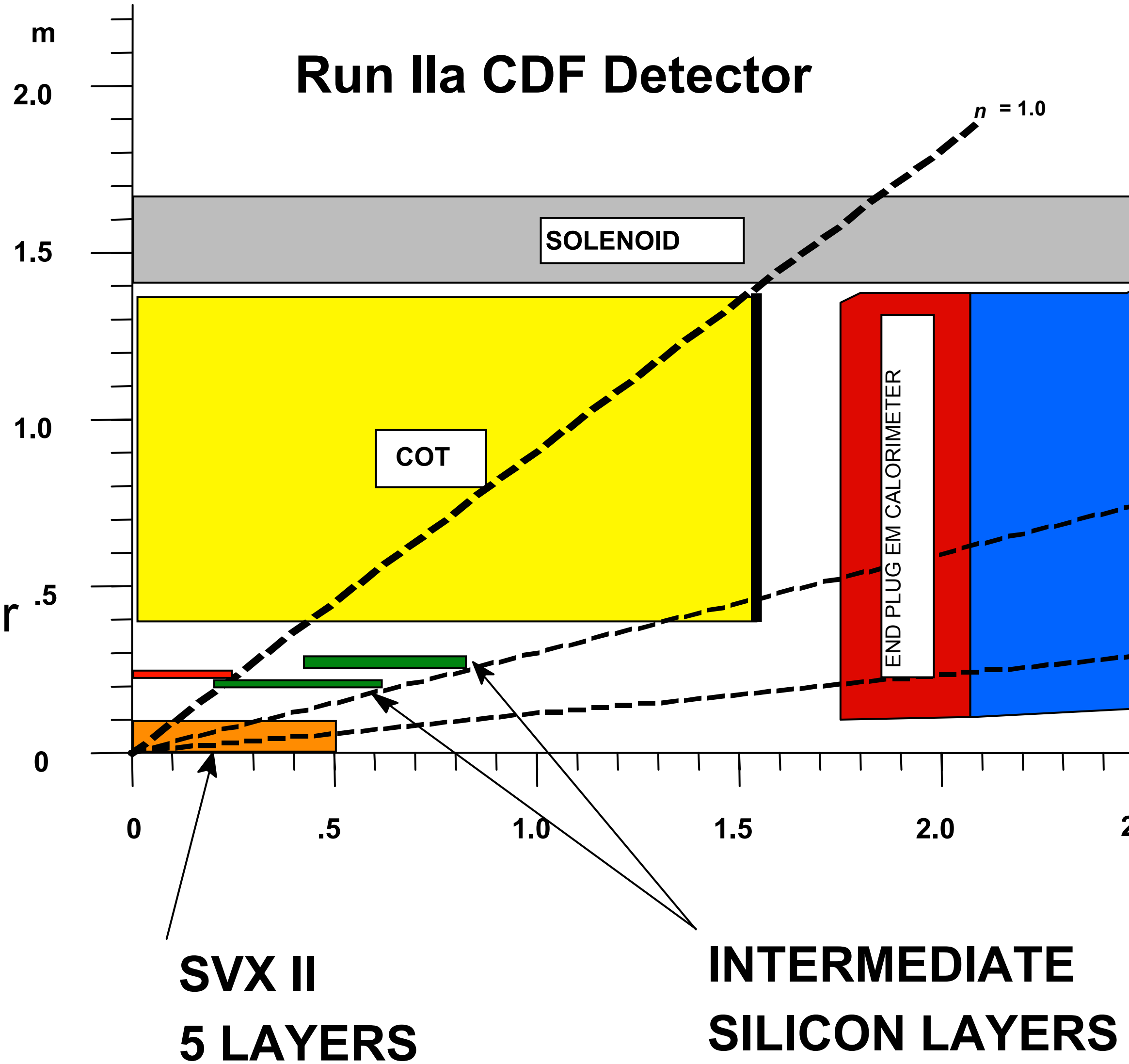
Summary of Run IIb specifications

- **Level 1 Accept rate: >25kHz (spec 50kHz)**
  - **deadtimeless**
- **Level 2 Accept rate: 750 Hz →bursts to 1.1kHz**
  - **L2 processing deadtime < 5%**
  - **readout deadtime (on L2A) < 5%**
- **Level 3 Accept rate: 85Hz**
  - **Event builder rate: 400MB/s**
  - **Output data rate: 40MB/s**

- Reminder: trigger & bandwidth rates estimated based upon Run IIa, significant underestimate possible (assumes linear growth in fake contribution)

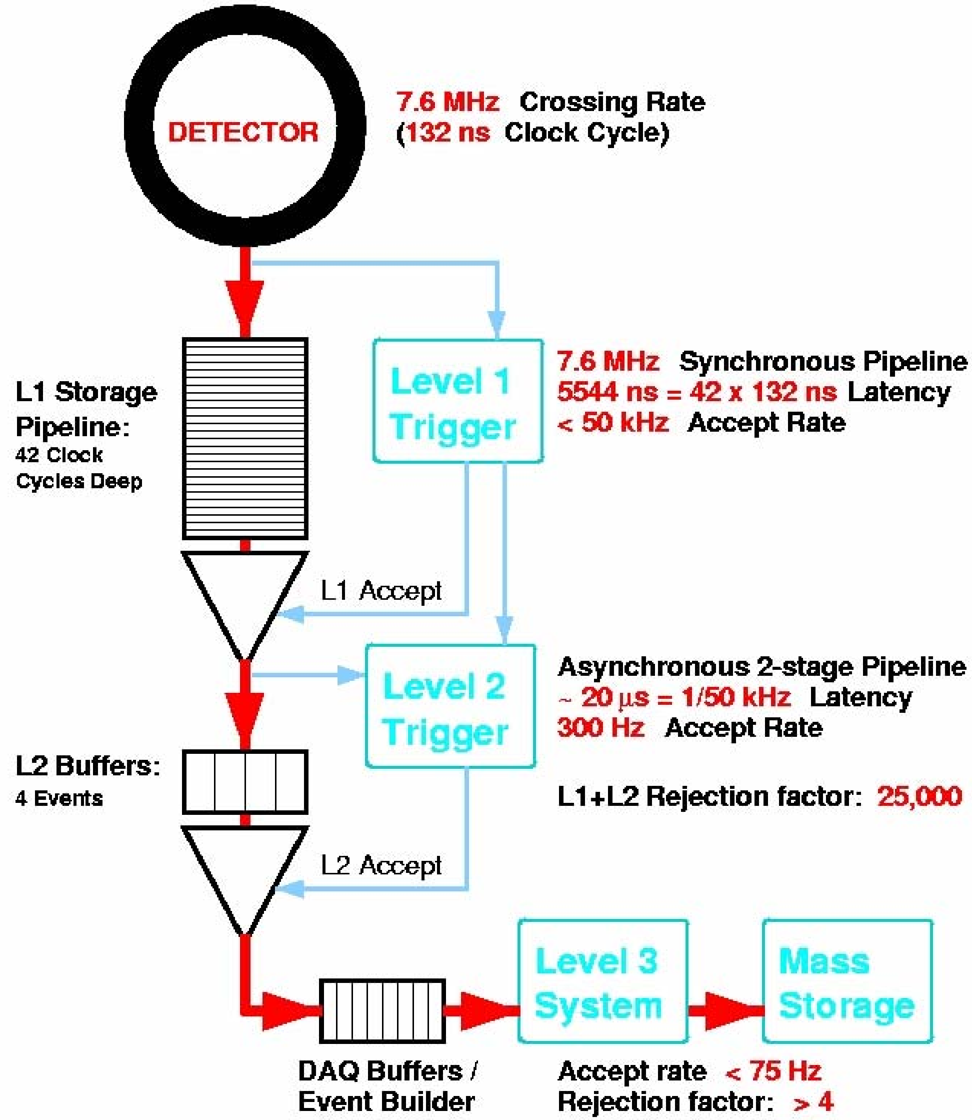
The CDF Detector

- Important detector element for this talk is the Central Outer Tracker (COT)
  - drift chamber with 30k sense wires
  - solenoid field is 1.4T
  - track needs p_T~75 MeV to get to COT inner layer
  - tracks with $|\eta|<1$ pass through all COT layers
  - inner layers see tracks with $|\eta|<2$



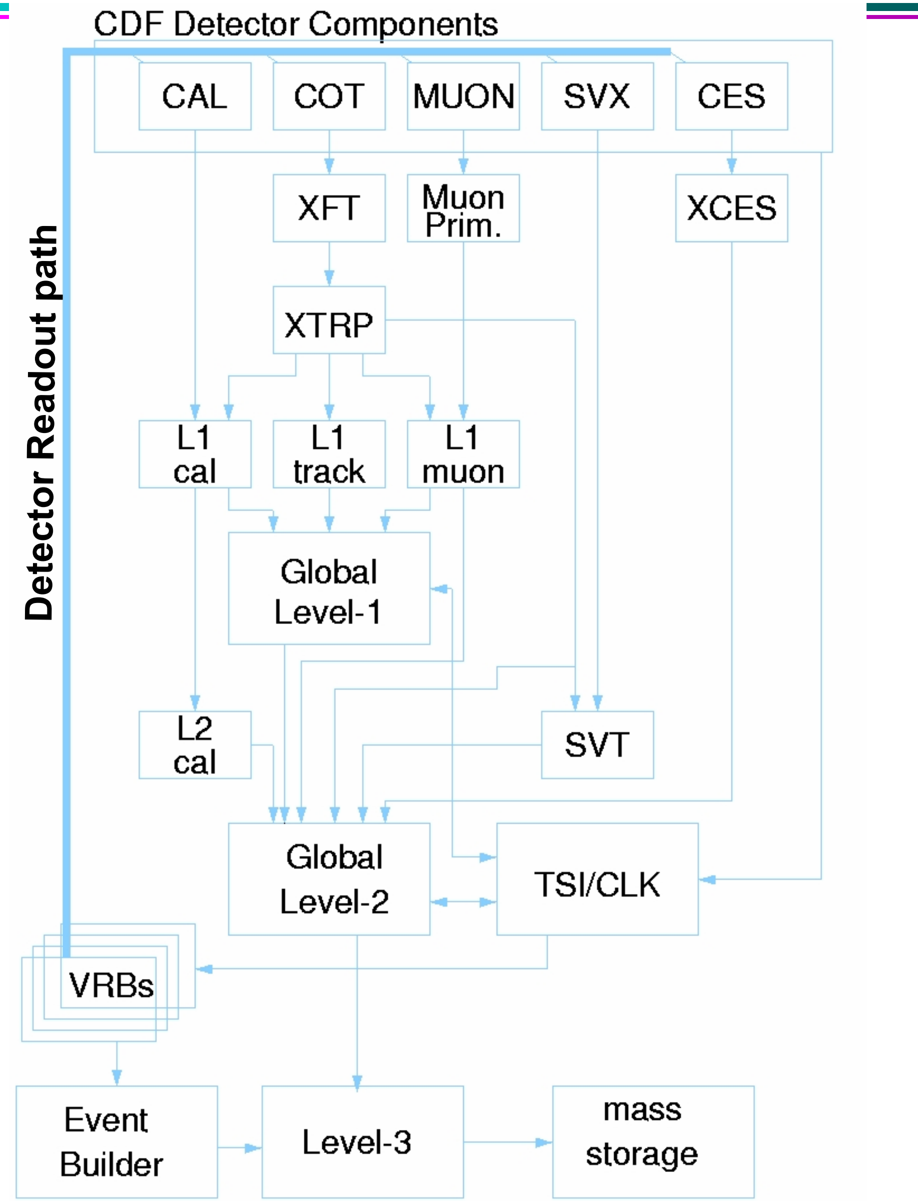
CDF Data Acquisition System

- Level 1 trigger
  - pipelined and "deadtimeless"
  - fully synchronous
  - designed for 132ns operation
  - on L1A, write data to 1 of 4 local L2 buffers
- Level 2 trigger
  - asynchronous
  - L1 + supplemental info
- Level 3 trigger
  - full detector readout
  - PC farm runs reconstruction
  - output to mass storage



CDF Run II Trigger System

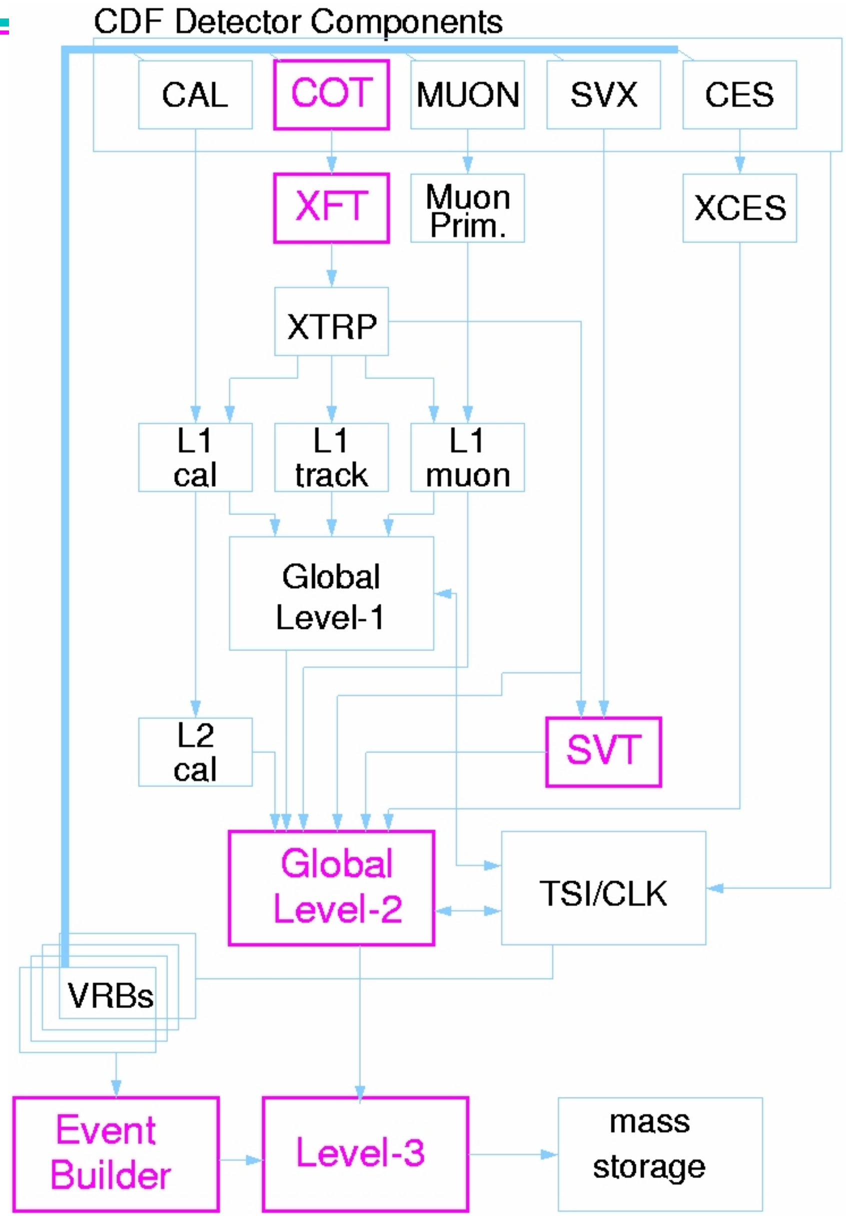
- Level 1 trigger
  - tracking
  - calorimeter: jets & electrons
  - muons
- Level 2 trigger
  - L1 information (tracks, e, μ)
  - calorimeter shower max
  - silicon information
  - algorithms run in L2 processor
- Level 3 trigger
  - full detector readout
  - “offline” processing



Trigger/DAQ Upgrades for Run IIb

General considerations:

- upgrades "targeted" to specific needs
  - *e.g.* COT TDCs replaced, but remaining COT readout (ASDQ, repeaters) unmodified
- retain existing infrastructure
  - cables, crates unchanged
  - I/O protocols, timings retained
  - upstream/downstream components unchanged
- upgrades plug compatible with existing components
  - take advantage of knowledge & experience
  - will aid in commissioning



COT TDC Upgrade

Central Outer Tracker (COT)

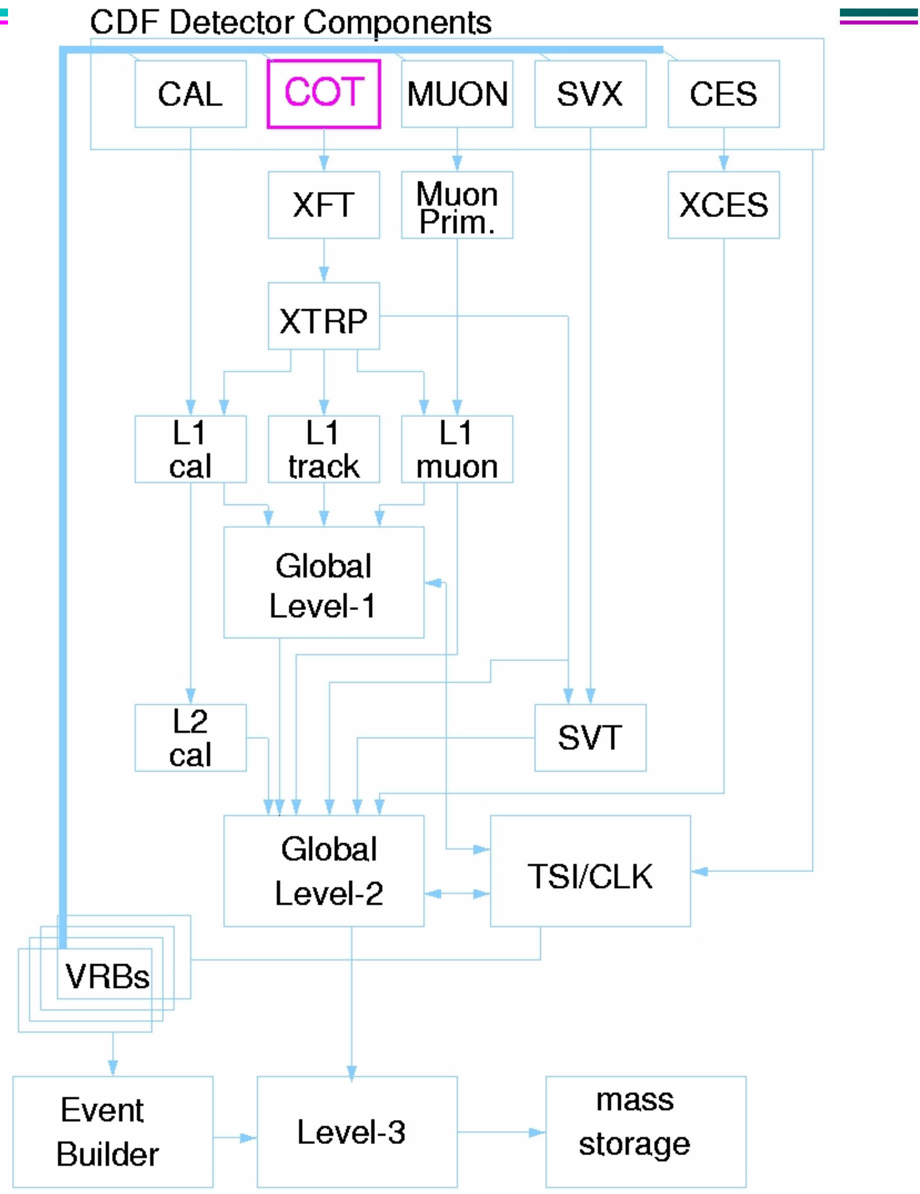
- central drift chamber

COT readout path:

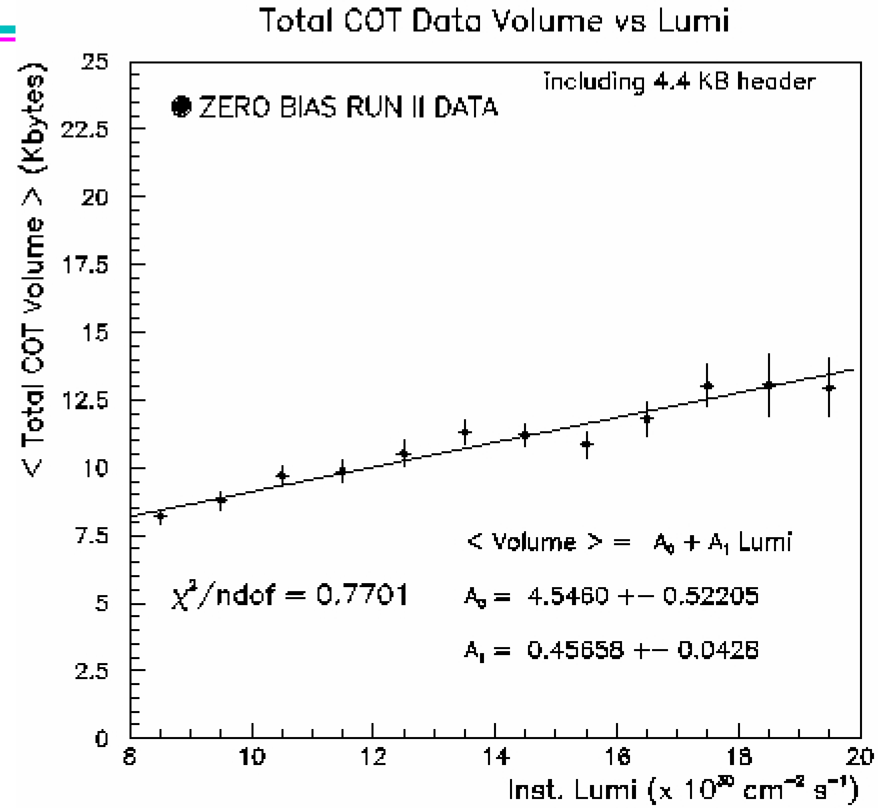
chamber→ASDQ → microcoax → repeater board →flat cable →TDC

ASDQ = amplifier shaper discriminator with charge-encoding

TDC = time-to-digital conversion



TDC Replacement



Limitations of current system:

- TDC on-board data processing
  - existing system performs hit processing after L2A
  - processing time (=deadtime) grows with # of hits
  - COT occupancy higher than expected
  - Run IIa processing time too large for Run IIb
- VME readout
  - 16 TDCs per crate read out serially by VME block transfer
    - current VME transfer rate 14MB/s with additional overhead per board
    - Run IIa, 300Hz…falls to ~150Hz (!) in Run IIb
- Data transfer
  - TRACER→TAXI→VRB link provides bandwidth limitation
    - maximum TAXI →VRB is <12MB/s…Run IIb requires 14MB/s

Run IIb TDC Performance

Specification: entire TDC readout must be completed within 600μs to handle 1.1kHz rate ⇒ 14MB/s.

- **TDC (on-board) processing time [time after L2A]**
  - Now: slowest TDC >650μs/event
  - Need ~360μs to achieve 1kHz L2A rate
- **VME readout**
  - Currently: ~ 500μs per crate
  - Run IIb: x10 more data ⇒ >1ms
- **Data transfer**
  - Run IIb: expect 14MB/s, TAXI link limited to <12MB/s

- Internal CDF TDC Review committee convened in June

  Conclusion:
  - existing COT TDCs + VME readout system cannot maintain necessary L2A rate in Run IIb
  - TDC system must be replaced **OR** significant modifications to the DAQ & infrastructure must take place

New TDC Design

- Address on-board processing deadtime by moving hit processing into the L1→L2 transition
  - “hide” hit processing behind L2 trigger
- Address VME and Readout problems via bypassing the VME→TRACER→TAXI
  - Keep existing data path as a backup (commissioning)
  - Maintain other pieces of DAQ chain (VRB →EVB)
- Design exclusive to COT system, reduces constraints
  - Run IIa TDC will continue to work well for other systems (muons, hadron timing, CLC)

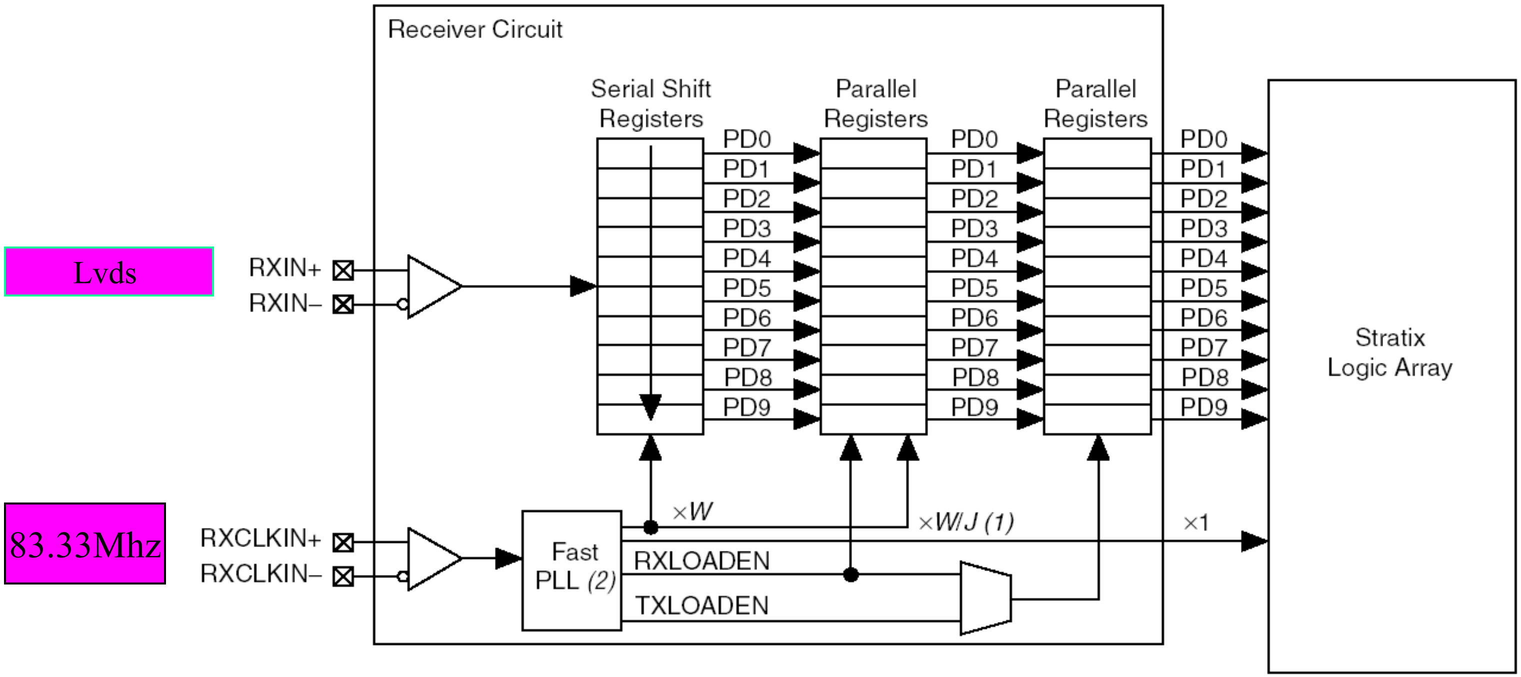
TDC Specifications

- Backward compatible with existing system
  - No change to COT front-end, cables or calibration
  - No change to track trigger (XFT) interface
  - Accept CDF specific signals from CDF_CLOCK/TRACER
- Must handle the following rates
  - 50kHz L1A, 1.1kHz L2A
  - Readout time below 500μs with 20kB/crate
- Allow for on-board data compression
- Perform hit finding for track trigger
- "TDC Specifications" document provides details

New TDC Design

- Done with Altera Stratix FPGA
  - commercially available
  - high bandwidth differential input ⇐ **matches COT**
  - sufficient on-chip logic & memory to carry out all needed functions (with room to spare)
  - moderate price
- Time-to-digital conversion performed on chip input
  - 840MHz LVDS inputs
  - not sensitive to routing issues
  - remainder of FPGA functionality digital

Figure 3. Stratix High-Speed Interface Deserialized in ×10 Mode



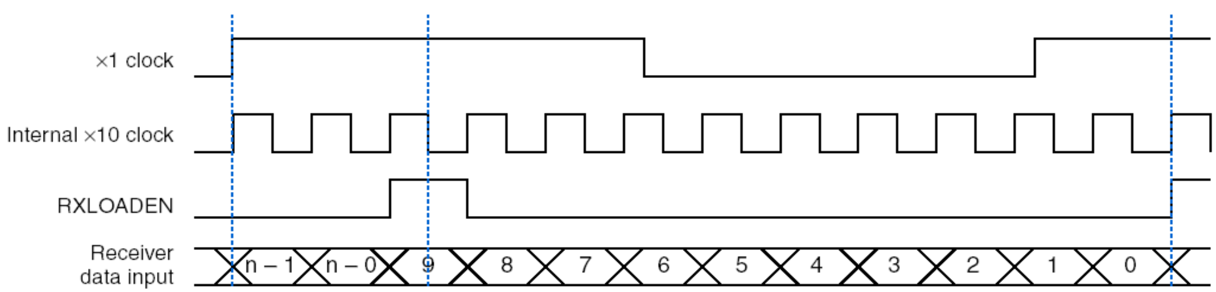
Notes to Figure 3:

W,J=10

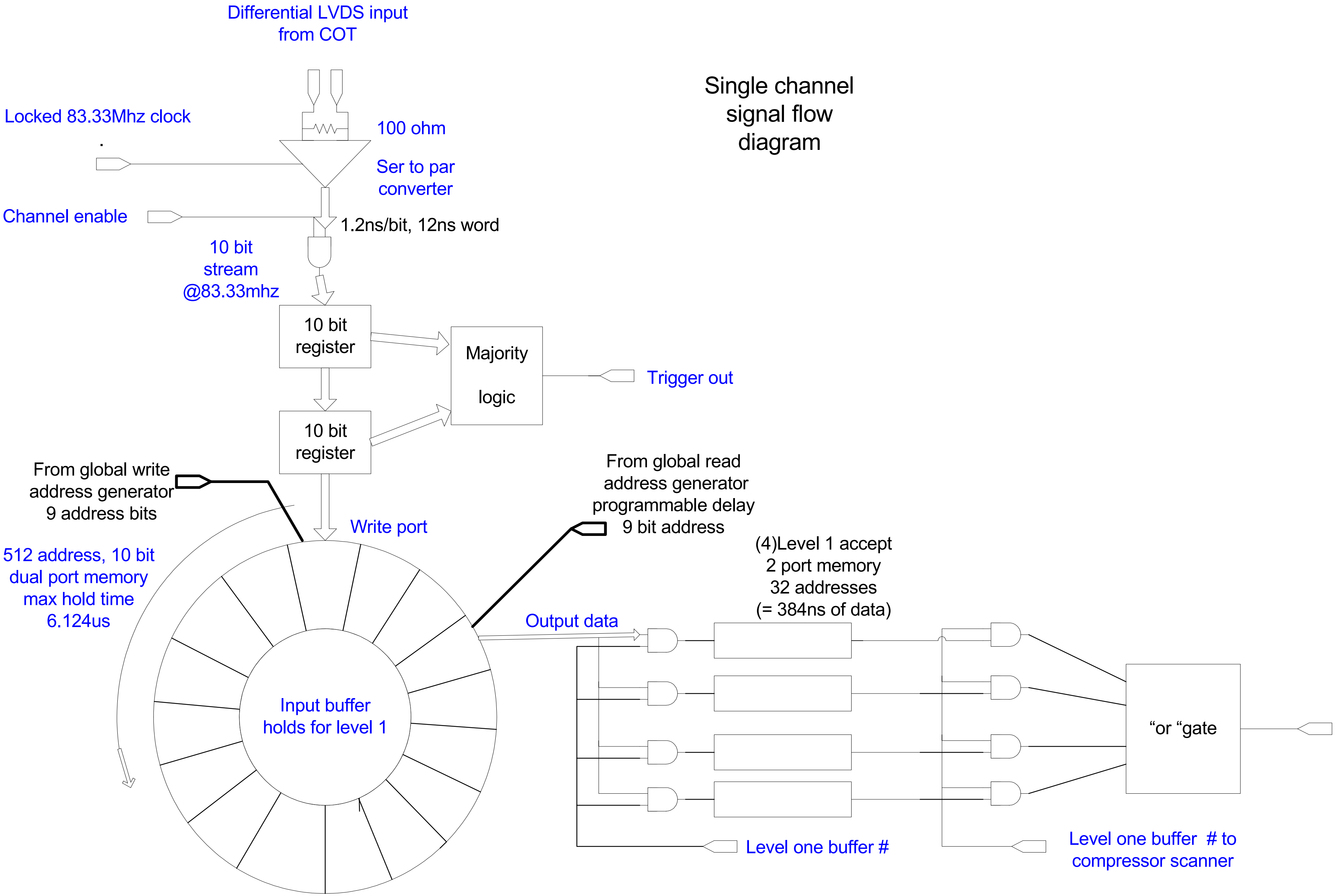
(1) *W* = 1, 2, 4, 8, or 10.
J = 4, 8, or 10.
W does not have to equal *J*. When *J* = 1 or 2, the deserializer is bypassed. When *J* = 2, the device uses DDRIO registers.

(2) This figure does not show additional circuitry for clock or data manipulation.

Figure 4. Receiver Timing Diagram



ALTERA LVDS RECIEVER



Differential LVDS input
from COT
Single channel
signal flow
diagram
Locked 83.33Mhz clock
100 ohm
Ser to par
converter
Channel enable
1.2ns/bit, 12ns word
10 bit
stream
@83.33mhz
10 bit
register
Majority
logic
Trigger out
10 bit
register
From global write
address generator
9 address bits
From global read
address generator
programmable delay
9 bit address
Write port
512 address, 10 bit
dual port memory
max hold time
6.124us
(4)Level 1 accept
2 port memory
32 addresses
(= 384ns of data)
Output data
Input buffer
holds for level 1
"or "gate
Level one buffer #
Level one buffer # to
compressor scanner

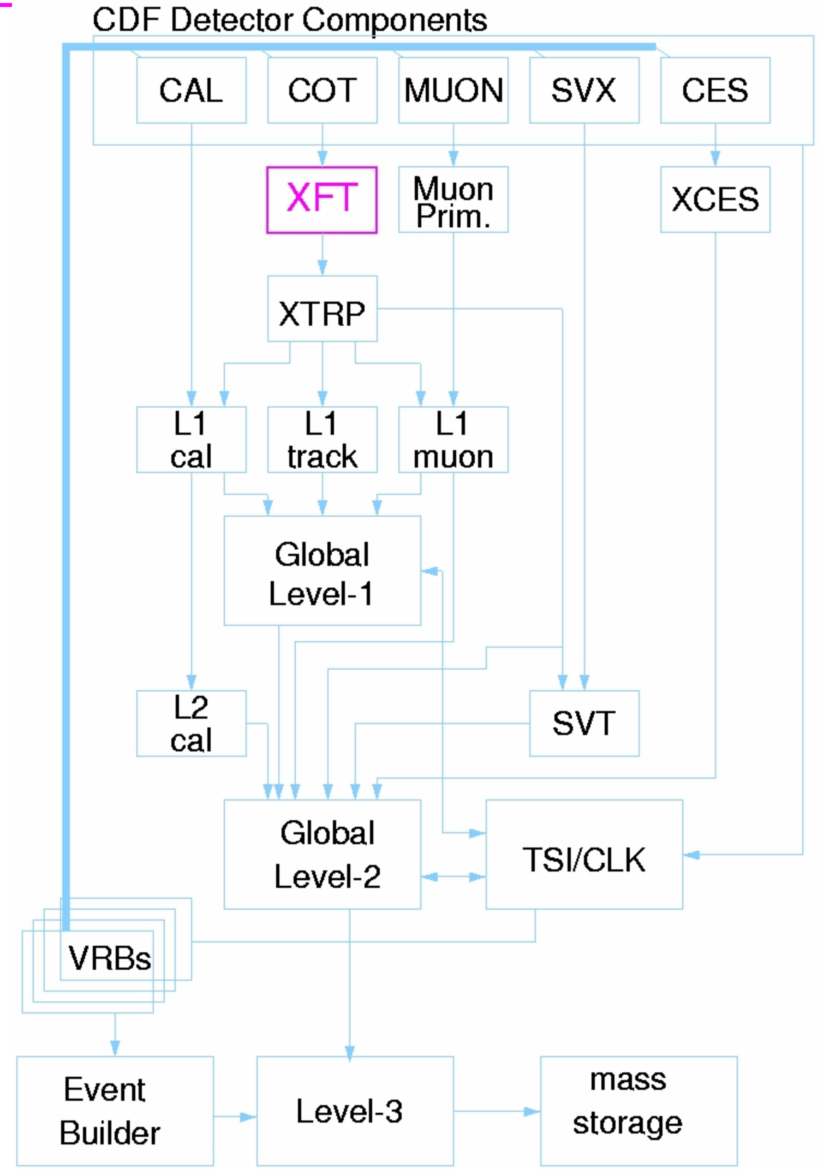
TDC Readout

- TDC readout performed by G-link.
  - TDCs daisy-chained fiber optic to a data concentrator
  - concentrator ships data to VRB
  - VRB supports G-link for SVX readout
- TDC will support Run IIa VME readout for commissioning
  - will be able to install new TDCs into existing system for testing and timing resolution studies

eXtremely Fast Tracker Upgrade

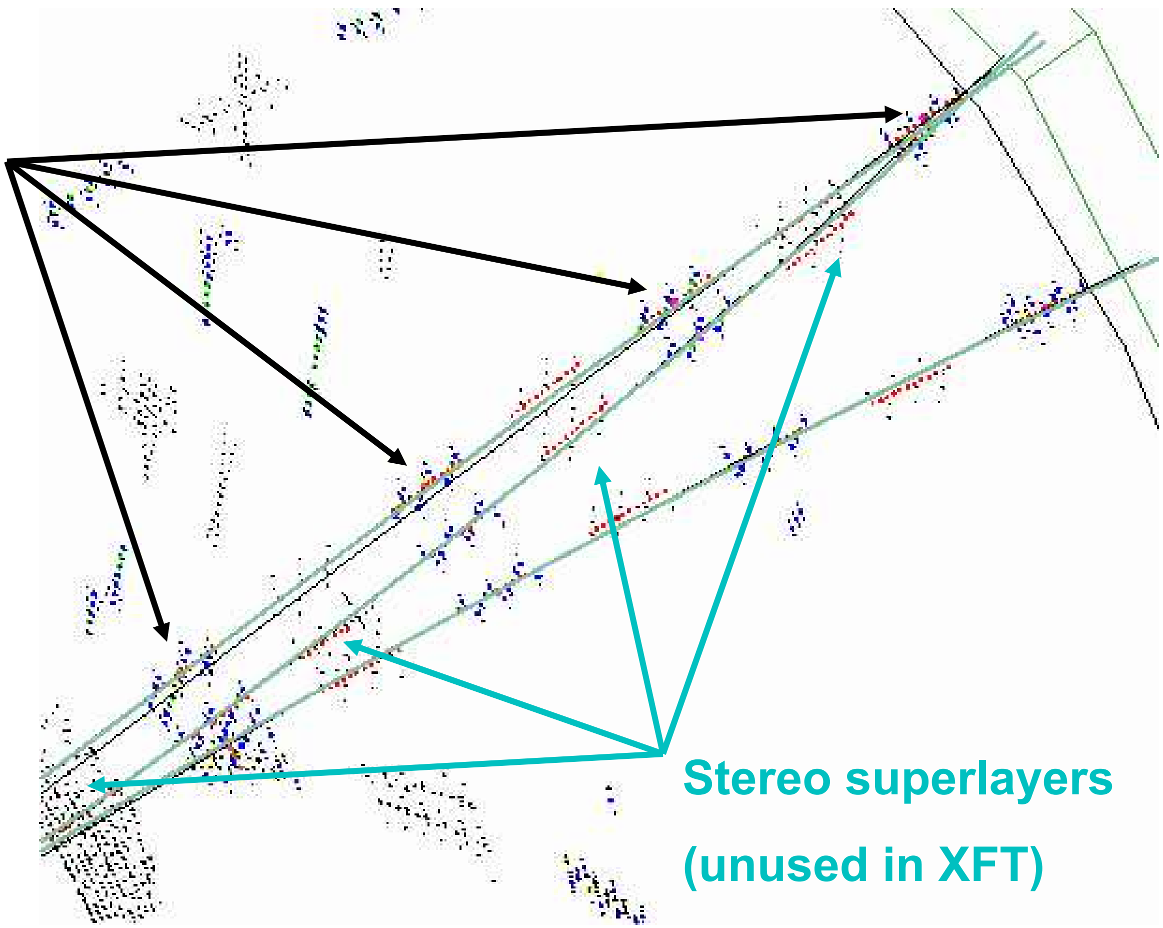
XFT finds charged tracks with $p_T > 1.5$ GeV/c

Part of the Level 1 Trigger system



Run IIa Track Trigger System

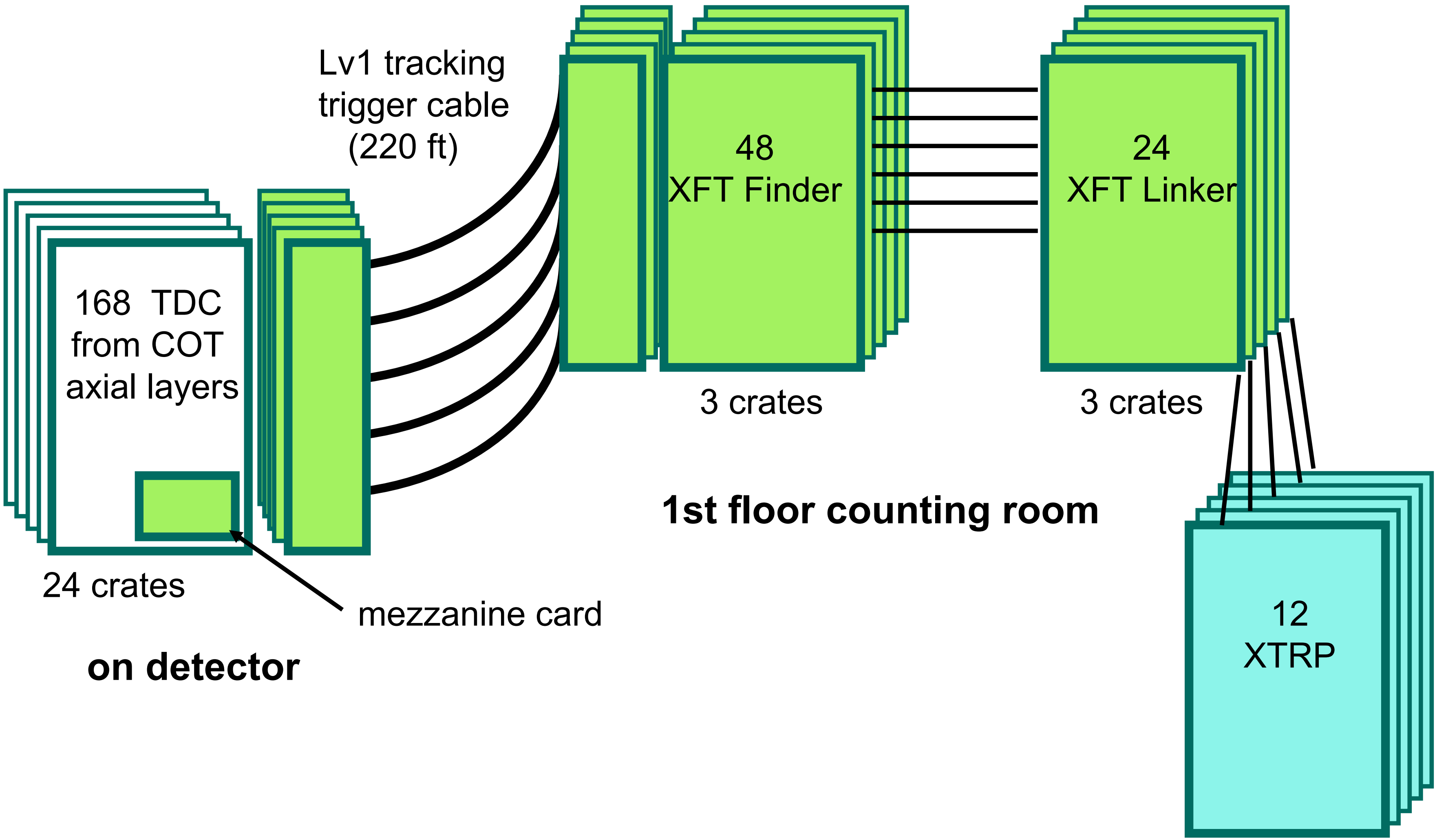
- XFT works by finding line segments in the four axial superlayers
  - “finder” boards



- Tracks are found by linking the segments into tracks
  - “linker” boards

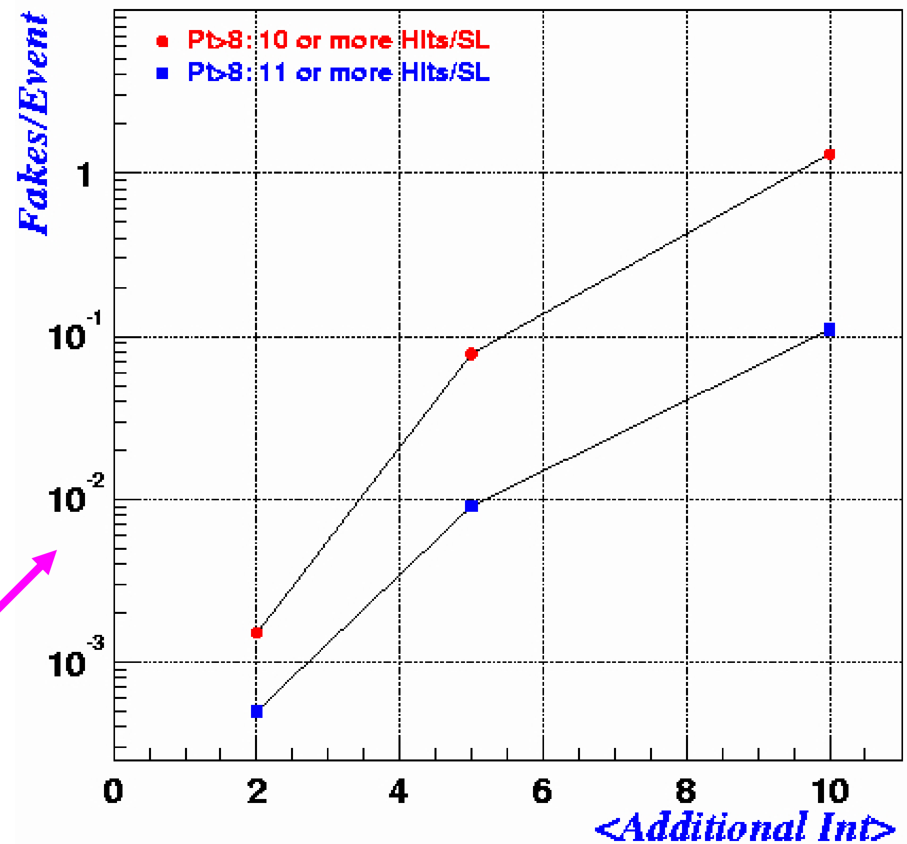
X Interaction point

Run IIa Track Trigger System



XFT Upgrade

- Track-based triggers are responsible for >50% of the Run IIb physics program
  - e, μ, τ, *b*-tags
- COT occupancy at high luminosity causes significant L1 track trigger (XFT) degradation
  - Significant growth in fake track rate (primarily at high p_T)
  - Degradation in p_T and ϕ_0 resolution (next slide)



Minimum bias MC events

XFT p_T & ϕ_0 Resolution

Data: high p_T electrons

+0 minimum bias events

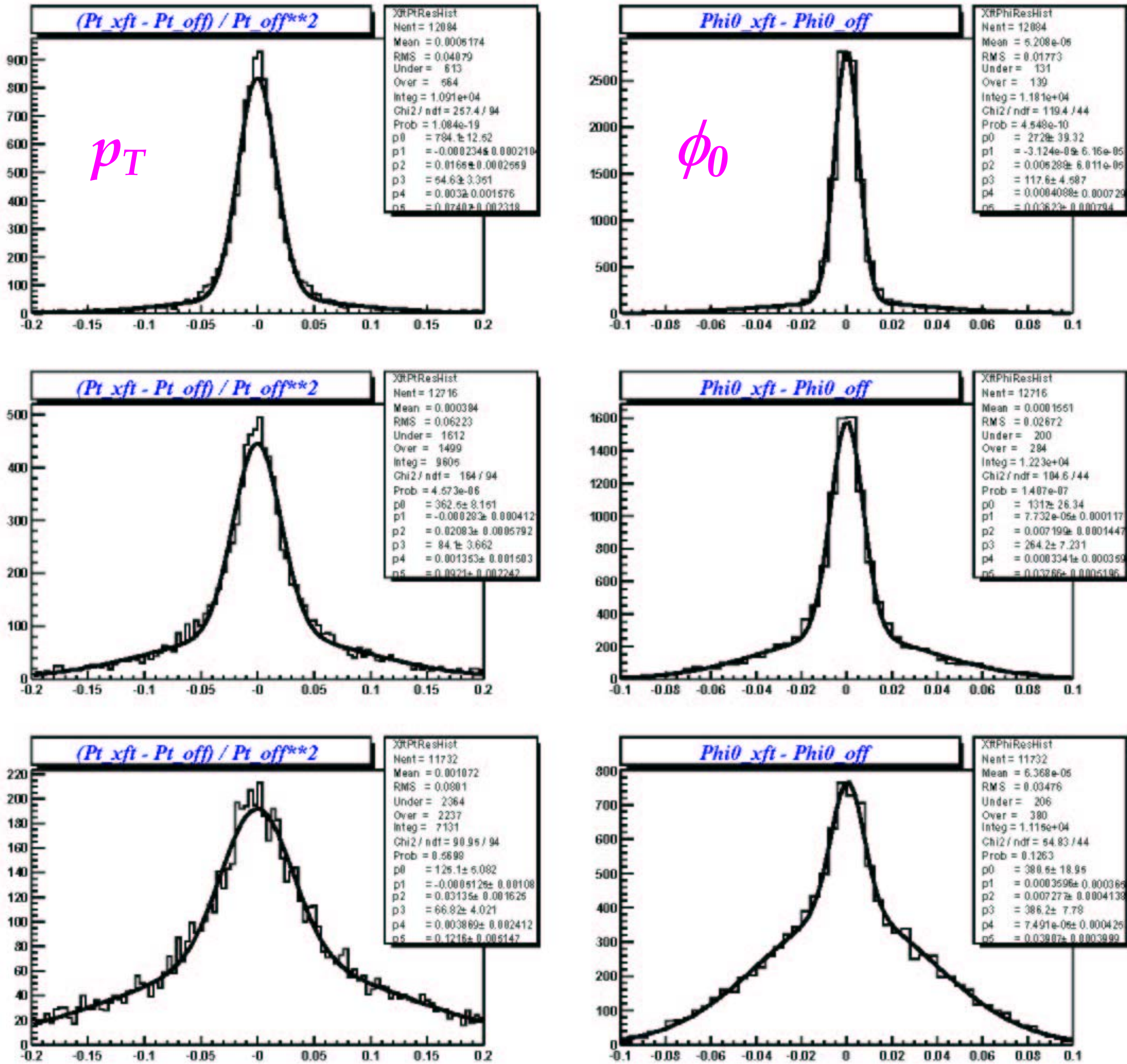
$\mathcal{L}$ = now

+5 minimum bias events

$\mathcal{L} = 2\times10^{32}$ cm^{-2} s^{-1} @396ns

+10 minimum bias events

$\mathcal{L} = 4\times10^{32}$ cm^{-2} s^{-1} @396ns



XFT IIb Design

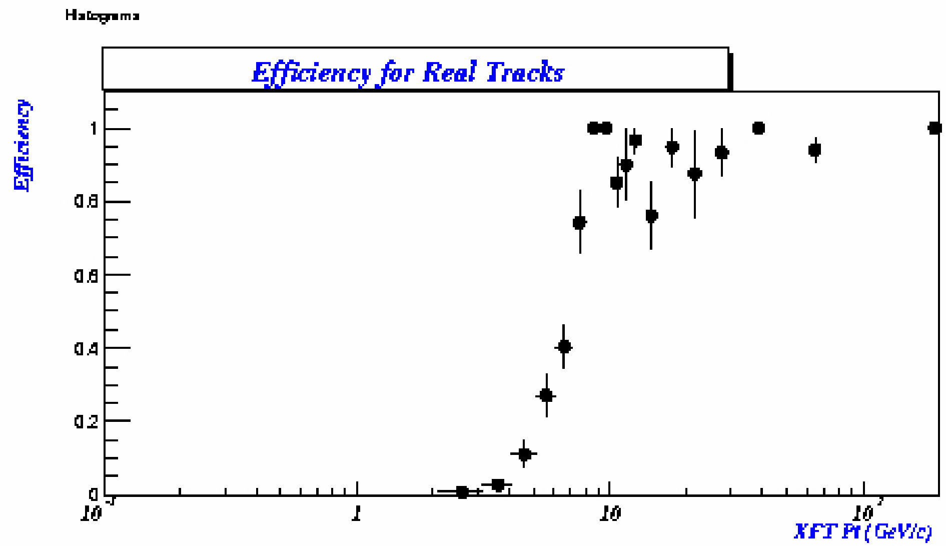
- **Reduce fakes and improve resolution with improved axial track finding & 3D information**
- Take advantage of existing design and infrastructure
  - Cables, I/O, data formats unchanged
- Difference between XFT & offline tracking is time binning. Segment angle match improves with finer time bins.

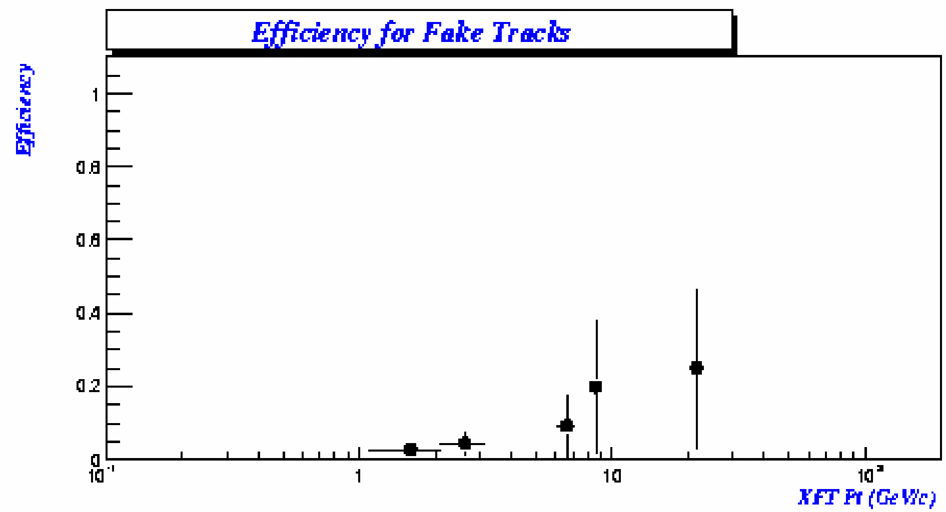
Upgrade:

- Utilize 396ns baseline to pipe more information per beam-X from TDC→XFT.
  - Go from two time bins to six time bins in the trigger
- Supplement axial tracking with stereo measurement
  - Segment finding identical to axial XFT
  - Stereo information provides:
    - improved fake track rejection (important at high $\mathcal{L}$)
    - new: electron & muon matching in η

XFT Upgrade Performance

- Additional timing information plus stereo provides high efficiency for tracks while keeping the fake rate low
- Plots shown are for 10 interactions/crossing
  - high efficiency
  - low fake rate
  - improved p_T and ϕ resolution





XFT Upgrade

What stays the same:

- TDC transition modules
- Cables (TDC XFT)
- Finder transition modules
- Finder backplanes
- Finder Linker cables
- Linker transition modules
- Linker backplanes
- Linker output cables

What changes:

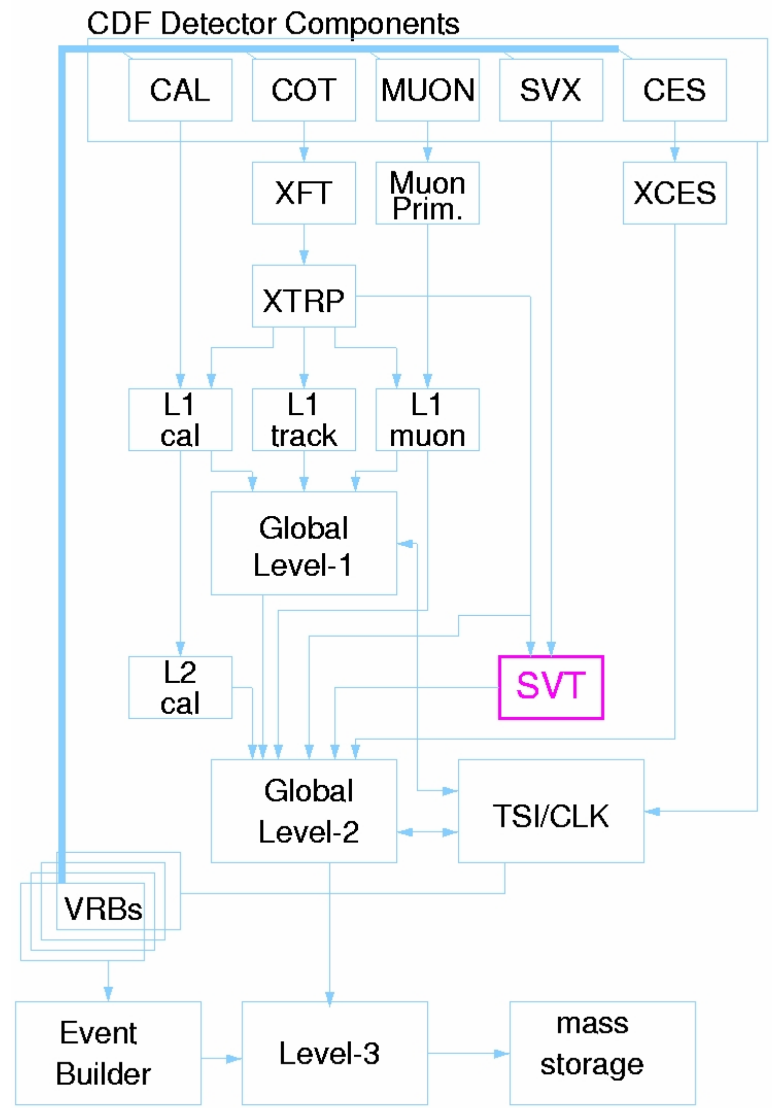
- Finder boards
  - Base functionality identical
  - Input/output circuitry identical
  - New/larger FPGAs, faster internal clock
- Linker boards
  - Base functionality identical
  - Input/output circuitry identical
  - New/larger FPGAs, faster internal clock
- Stereo association modules
  - new: axial-stereo match

SVT Upgrade

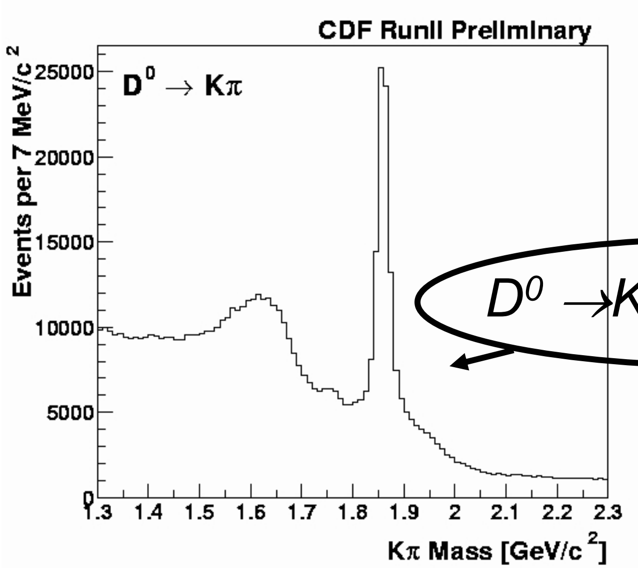
Silicon Vertex Tracker (SVT)

- brings axial silicon information into trigger
- allows for cuts on impact parameter in trigger (!)

- In order to be fast, SVT must specifically handle
  - SVX readout
  - SVX geometry
  - Tevatron beam position

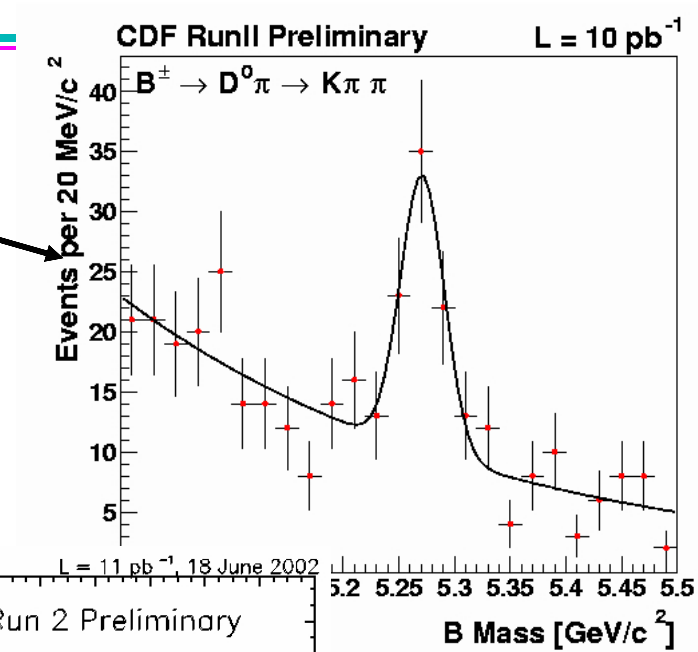


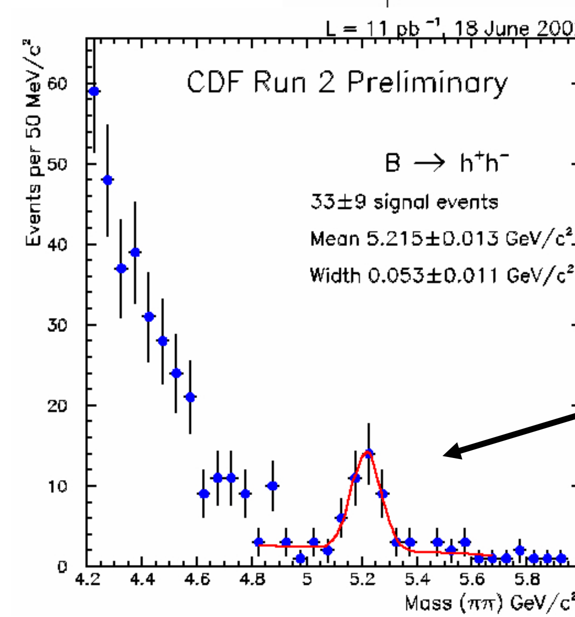
Run IIa SVT



$D^0 \rightarrow K^-\pi^+, K^-K^+, \pi^-\pi^+$

$B^+ \rightarrow D^0\pi^+$





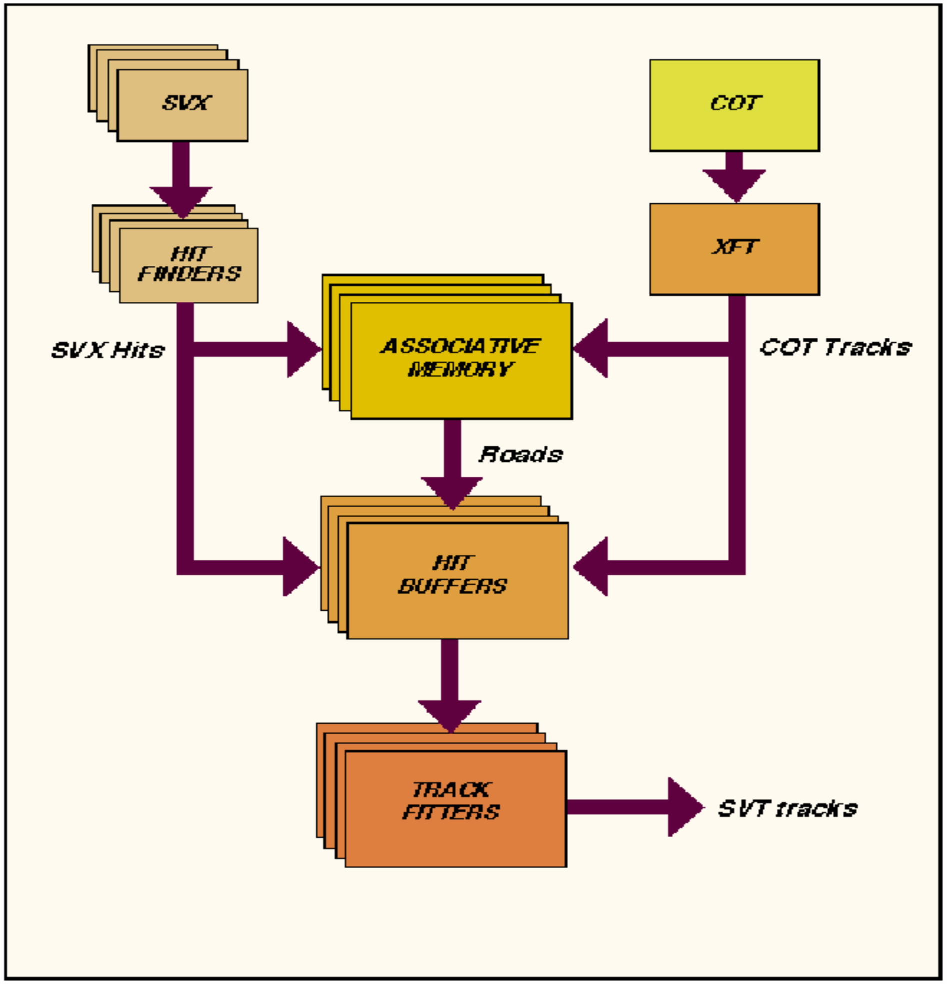
$B^0 \rightarrow h^+h^-$

- Silicon tracking information in the trigger
  - find displaced tracks
  - Run IIb, important for Higgs, SUSY, $Z \rightarrow b\bar{b}$

SVT Upgrade

- SVT is unchanged from the Run IIa system
- SVX IIb geometry different than SVX II geometry
- due to geometry change, SVT in Run IIb requires
  - 12 additional Merger boards
    - layout, functionality identical to existing boards
    - this item is production only
  - new Track Fitter boards
    - layout changes to handle geometry
    - function of board unchanged

SVT architecture

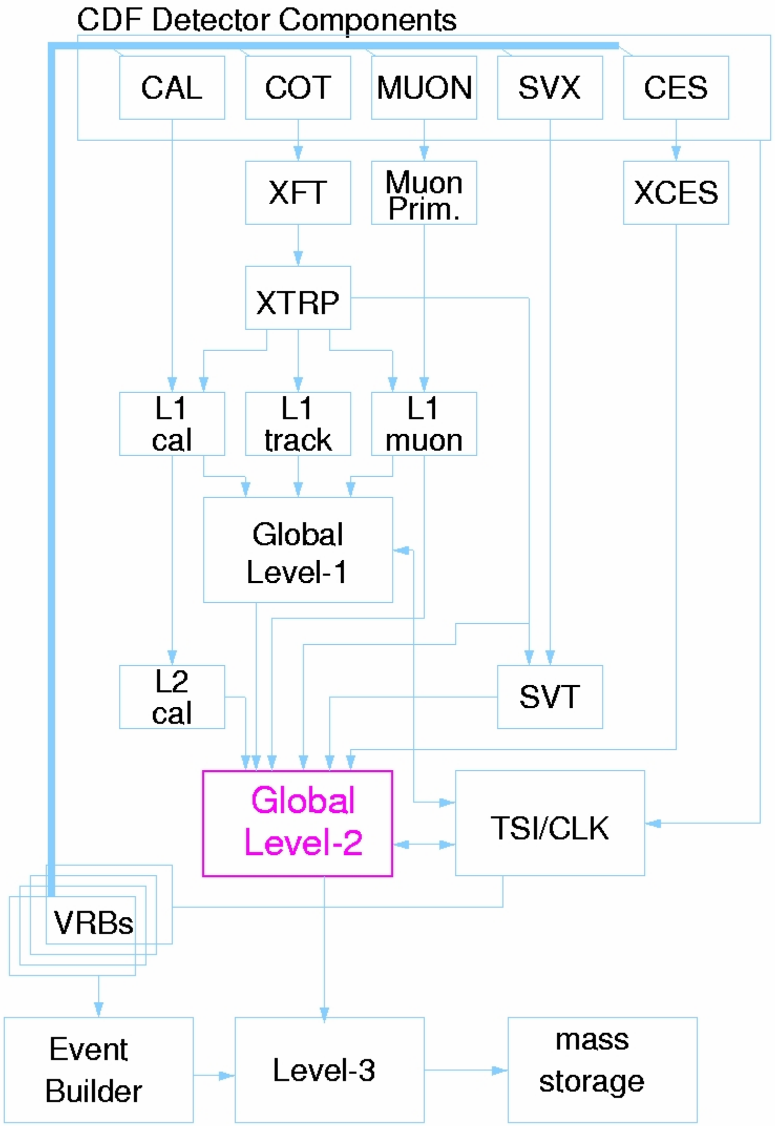


L2 Decision Crate Upgrade

Level 2 trigger receives information from:

- L1 trigger components
  - tracks, muons, jets, missing E_T, electrons
- central strip chambers
- silicon

- Information brought together and fed to processor(s) in the L2 decision crate
  - L2 decision based upon trigger primitives
  - high rate (50kHz) in, must be fast



Run IIa Level 2 Decision Crate

- CDF Level 2 decision crate:
  - 7 different flavors of interface board
    - XTRP,SVT, L1, ISO, MUON, CES, Cluster
    - each uses different input format, different board designs
  - 1 board with Alpha processor for L2 processing/decision
    - system designed to run with 4 Alphas
  - diversity makes system challenging to test & maintain
- Current (in progress) CDF project to build a L2 trigger test-stand system (Pulsar project)
  - will have high speed I/O and buffering capabilities
  - system can source/sink data for **every** L2 interface board

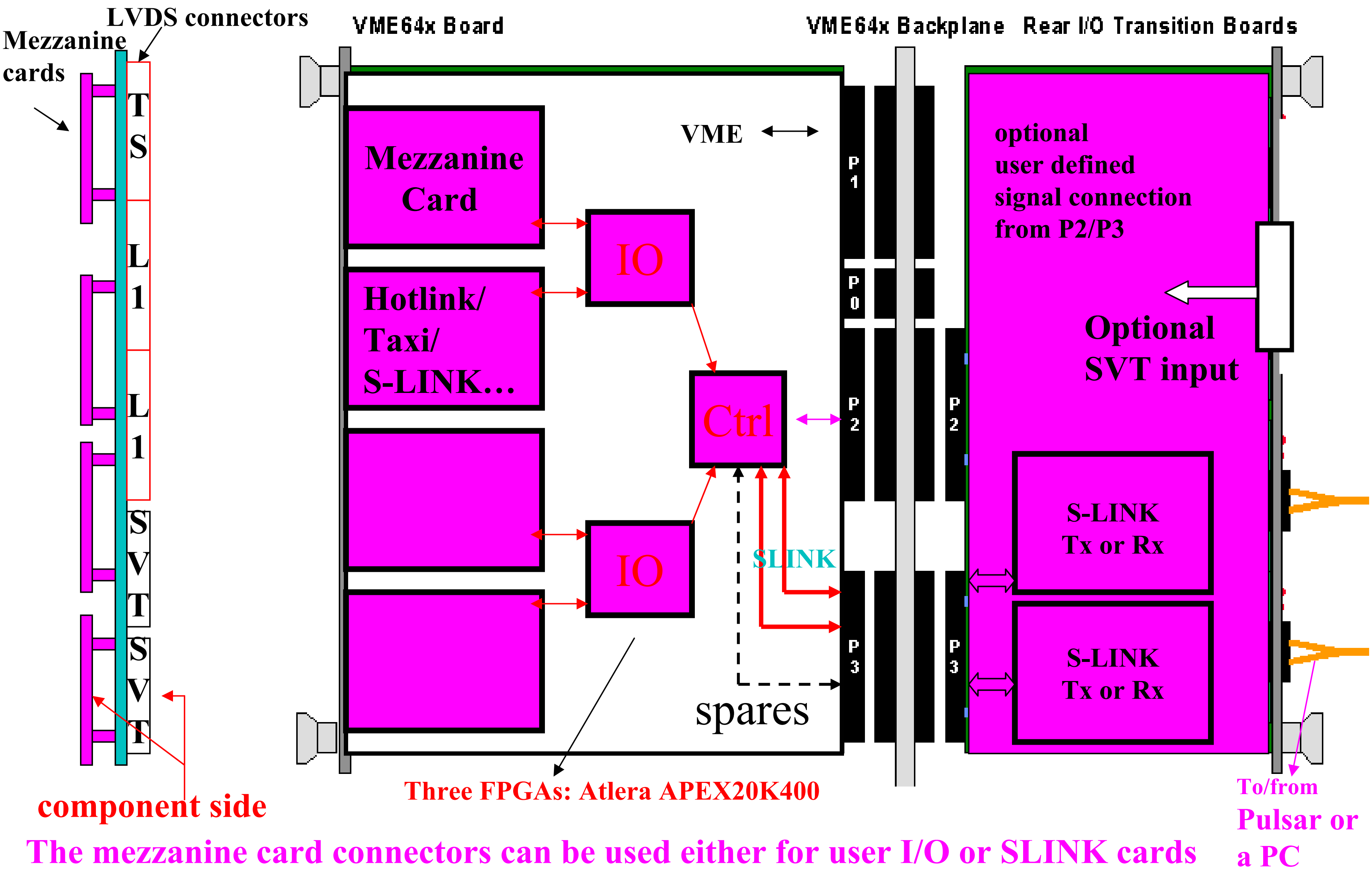
Level 2 Replacement

- DEC Alphas not feasible to maintain long term
  - no longer produced/supported…..DEC no longer exists
  - CDF internal review committee recommends replacing Alphas for Run IIb
- Concerns about long term operation & maintenance of large number of diverse interface boards
- **Replace existing L2 system with a Pulsar system**
  - interface board now common to every system
  - incorporates test/debug into interface board
  - data transfer uses S-link technology developed for LHC and supported at CERN
  - standard S-link ⌦ PCI allows simple, high speed interface with commercial PC as L2 processor

PULSAR design

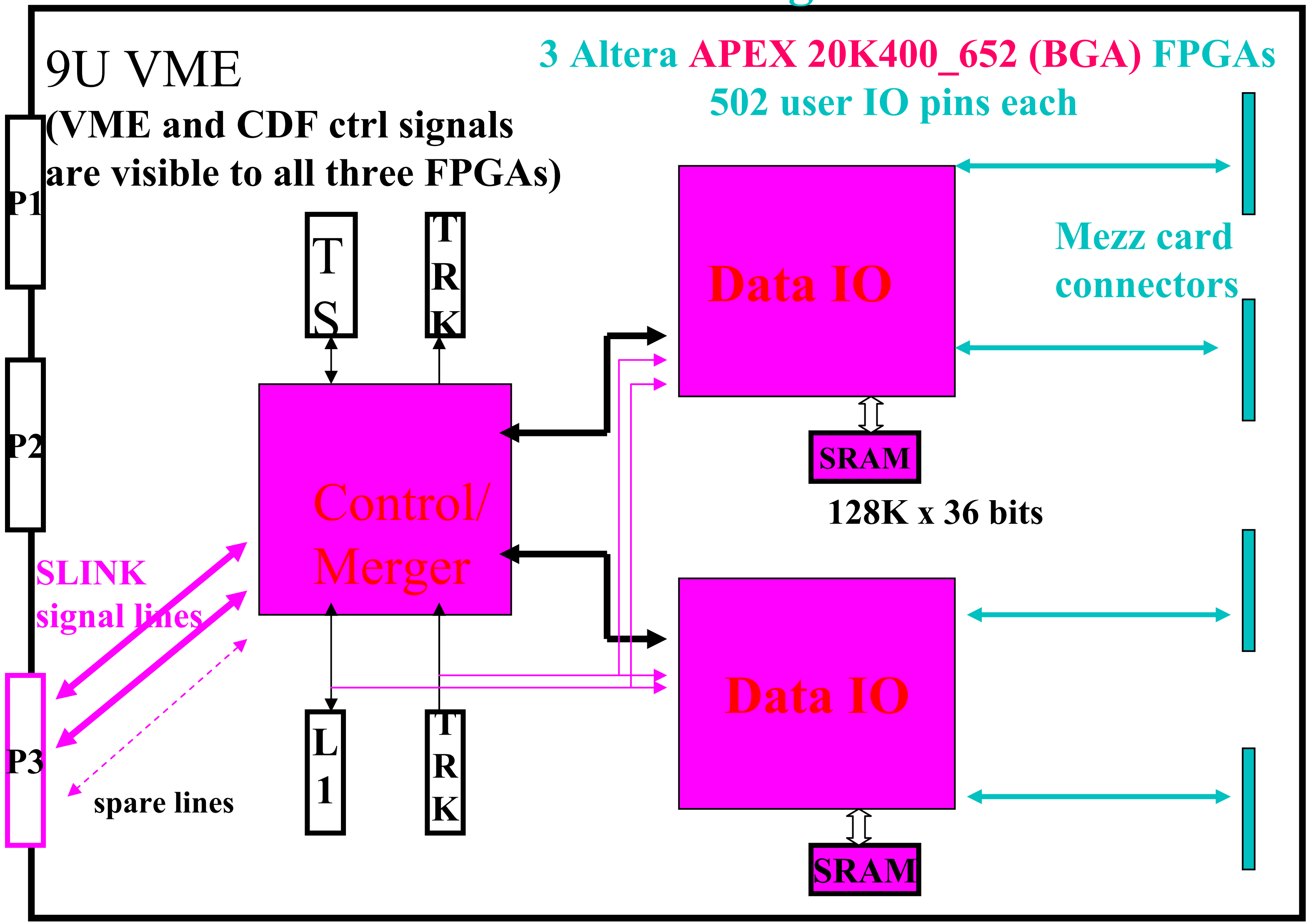
Front-panel (double width)

Each mezzanine card can have up to 4 (hotlink/Taxi) fiber channels



The mezzanine card connectors can be used either for user I/O or SLINK cards

Pulsar design



3 APEX20K400 FPGAs on board = 3 Million system gates/80KB RAM per board

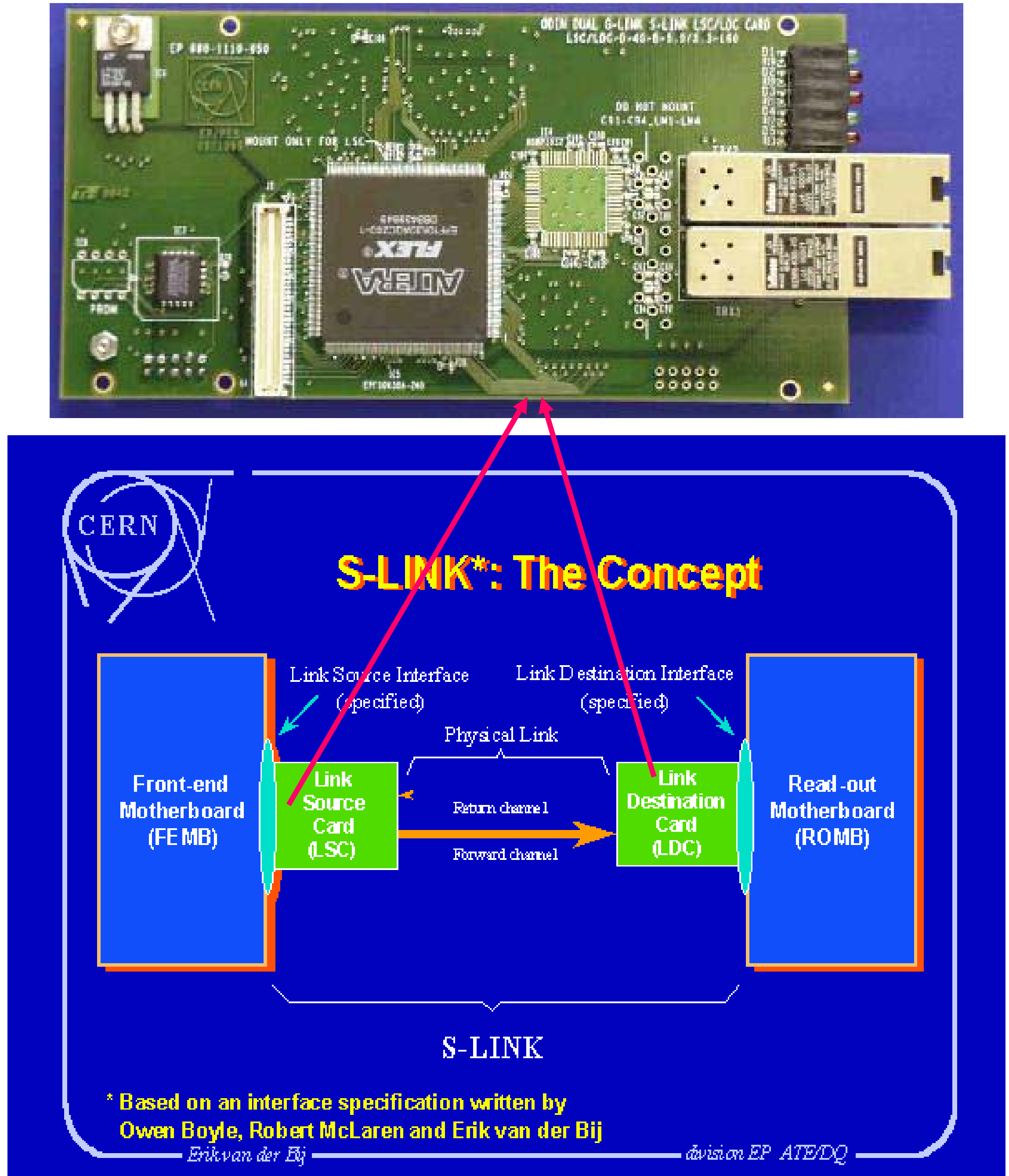
2 128K x 36 pipelined SRAMs with No Bus Latency: 1 MB SRAM (~5ns access time)

SLINK format example:

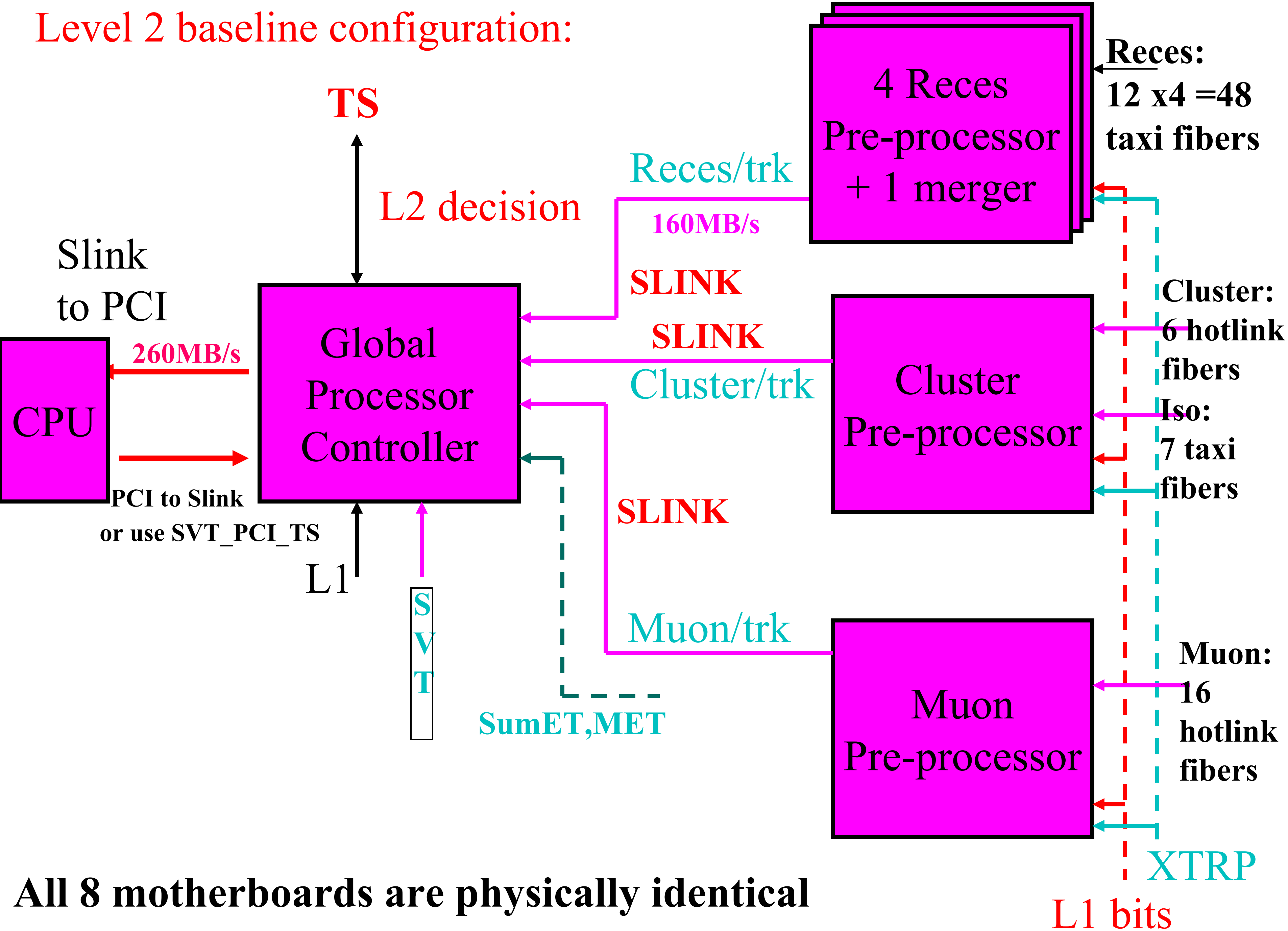
ATLAS SLINK data format

Beginning of Block control word
Start of Header Marker
Header Size
Format Version No.
Source Identifier
Level 1 ID
Bunch Crossing ID
Level 1 Trigger Type
Detector Event Type
Data or Status elements
Status or Data elements
Number of status elements
Number of data elements
Data/Status First Flag
End of Block control word

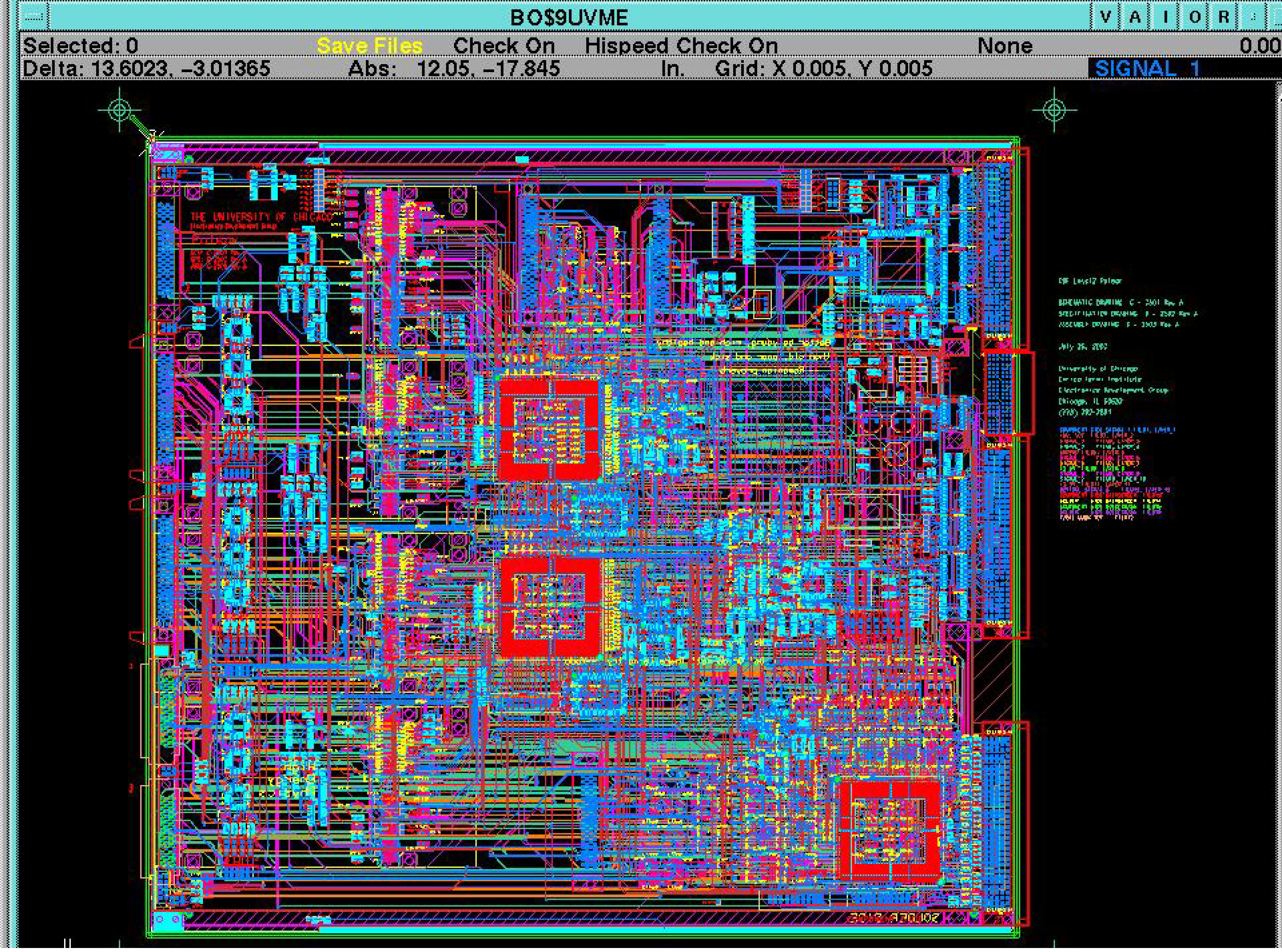
SLINK interface mezzanine card



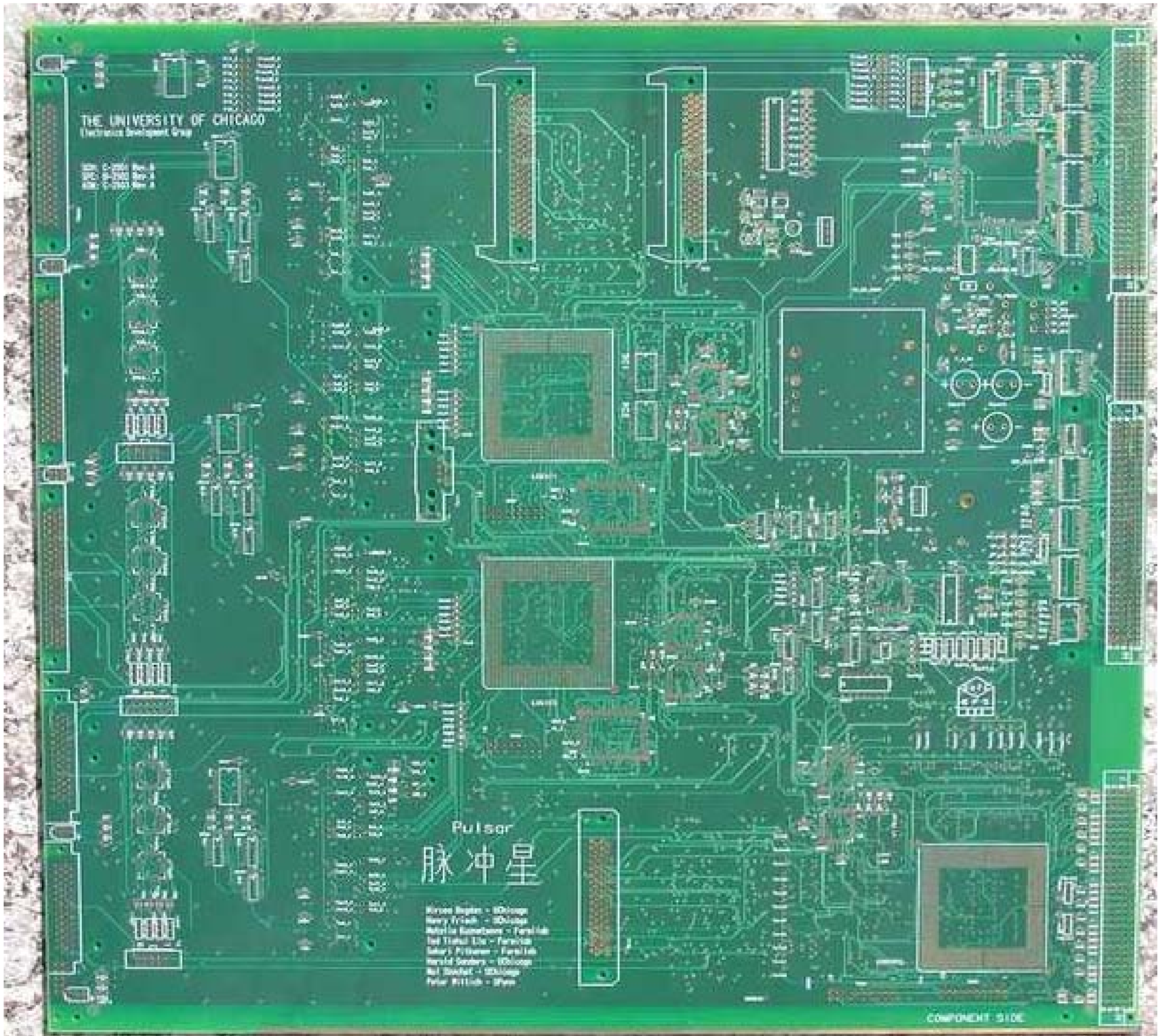
Level 2 baseline configuration:



All 8 motherboards are physically identical


BO$9UVME
V A I O R
Selected: 0
Save Files
Check On
Hispeed Check On
None
0.00
Delta: 13.6023, -3.01365
Abs: 12.05, -17.845
In.
Grid: X 0.005, Y 0.005
SIGNAL 1
THE UNIVERSITY OF CHICAGO

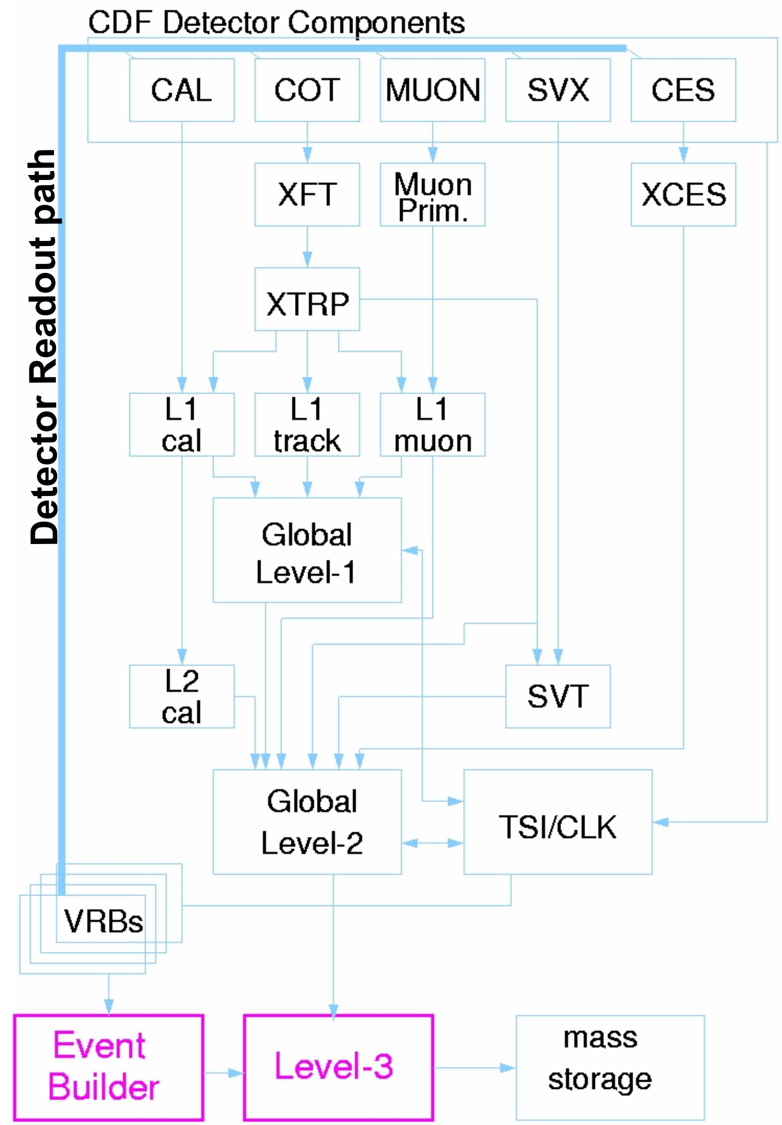
Prototype Pulsar Board



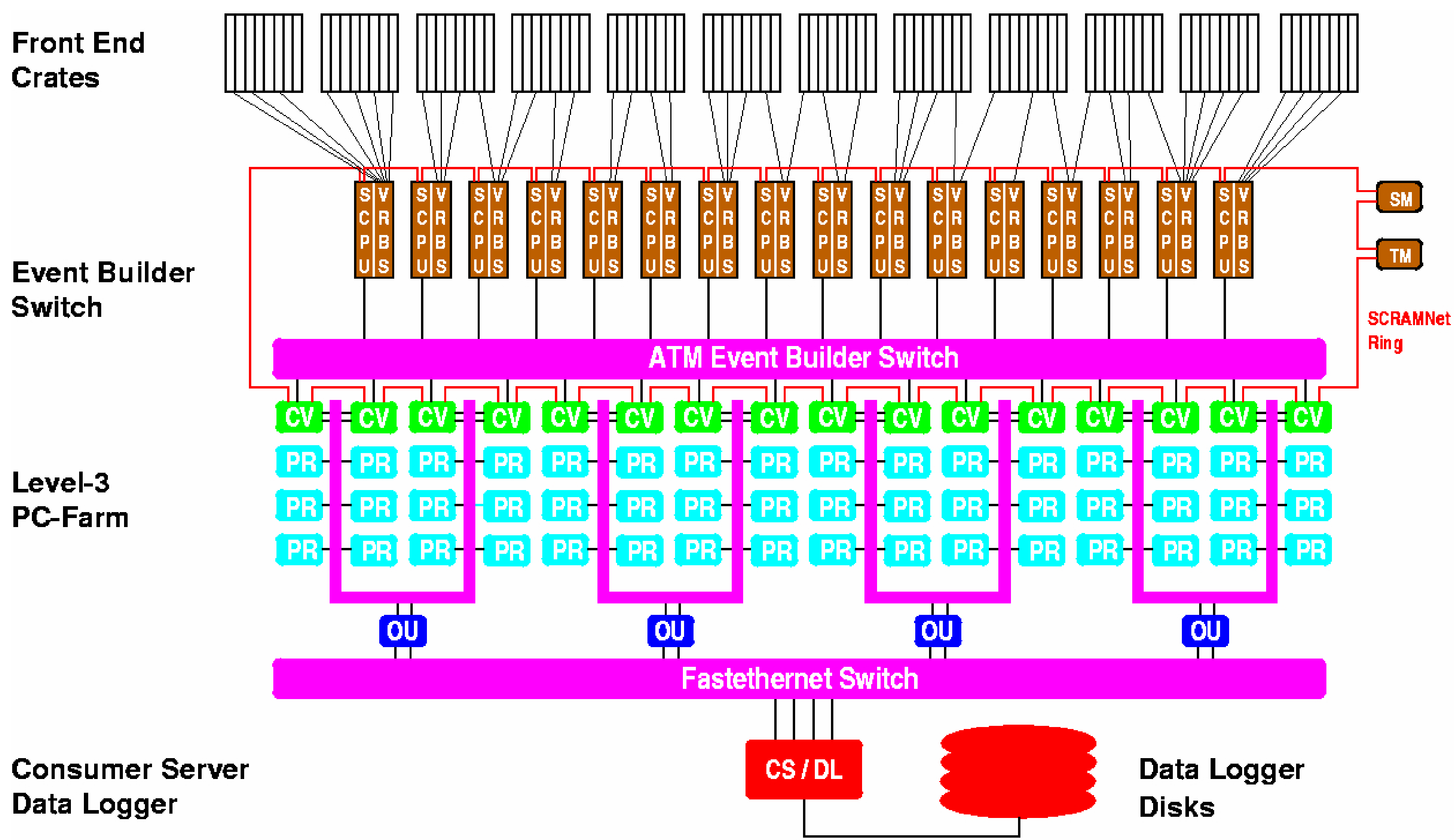
Event Builder/L3 Upgrade

Full detector readout occurs on Level 2 trigger accept

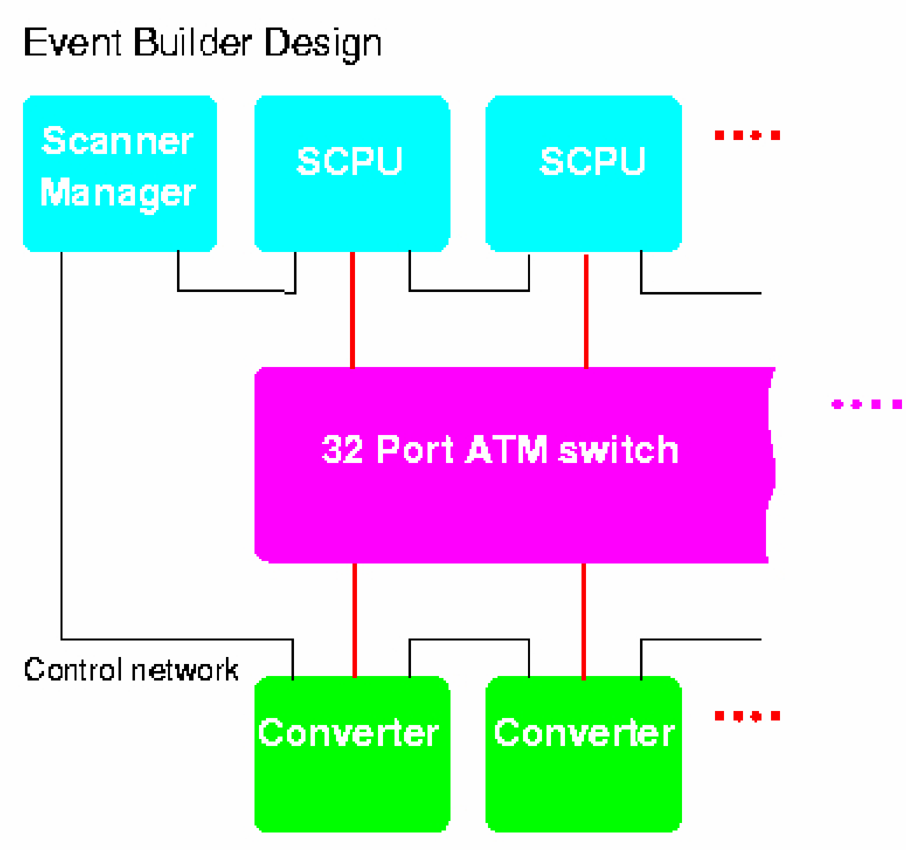
- Event Builder
  - subsystems send data to VRBs
  - Event builder accepts data from VRBs, assembles the full event
- Level 3 Trigger
  - event sent: EVB→L3 PC farm
  - single PC node per event runs reconstruction & trigger algorithms
  - greater rejection at L3 needed in Run IIb

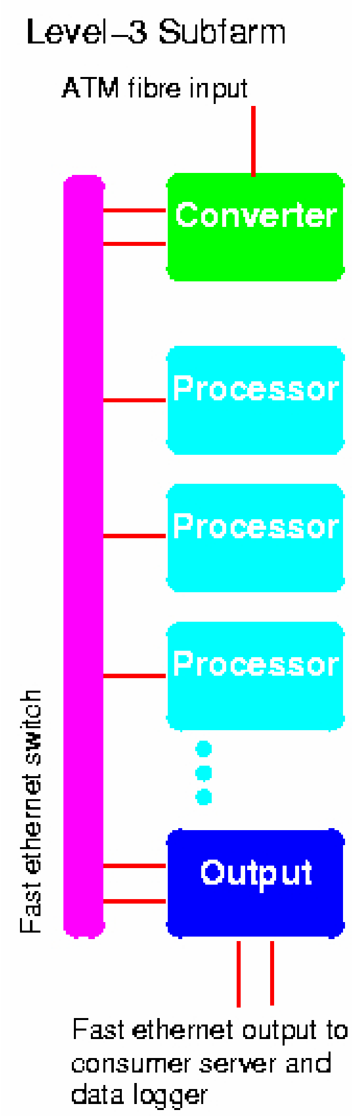


Readout/L3 Architecture



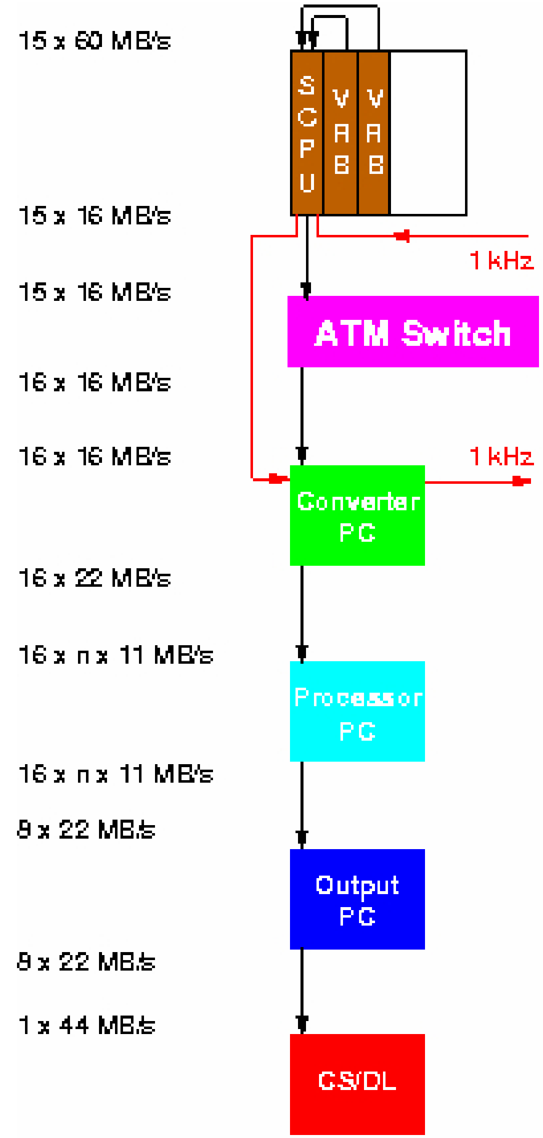
Readout/L3 Architecture





ATM Upgrade

- Based upon Run IIb trigger table and data volume, extrapolate to ~400MB/s through ATM switch
  - current system ~240MB/s peak
- Upgrade system from ASX1000 ATM → ASX4000 ATM (bigger, newer, faster) going to OC12 ATM links
  - anticipate ~500MB/s or better



Level 3 PC Farm Upgrade

- More Level 3 PC processing power is required for Run IIb
  - reconstruction takes longer
    - higher occupancy
  - trigger algorithms more elaborate
    - greater rejection required

sample	Mean CPU time (seconds)†
t-tbar + 0 minimum bias	0.82 ± 0.03
t-tbar + 5 minimum bias	2.66 ± 0.10
t-tbar + 10 minimum bias	5.93 ± 0.19
t-tbar + 15 minimum bias	8.32 ± 0.67

† CPU time to run COT tracking on offline analysis computer (fcdfsgi2). Tracking code not optimized for higher luminosity conditions.

- Purchase processors at constant rate over 3 years of project
- Expect processor improvements will keep up with our growth in L3 needs throughout Run IIb
  - increased complexity of events offset by improved processing power

Trigger/DAQ Management

1.3 CDF Trigger/DAQ
Kevin Pitts

- **1.3.1 TDC Project**
  Henry Frisch, Ting Miao
- **1.3.2 Level 2 Trigger**
  Ted Liu, Peter Wittich
- **1.3.3 XFT II Project**
  Richard Hughes, Brian Winer
- **1.3.4/1.3.5 L3 farm/Event Builder**
  Christoph Paus
- **1.3.6 Silicon Vertex Trigger**
  Bill Ashmanskas, Luciano Ristori

CDF Trigger/DAQ Manpower

- TDC
  - Chicago (ENG+TECH), Fermilab(ENG+PHYS+TECH), Duke(PHYS)
- XFT
  - Ohio State(ENG+PHYS+TECH), Illinois (ENG+PHYS+TECH), Florida (ENG+PHYS+TECH)
- Level 2
  - Fermilab(PHYS+TECH), Chicago(ENG+TECH), Penn(ENG+PHYS+TECH), Argonne(ENG+PHYS+TECH)
- SVT
  - Pisa(ENG+PHYS+TECH), Chicago(ENG+PHYS+TECH)
- EVB/L3
  - MIT(PHYS), Fermilab(ENG)

Trigger/DAQ Costs

Total escalated Base cost (including R&D component):

Fiscal Year		2002	2003	2004	2005	2006	Totals
(AY $)	Total Base	$ 43,121	$ 1,078,463	$ 2,471,767	$ 1,509,360	$ -	$ 5,102,712
	R&D	$ 36,616	$ 567,722	$ 126,627	$ -	$ -	$ 730,965

Total Contingency – 2,802 K$ (AY)

Total Cost + Cont. – 7,904 K$ (AY)

M&S overhead 0.177

Labor overhead 0.286

includes G&A

Cost by Subproject

Costs listed in AY dollars:

WBS	Task Name	Cost (AY$)	Cont.(AY$)	Cont. (%)	Total (AY$)
1.3.1	Run 2b TDC Project	$1,481,527	$1,147,685	77%	$2,629,212
1.3.2	Run 2b Level 2 Project	$350,070	$111,000	32%	$461,070
1.3.3	Run 2b XFTII Project	$1,885,814	$893,994	47%	$2,779,808
1.3.4	Event-Builder Upgrade	$602,093	$202,333	34%	$804,426
1.3.5	Computers for L3 PC Farm	$494,746	$253,558	51%	$748,304
1.3.6	SVT Upgrade	$288,462	$193,126	67%	$481,588
1.3.	*Run 2b DAQ & Trigger*	$5,102,712	$2,801,696	55%	$7,904,408

Comments:

- Non-Fermilab labor included in M&S
- most of XFT labor is in the form of in-kind contributions from Ohio State, Illinois and Florida

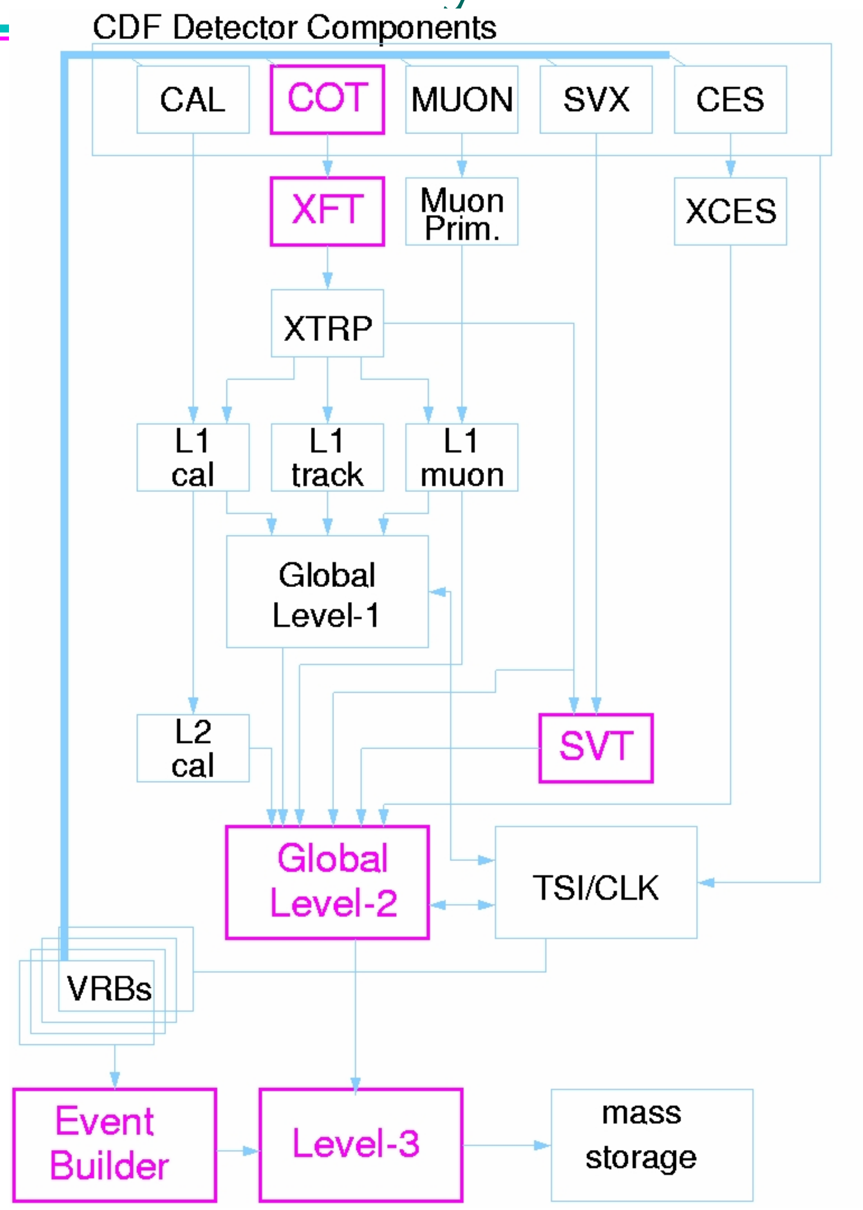
DAQ/Trigger Project Schedule

- All components completed before silicon
- Preproduction complete, production well along (or complete) before shutdown for Run IIb
  - commissioning in full CDF system with beam
- Completion dates:

TDC	4/19/05
XFT	3/7/05
SVT	7/20/04
Level 2	11/10/04
EVB/L3	2/24/05

DAQ/Trigger Summary

- These are the pieces of the CDF Front-end, Trigger and Data Acquisition system we need to upgrade/update to carry out a high p_T physics program
  - TDC replacement
  - XFT upgrade
  - SVT upgrade
  - L2 replacement
  - Event builder/L3 upgrade
- The remainder of the Run Iia CDF front-end/trigger/DAQ system will perform well throughout Run IIb



Supporting Documentation

- CDF Run IIb Technical Design Report
- "Report from the Run IIb Committee"
  - appendices: "Trigger Rates", "XFT", "Event Builder", "TDC"
- CDF 6065: "COT Data Volume & Implications for Readout in Run IIb"
- CDF 5824: "A First Look at the Performance of the CDF Data Acquisition System"
- "Report from the TDC Review Committee"
- "CDF Run IIb TDC Specifications"
- CDF 5986: "Performance Study of the eXtremely Fast Tracker at High Luminosity"
- PULSAR Web page (documentation, schematics, BOM): http://hep.uchicago.edu/~thliu/projects/Pulsar
- CDF 6059: "XFT Upgrade for Run IIb"
- CDF 6032: "Mezzanine Card Design Specifications for the PULSAR Board"
- "Report from the Level 2 Review Committee"