Progress On Conversion of SVX3 Chip To Quarter Micron Technology

- Conversion Method
- Done So Far
- Preamp Simulation Results
- What's Next?

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Conversion Method

- Conversion Method Proposed by O. Milgrome of LBNL IC Design Group. Relies heavily on simulation.
- Conversion Steps (for each circuit block):

  1. Simulate circuit extracted from Honeywell 0.8μm layout to verify that it works approximately with transistor models from a quarter micron process (TSMC)
     (The extracted circuit is a black box, hard to modify)

  2. Enter Circuit Schematic into Cadence and simulate to check that it behaves as the extracted circuit.

  3. Modify schematic as needed to improve performance. Check with simulation.

  4. Draw quarter micron cells from schematic. (In principle can use CERN standard libraries for digital circuits, which automates the layout generation)

  5. Extract circuit from quarter micron mask and simulate to verify that it is correct.

- Conversion End Product:

  – A 0.25μm Layout For A New Chip, "SVX3E".

  – New Specifications For SVX3E, **DIFFERENT** From SVX3D!

  – Physicist involvement in simulations is essential to make sure that new specifications are adequately meet physics needs.

Done So Far

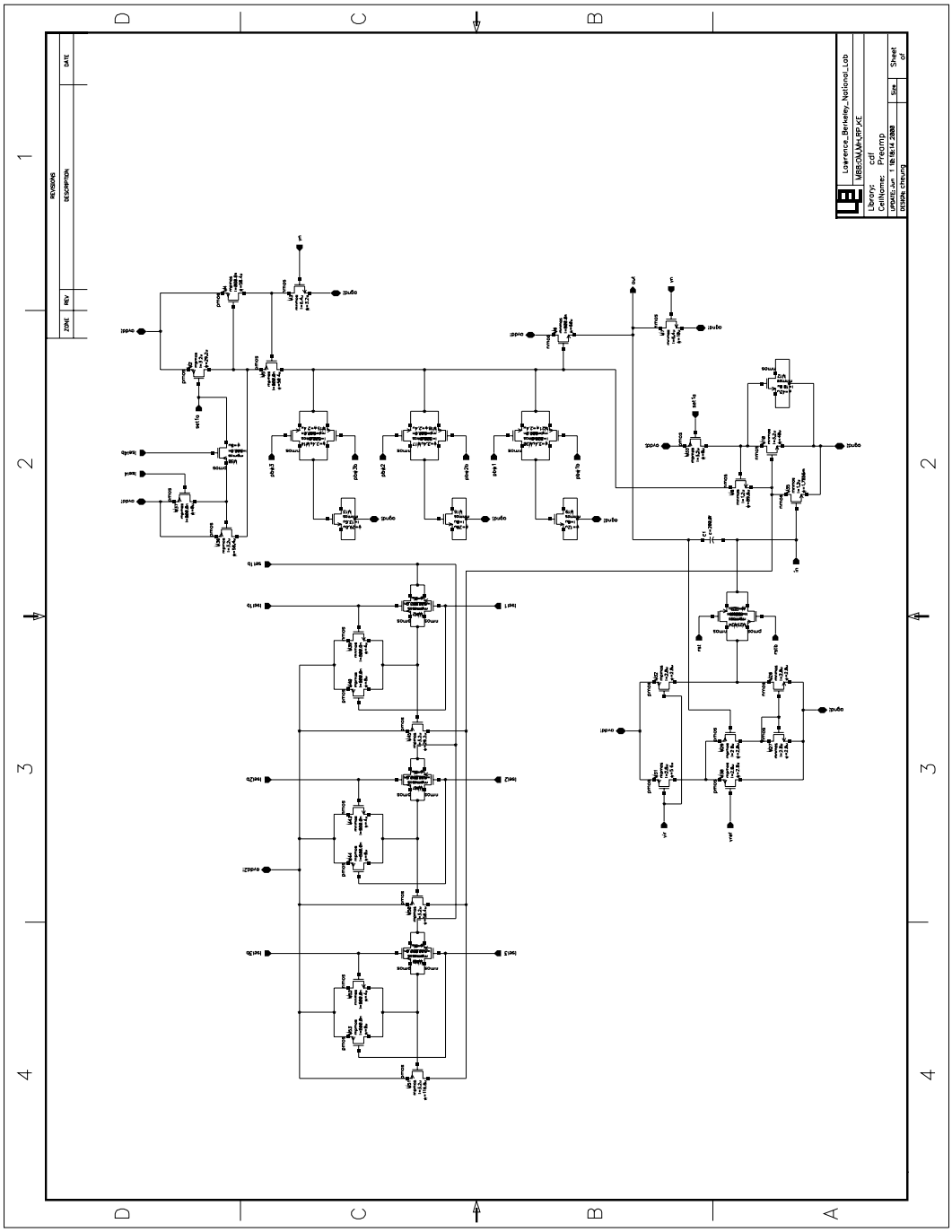
- Aaron and Jay up to speed on Spice simulations, Hillary (full time engineering student) up to speed on Cadence.

- Preamp extracted from Honeywell layout and simulated using Honeywell H-Spice model. Very good agreement with real chip data (better than previously available simulations)

- Extracted preamp simulated with TSMC quarter micron models. Behavior was reasonable.

- Preamp schematics entered into Cadence. Pipeline analog section has also been entered already.

- **Simulation of Preamp from Cadence schematic shows reasonable performance.**


Lawrence_Berkeley_National_Lab
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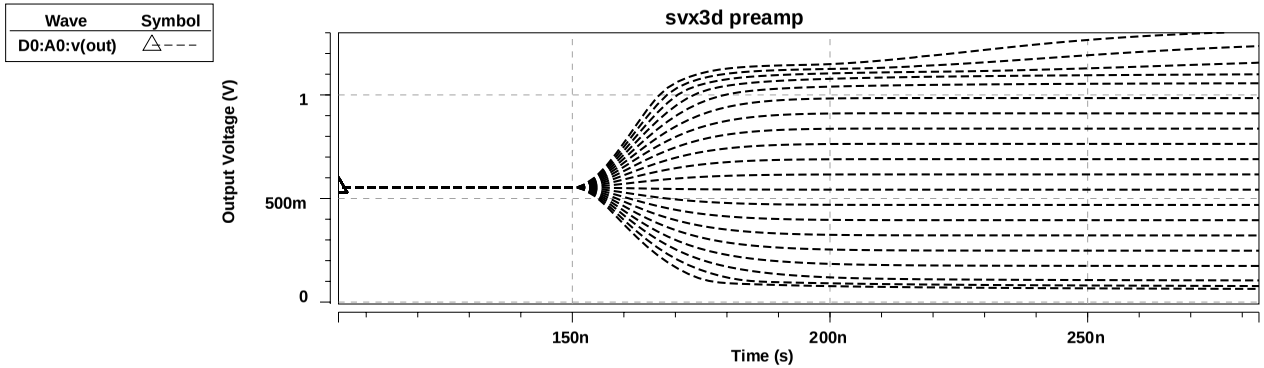
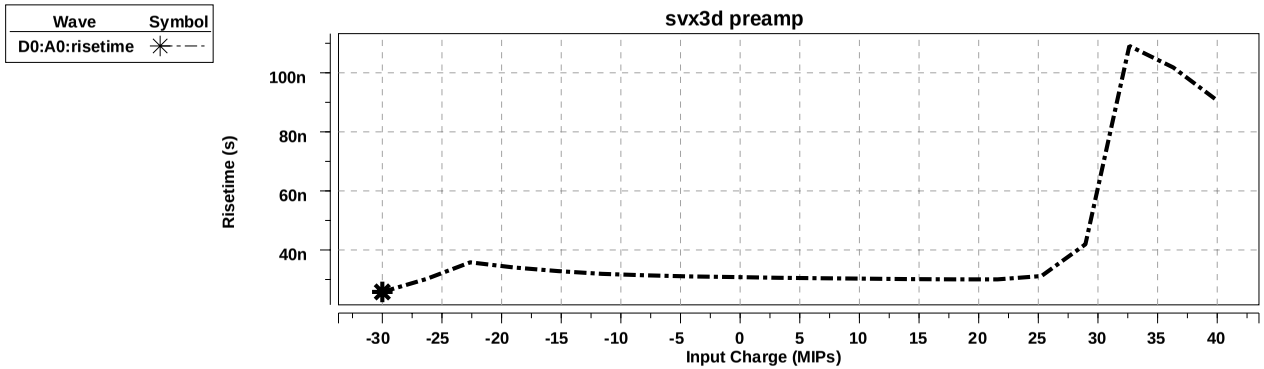
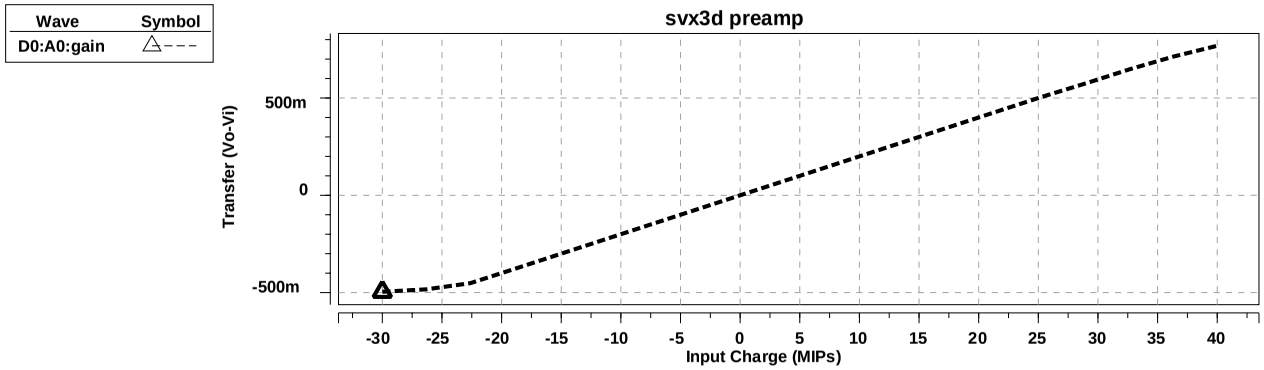
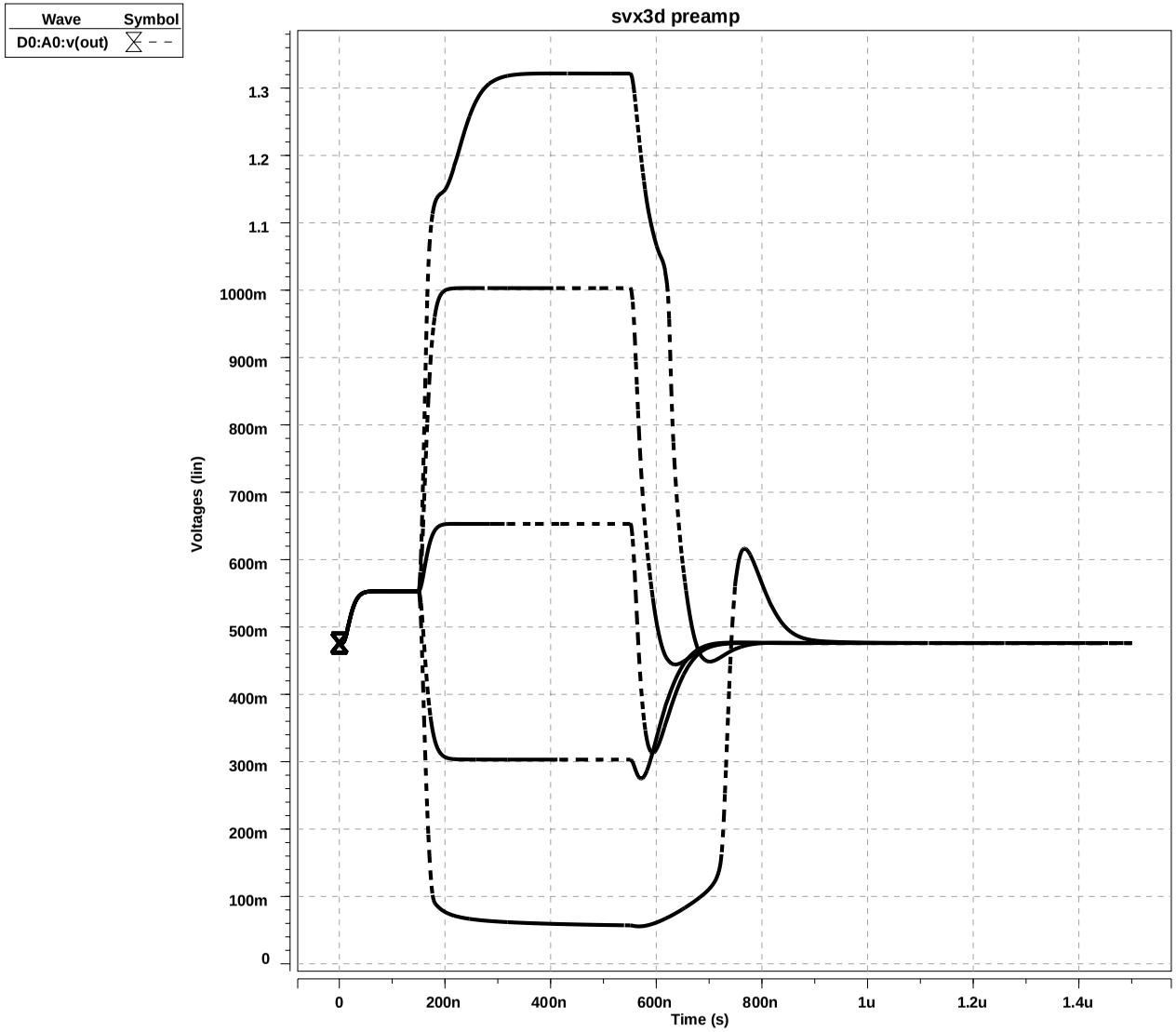
Preamp Simulation Results

	SVX3D Honeywell ($0.8\mu m$)	This Study (sim. $0.25\mu m$)
Supply Voltage	+5V	+2.5V
Input Transistor Current	190μA	279μA
Power	950μW	700μW
0-90% Risetime, 30pF Load BW bits = 0	65ns	30ns
Noise 30pF Load, 65ns Risetime		
Dynamic Range	110 MIPs	45 MIPs
Reset Time	500ns	<500ns


svx3d preamp
Wave
Symbol
D0:A0:v(out)
Output Voltage (V)
1
500m
0
150n
200n
250n
Time (s)


svx3d preamp
Wave
Symbol
D0:A0:risetime
Risetime (s)
100n
80n
60n
40n
-30
-25
-20
-15
-10
-5
0
5
10
15
20
25
30
35
40
Input Charge (MIPs)


svx3d preamp
Wave
Symbol
D0:A0:gain
Transfer (Vo-Vi)
500m
0
-500m
-30
-25
-20
-15
-10
-5
0
5
10
15
20
25
30
35
40
Input Charge (MIPs)


svx3d preamp
Wave
Symbol
D0:A0:v(out)
Voltages (lin)
1.3
1.2
1.1
1000m
900m
800m
700m
600m
500m
400m
300m
200m
100m
0
0
200n
400n
600n
800n
1u
1.2u
1.4u
Time (s)

What's Next?

- Tweak preamp schematic to further enhance/optimize performance (Oren)
- Simulate modified preamp circuits. Select the best (Aaron, Jay, Bob)
- Draw preamp cell from schematic (Hillary)
- Simulate pipeline analog section (Aaron, Jay, Bob)
- Extract full pipeline including logic and verify that it works approximately (Oren, AJB)
- Enter pipeline logic schematic into Cadence (Hillary)
- Simulate channel number & data FIFOs (already extracted) to verify they work approximately (AJB)
- Continue like this for every circuit
- Goal to have conclusion by September 2000.

Some possible tweaks

- *Trivial mods*
  - Increase C_f $\Rightarrow$ more dynamic range, less gain. Can compensate gain with writeamp.
  - Change size of input transistor $\Rightarrow$ need to watch intrinsic noise
- *Less Trivial mods*
  - Modify cascode configuration
  - Modify "load" configuration
  - Continuous reset