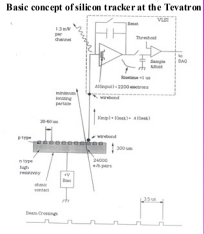
SVX: The CDF Silicon Vertex Detector

Hardware Development for the First Precision Silicon Tracker at a Hadron Collider

Basic concept of silicon tracker at the Tevatron



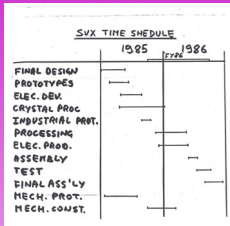


Figure A: 1985 Schedule for SVX Construction

History

- The original CDF proposal was dated 1981 (D. Ayres et al)
  - Already at that time the Pisa group, most notably Aldo Menzione, discussed the addition of silicon tracking (SVX) to the vertex region
- 1984 Sherwood Parker, Terry Walker, and Bernard Hyams published a description of *Microplex*, the 1st NMOS ASIC designed to read silicon strips
- Spring 1985 A workshop was held at Fermilab to discuss the SVX upgrade in the context of these new developments, 1st schedule presented (Figure A), Godparent committee was formed including:
  - Willy Chinowsky, Brig Williams, Masa Mishina, Henry Frisch, Alan Clark
- Technical and other challenges were perceived
  - SVX strips were long (Figure B) Microplex S/N might be insufficient
  - Channel count (~50K) was high – what to do with cables?
  - Bad experience at UA1 with a wire chamber vertex detector
  - Could the device do any physics?
  - Could precision be achieved and maintained?
- The overall zeitgeist was negative for the SVX but this was partially offset by the fact that most of the LEP detectors were installing silicon tracking But "….these were not at a hadron collider!!!…"
- October 1985 A workshop was held in Berkeley – "New Solid State Devices High Energy Physics" in conjunction with the IEEE NSS and a meeting on the CDF SVX project.
  - Stuart Kleinfelder discusses the application of CMOS to SVX, offering a potential gain in S/N – a plan is made to develop a CMOS ASIC for CDF
- April 1986 Kleinfelder proposes a CMOS ASIC "the SVX chip" (Figure C) including:
  - Improved S/N for long strips
  - Sparse readout – only hit channels would be read: reduced cable plant!
  - Neighbor logic – read neighbors of hit channels
  - Low power
- Summer 1986 First prototype SVX chip is on the test bench (Figure D)
- 1987 Bench + beam tests demonstrate good performance for SVX (Figure E)
  - Prototype ladders are constructed using hybrids, SVX chips, Micron detectors
  - A custom DAQ system is designed and built (SRS+SDA)
  - Prototype Beryllium bulkheads are designed and prototyped
  - Assembly procedures are developed and tested

At this point the project properly organized and a proposal was written to FNAL

- 1988 Proposal P-775 is written and approved by the PAC (Figure F)
- 1989 Fermilab assumes project management, Dan Amidei (later Paul Tipton) becomes leader with,
  - Fabrizio Raffaelli – mechanical engineering
  - Slawek Tkacyk + P.I.G. – DAQ
  - Mike Hyrczk and John Skarha– mechanical construction
  - Carl Haber – front end electronics
  - Aldo Menzione – detectors
- 1989 Production order for 174" wafers of SVX chips is placed with Hewlett Packard in 3 micron rad-soft CMOS
  - Radiation studies on the CDF beam pipe (Figure G)
- 1990 Second beam test (Figure H)
- 1990 Project is in production (Figure I)
  - Detector testing
  - Wafer probing
  - Hybrid fabrication and assembly (Figure J)
  - Beryllium bulkheads and cooling pipes (Figure K)
  - DAQ modules
  - Ladder assembly and test
  - Cooling and monitoring system
  - HV and LV control
  - Radiation exposure monitoring and control
- 1991 Barrel assembly and test begins and ends, Paul Tipton becomes project leader (Figure L,M), SVX* is organized, J. Incandela is project leader
- December 1991 1st attempt to insert SVX into CDF (Figure N)
- Winter 1992 SVX is installed into CDF and under test
- May 12, 1992 1st collisions of Run1A – SVX works! (Figure O)
- 1992 – 1993 Major construction and test effort for SVX*
- May 1993 SVX-Prime is installed and in operation as well!

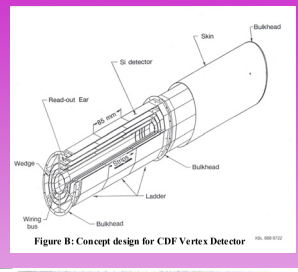


Figure B: Concept design for CDF Vertex Detector

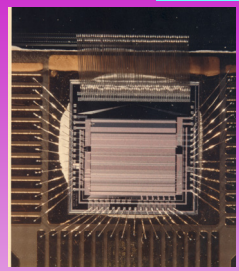


Figure D: 1st prototype SVX chip under test with silicon

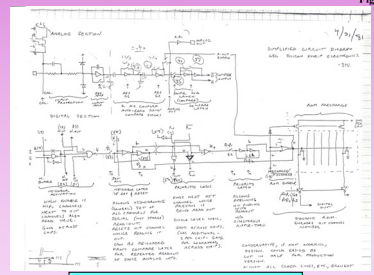


Figure C: 1986 first hand sketch of SVX Chip design

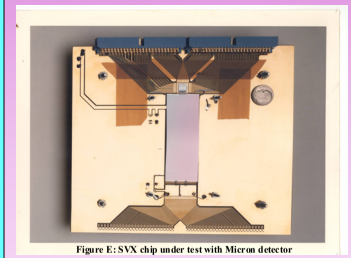


Figure E: SVX chip under test with Micron detector

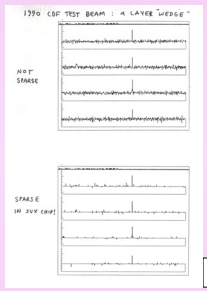
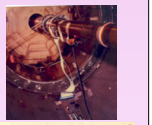


Figure H: beam test demonstrates sparse readout



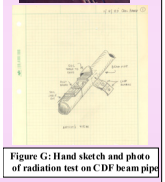


Figure G: Hand sketch and photo of radiation test on CDF beam pipe

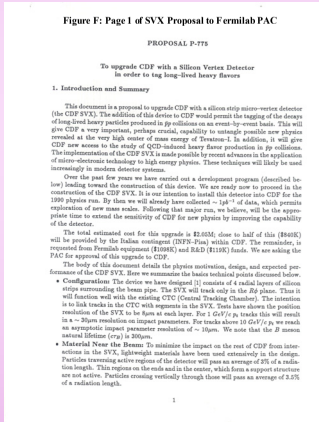


Figure F: Page 1 of SVX Proposal to Fermilab PAC

PROPOSAL P-775

To upgrade CDF with a Silicon Vertex Detector in order to tag long-lived heavy flavors

1. Introduction and Summary

This document is a proposal to upgrade CDF with a silicon strip micro-vertex detector (the CDF SVX). The addition of this device to CDF would permit the tagging of the decays of long-lived heavy particles produced in $p\bar{p}$ collisions on an event-by-event basis. This will give CDF a very important, perhaps crucial, capability to untangle possible new physics revealed at the very high center of mass energy of Tevatron-I. In addition, it will give CDF new access to the study of QCD-induced heavy flavor production in $p\bar{p}$ collisions. The implementation of the CDF SVX is made possible by recent advances in the application of micro-electronic technology to high energy physics. These techniques will likely be used increasingly in modern detector systems.

Over the past few years we have carried out a development program (described below) leading toward the construction of this device. We are ready now to proceed in the construction of the CDF SVX. It is our intention to install this detector into CDF for the 1990 physics run. By then we will already have collected ~ $1pb^{-1}$ of data, which permits exploration of new mass scales. Following that major run, we believe, will be the appropriate time to extend the sensitivity of CDF for new physics by improving the capability of the detector.

The total estimated cost for this upgrade is $2.6M; close to half of this ($840K) will be provided by the Italian contingent (INFN-Pisa) within CDF. The remainder, is requested from Fermilab equipment ($1088K) and R&D ($110K) funds. We are asking the PAC for approval of this upgrade to CDF.

The body of this document details the physics motivation, design, and expected performance of the CDF SVX. Here we summarize the basics technical points discussed below.

- **Configuration:** The device we have designed [1] consists of 4 radial layers of silicon strips surrounding the beam pipe. The SVX will track only in the $R\phi$ plane. Thus it will function well with the existing CTC (Central Tracking Chamber). The intention is to link tracks in the CTC with segments in the SVX. Tests have shown the position resolution of the SVX to be $8\mu m$ at each layer. For 1 GeV/c p_t tracks this will result in a ~ $30\mu m$ resolution on impact parameters. For tracks above 10 GeV/c p_t we reach an asymptotic impact parameter resolution of ~ $10\mu m$. We note that the B meson natural lifetime ($c\tau p$) is $200\mu m$.
- **Material Near the Beam:** To minimize the impact on the rest of CDF from interactions in the SVX, lightweight materials have been used extensively in the design. Particles traversing active regions of the detector will pass an average of 3% of a radiation length. This reliance on the ends and in the center, which form a support structure are not active. Particles crossing vertically through those will pass an average of 2.5% of a radiation length.

1

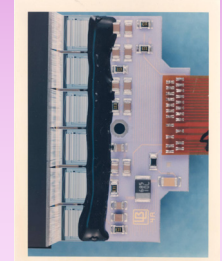


Figure J: Layer 4 hybrid with 768 wirebonds

Figure K: Beryllium bulkhead with cooling lines in place

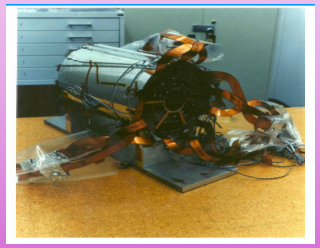


Figure M: one of two completed SVX barrels

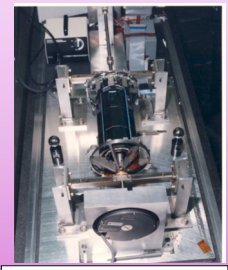


Figure L: Ladders are being loaded into barrels

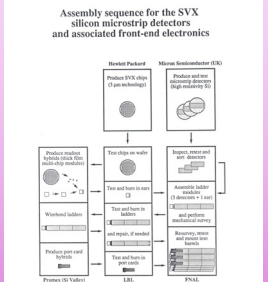


Figure I: production plan for electronics and ladder assembly

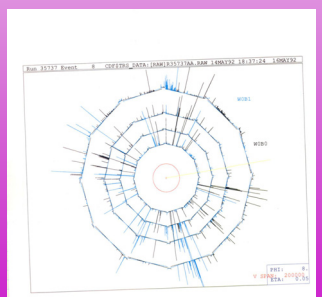


Figure O: Early Run1a event seen at CDF (after 4 days of running)

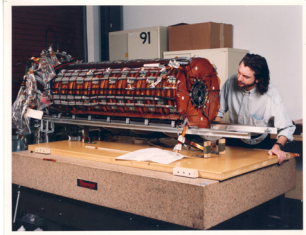
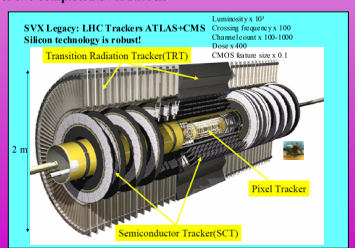


Figure N: Nicola Bacchetta (New Mexico, now Padova) looks at his 1st baby.



SVX+SVX* Author List

Special credit to Alvin Tollestrup who was an early supporter and advocate of the SVX project

D. Amidei: 1st SVX Project Leader
P. Azzi: testing and analysis
N. Bacchetta: testing, DAQ, commissioning, ops
Mark W. Bailey: DAQ
B.A. Barnett: J HU lead
Franco Bedeschi: simulation, algorithms
D. Bisello: Padova lead
V. Bolognesi: testing
C. Brown II: radiation, testing, mechanics
G. Busetto: software
J.D. Cammenga: testing
W.C. Carithers: LBNL co-lead
H. Carter: mechanical engineering
A.Castro: software, simulation
H.Y. Chao: mechanical
G.Chiarelli: simulation, detector studies
C.N. Chiou: mechanical
S. Cihangir: S idet, assembly
S. Dell'Agnello: software, display
P.F. Derwent: radiation monitoring, protection
R. Dincar
A. Dunn: testing
R.Ely: testing, design
E. Engels Pitt co-lead
B. Flaugher: mechanics, installation
A.Fraescheti: testing
A. Barbaro-Galtieri: LBNL co-lead
A.F. Garfinkel: Purdue lead
G. Gillespie: mechanics
D.Glenzinski: detector tests
H. Gonzalez: assembly, hands-of-gold
S. Gonzalez: assembly
C.Grimm: mechanical design
M.Gureau: assembly
C. Haber: front end electronics
T. Hawke: wirebonding
S. Holland: detector studies
M. Hrycyk: assembly Wizard
D. Hurnup: accelerator, rad protection
R. Hughes: DAQ
J. Incandela: SVX* project leader
E. Kajfasz: testing
R. Kleen
S. Kleinfelder: SVX chip design
M.Kruse: DAQ
M. Loreti: software
B. Lundberg: SiDet
F.Mando: testing
M. Mariotti: testing, DAQ, cooling pipes
J.A.J. Matthews: New Mexico lead
A. Menzione: original design and concept, detectors
T. Meisrick: electronics testing
C. Nelson: DAQ, digitizer
A.Paccagnella: detector development
L. Pescara: software
N.Pruiaella: software
N. Produit: testing
G. Punzi: DAQ, R&D testing, software
F. Raffaelli: lead mechanical engineer
P. Ratzmann: mechanical engineering
L. Ristori: DAQ
O. Schneider: ladder testing, calibration, s/w
P.G. Sciacca: testing
L.Scott
S. Segler: PIG lead
M. Shapiro: alignment
N.M. Shaw: detector tests, calibration, s/w
T .Shaw: DAQ design
P.Shepard: Pitt co-lead
P Singh: radiation damage, detector testing
J. Skarha: mechanical assembly
F.D. Snider: mechanicals, power supplies, cables
T.Y. Song: testing
J. Spalding: SiDet
A. Spies: testing, cables
D. Stuart: testing, DAQ, commissioning, ops
P. Tipton: 2nd SVX project leader, cooling
S. Tkacyk: DAQ lead
F. Tartarelli: testing
K. Tollefson: cooling, installation
D.Tousignant: mechanical drafting
J. Tseng: testing
N. Turini: DAQ, testing, commissioning
K. Turner: DAQ SEQ design
S. Vejcik II: assembly, radiation
G. Watts: cooling, monitoring
T.R. Wesson
W.C. Wester III: K testing, port card
H. Wenzel: alignment, analysis
C.H.Wang: mechanics
M.J.Wang: mechanics
M. Wong: chip testing
S.C.Wu: Taiwan lead
W. Yao: HV tests, analysis
R.Yarema: electrical engineering
J.C. Yun: mechanical assembly
F. Zetti: assembly and tests, old-world craftsman

Vendors

Micron Semiconductor: detectors
Promex: wirebonding, hybrids, assembly
Hughes Interconnect: flex cables
Lonthor Engineering: flex cables
Hardix: Be machining
Electrofusion: Be beam pipe
Forro EMD: thick film materials
Hewlett Packard: CMOS fabrication
Stellar Industries: ceramics

Carl Haber

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