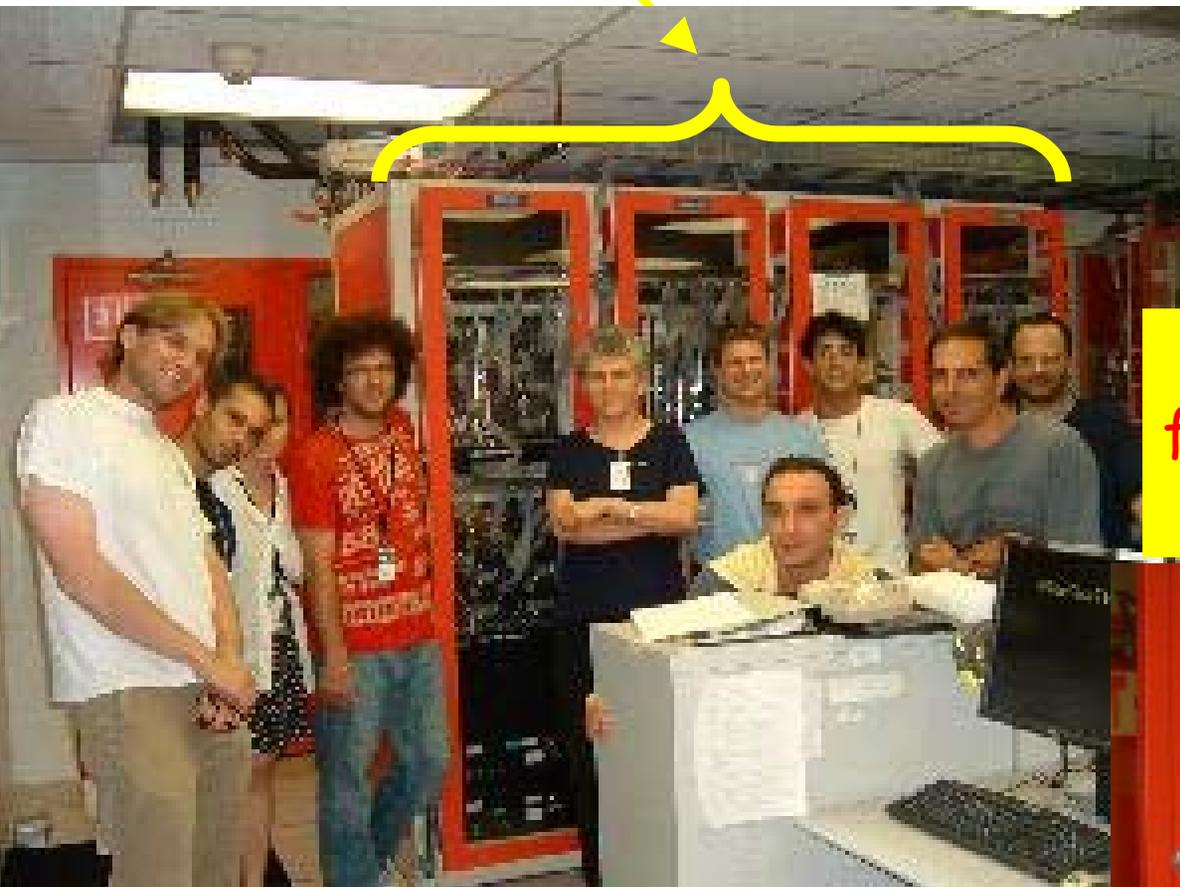
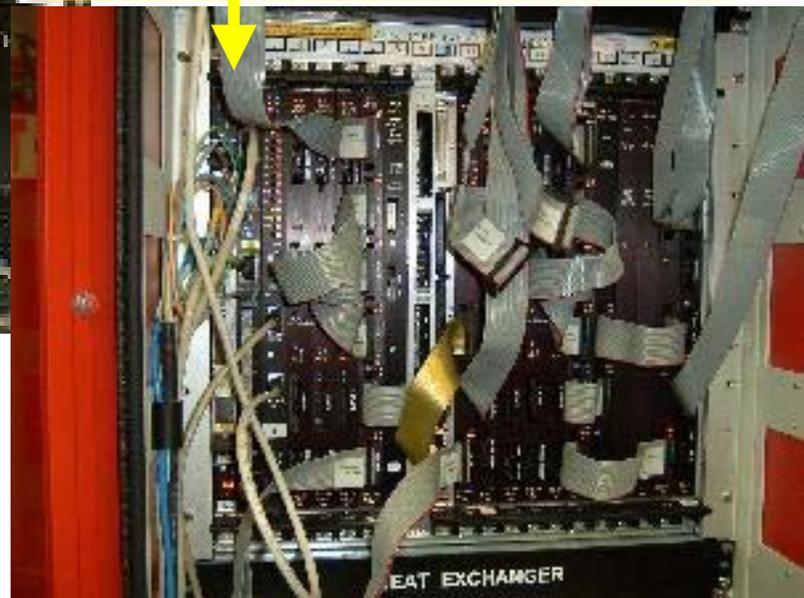


SVT UPGRADE STATUS



July 21 2005:
first AM++ & AMSRW
Inside SVT

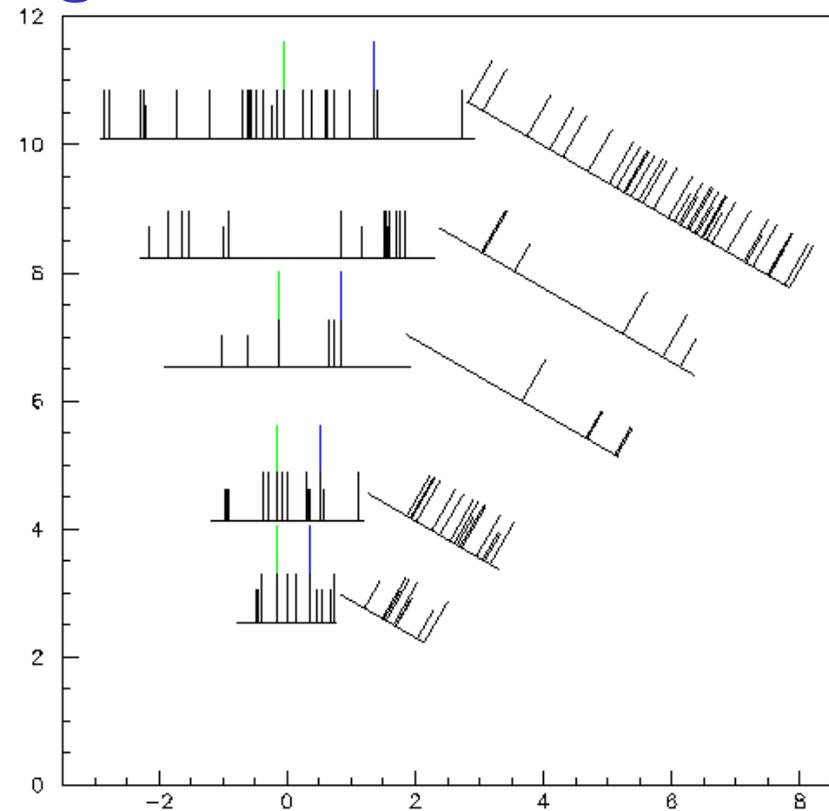
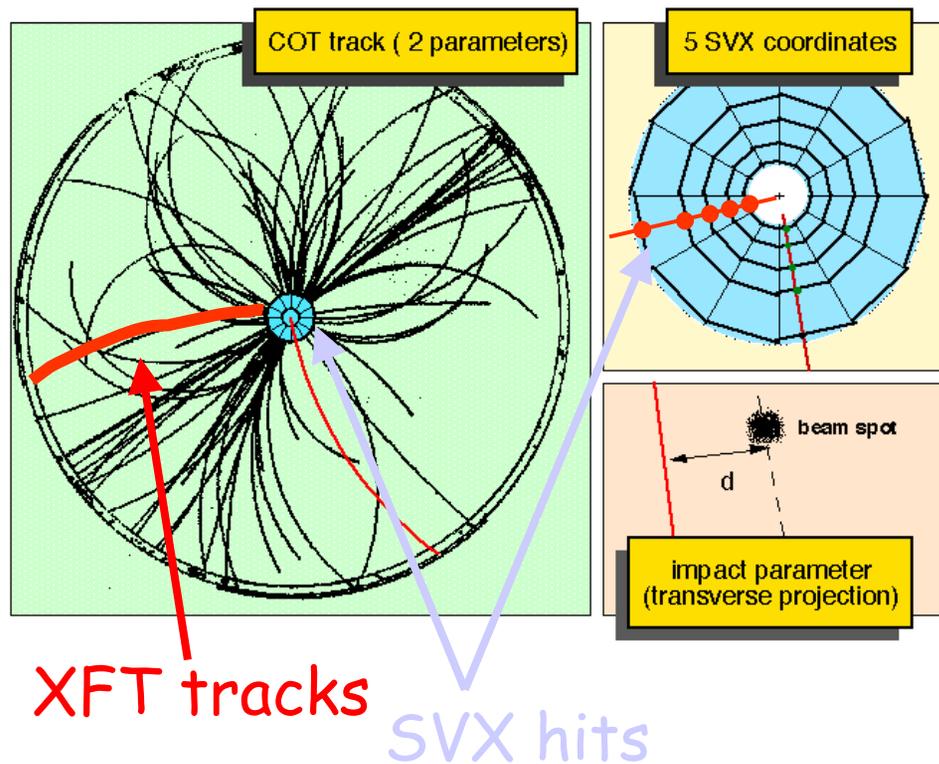


The SVT team at work in
Trigger room (90% italian)

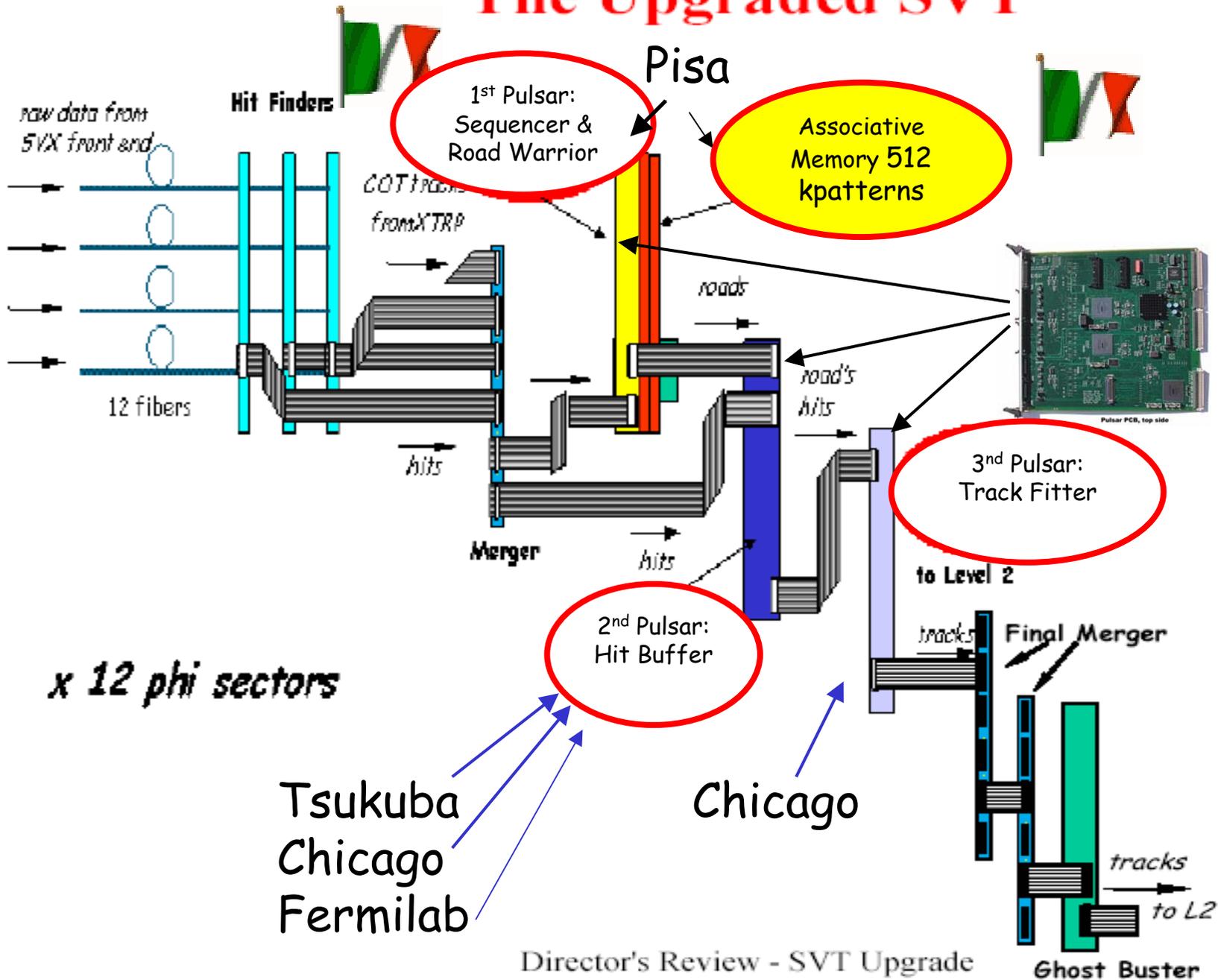
- What is the SVTupgrade
 - Why it is important
- } Short description
- Many upgrade steps at Fermilab: no shutdown
what has been done what has to be done
 - After the hardware installation algorithm optimization

SVT: Silicon Vertex Trigger

Finding tracks in the silicon



The Upgraded SVT



Large Impact on Upgrade from Italy (~20 names)

Project Leader: **Alberto Annovi**

AMchip03 project: **Sartori** Tripiccione, Pedron, Schifano (FE)
validation, test: **Annovi, Dell'Orso** Giovacchini (PI)

AM++ - LAMB **Bardi**, Giannetti (PI)

RW Belforte, Carosi, Catastini, **Spinella** (TS-PI-SI)

AMSRW Bitossi, Giannetti, **Piendibene, Spinella** (PI)

Software svtvme: **Annovi**, Giovacchini (PI)
monitoring-configuration **Carosi** Simoni, Volpi (PI)
simulation: Annovi, **Cerri** Simoni, Torre (PI-LBL-SI)
spymon: Di Ruzza, **Rescigno** (RO)

Tests: Annovi, **Giovacchini**, Torre

Installazione: **Annovi, Dell'Orso, Giannetti, Giovacchini**
Piendibene (PI), Torre (SI), Di Ruzza, Rescigno (RO)

USA: **Adelman** (TF++), Bellinger (software), Chappa (HB),
Furic (HB), Maruyama (HB), Tang (mezz.), **Shochet** (mezz.)

- **Nuova AM-board**: inizio estate 2004 (Pisa)
durante estate 2004: test con FPGA (Pisa)
- **Progetto prototipo AM-chip**: luglio 2004 (Ferrara-Pisa)
consegna chip ~2 mesi - disponibile ad ottobre.
- **Nuova LAMB**: montare nuovo AM-chip a ottobre 2004 (Pisa)
- **test del chip + scheda**: ottobre - dicembre 2004 (Pisa-Ferrara)
- **produzione**: inizio 2005 (Pisa-Ferrara)
- **installazione**: estate 2005 (Pisa-Ferrara)
- Altri **DAQ/Trigger upgrade**: previsti nel **2006**

Road Warrior: (~60 k\$ Fermilab)
messa in opera entro **fine 2003**

L1 accept rate is bottle neck

T

- L1A rate ~ 20 kHz (vs 50kHz design)

- L1A rate limited by L2 exec time

Rates at @ L=100E30 (current luminosity):

~15kHz high Pt L1A

~15kHz TTT L1A (now PS = 2)

Rates growing quadratically with luminosity

Level 2 pipeline structure:



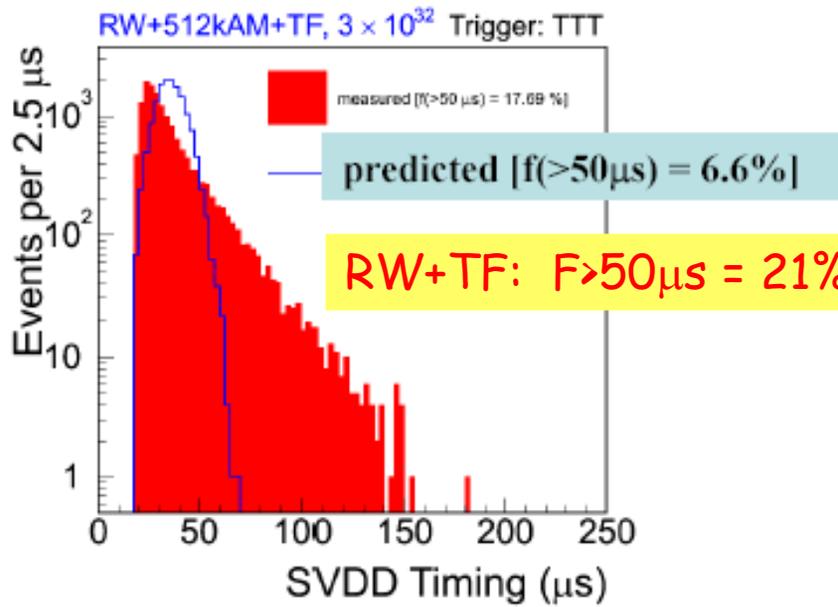
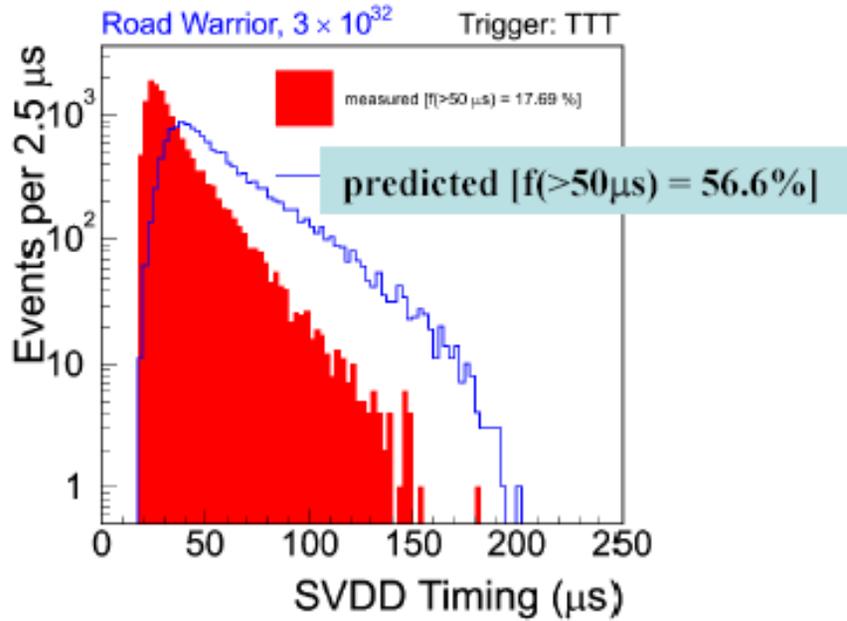
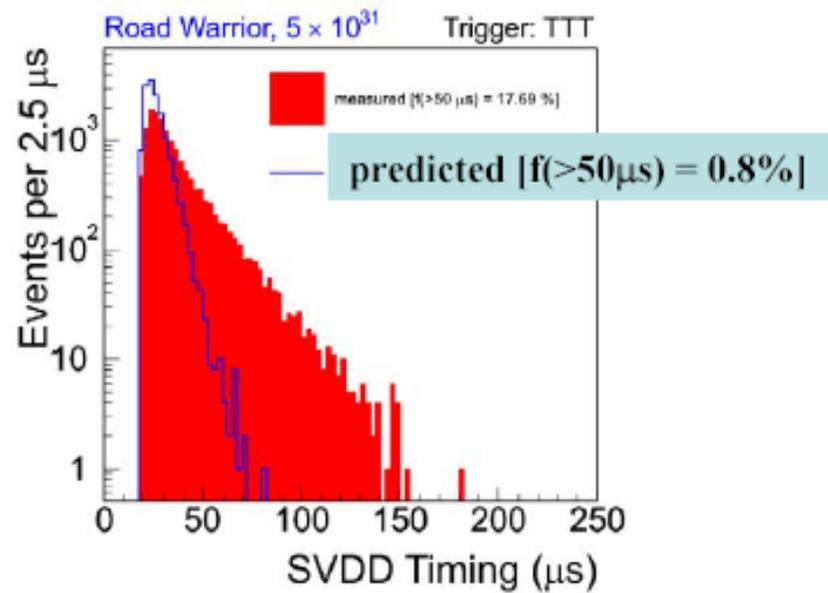
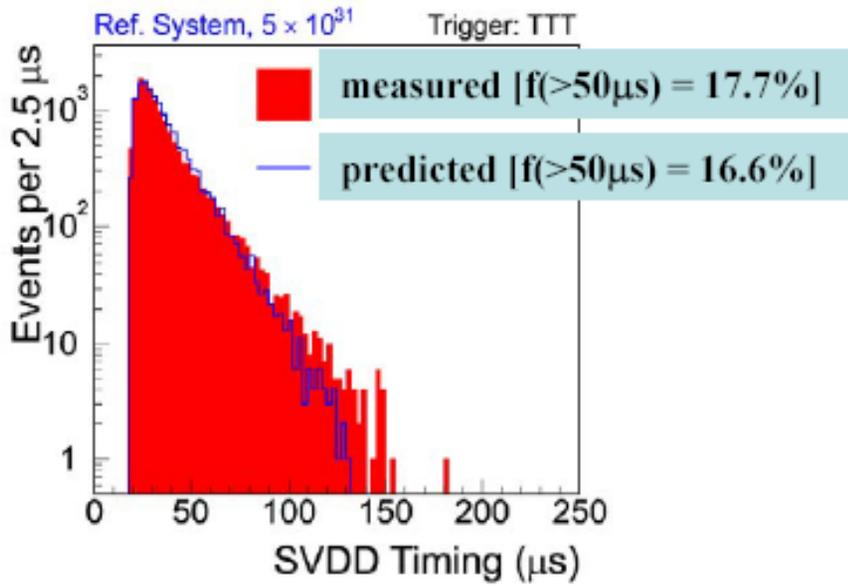
Optimized but
slower than
design

Upgrade in
progress

Upgrade in
progress

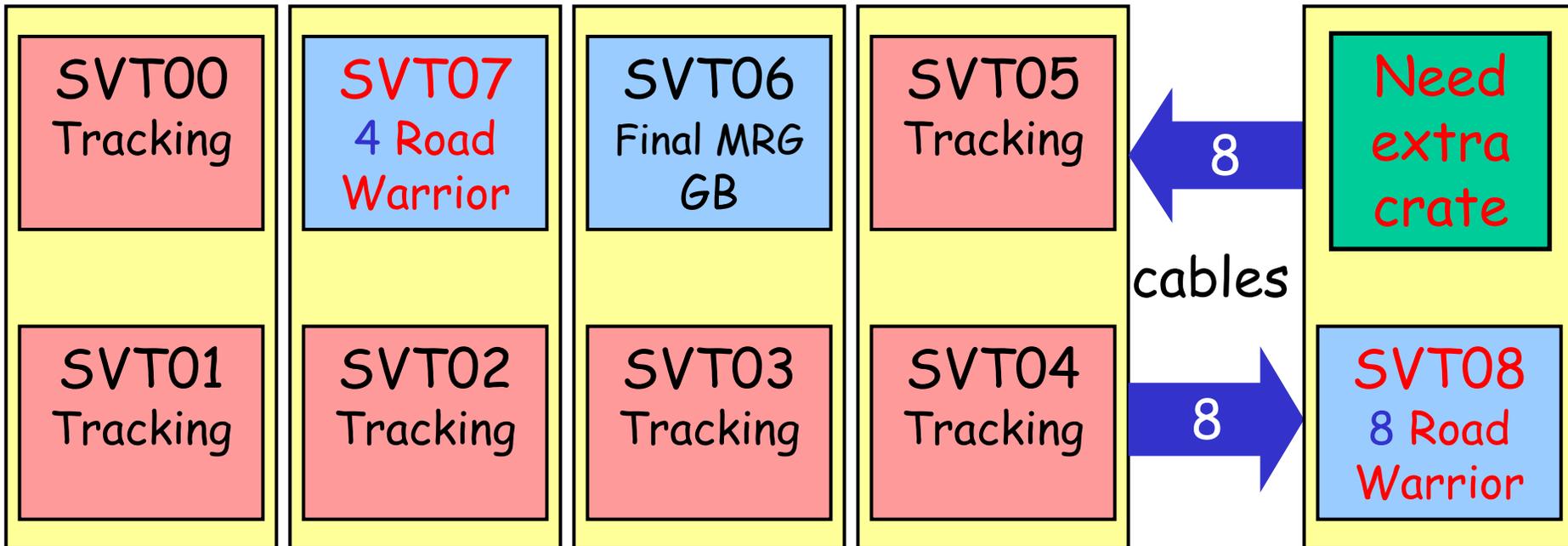
SVT upgrade has large impact on maximum L1A rate!

Extrapolate to high \mathcal{L} with & without upgrades

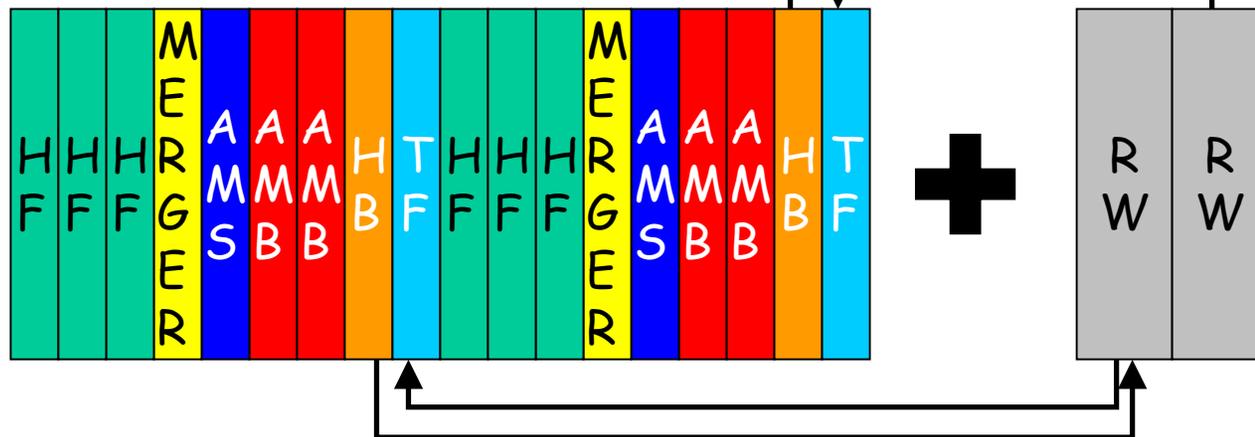


SVT before July

SVT

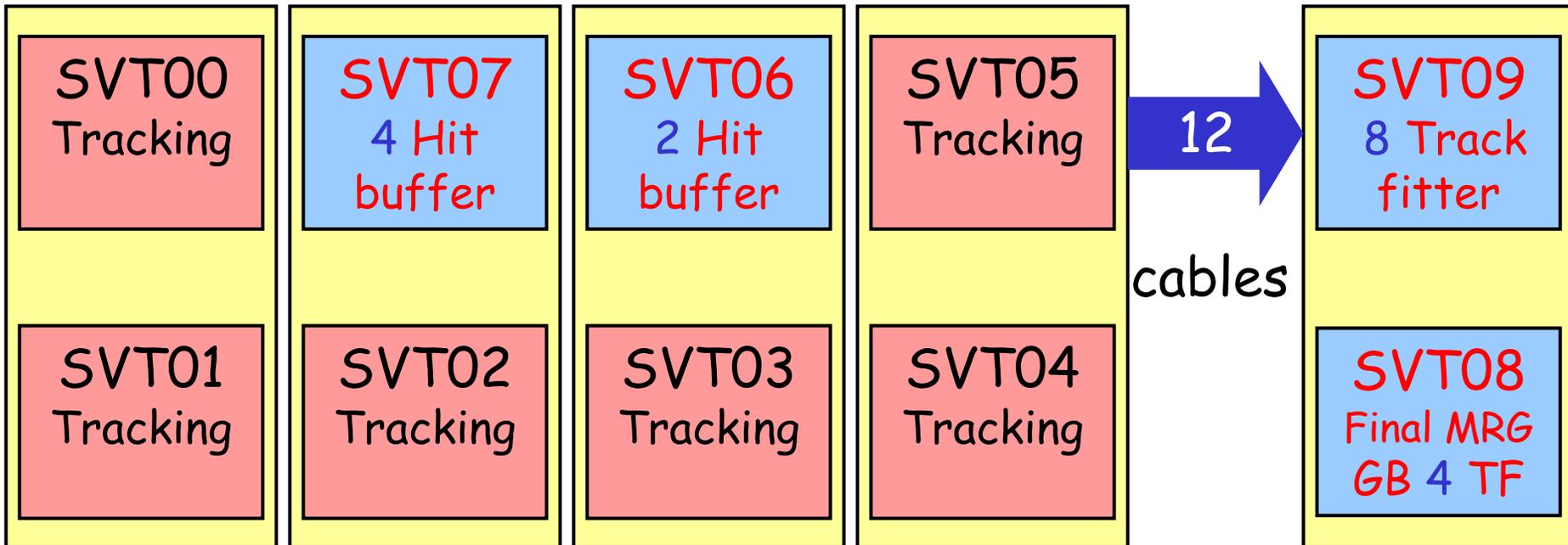


SVT tracking crate (2 wedges)

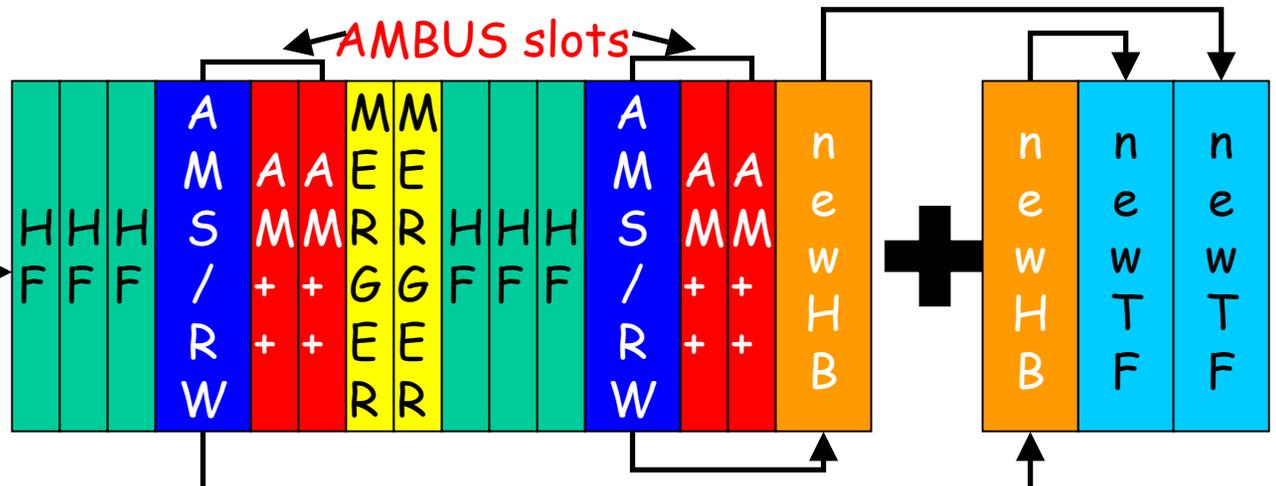


Final configuration

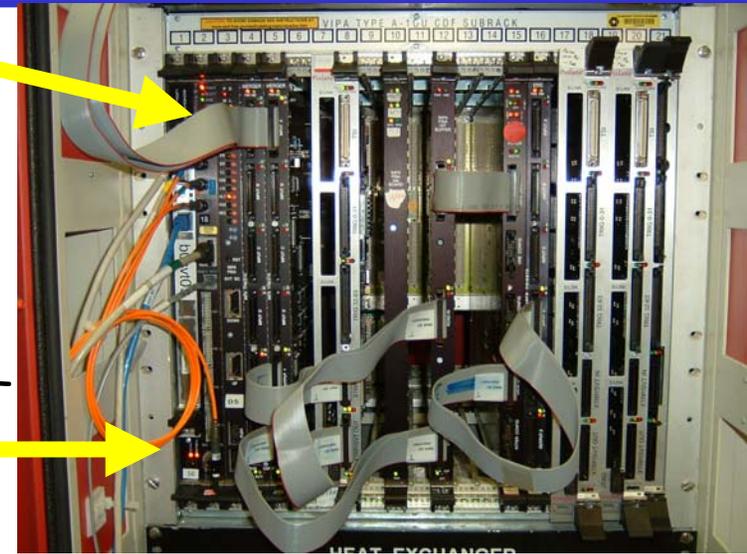
SVT



SVT tracking crate (2 wedges)



Real data



Board/software Validation (step # 0)

- Boards will be first tested in the test stand
- Then they will be tested parasitically with real data
- Need few slots in a test stand placed near SVT

Hardware installation in 3 steps:

1. AMS/RW and AM++ inside SVT (July 29)

2. TF++ installed in ex-Road Warrior Pulsars → 128 kpat

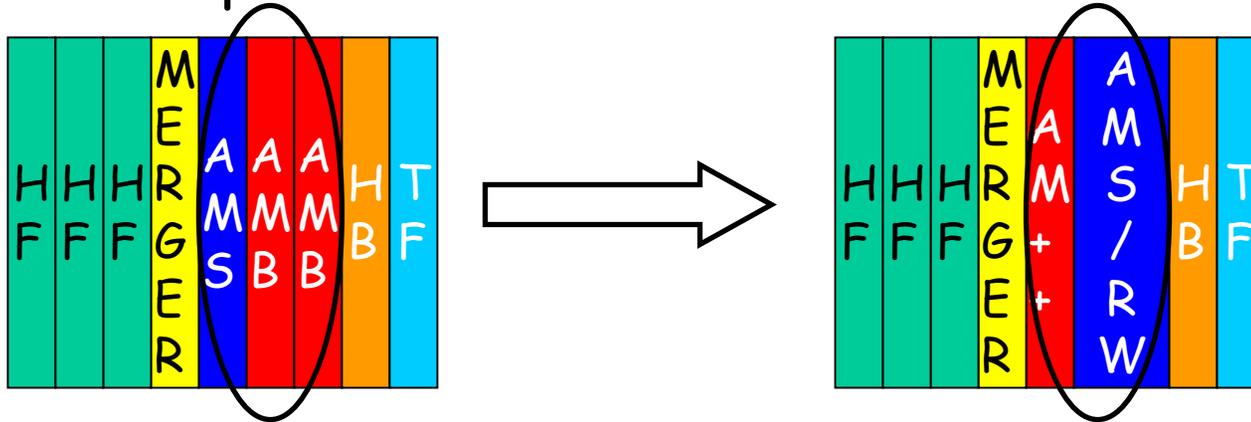
3. Install finally HB and 2nd AM++ board → 512 kpat

We are here

Study of performances - firmware optimization (4th step - 06)

Other hardware improvements?? (5th step - after 06.. may be)

- AMS/RW + **one** AM++ board have been installed with minimal impact



- Compatible with old boards** (can work with 32k patterns)
- Minimal re-cabling and reconfiguration

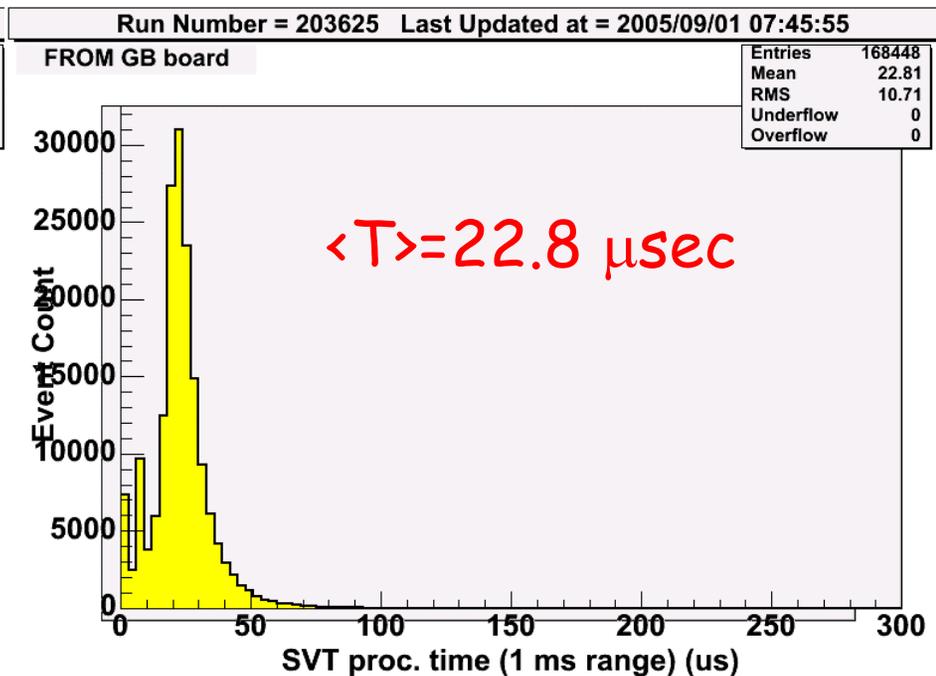
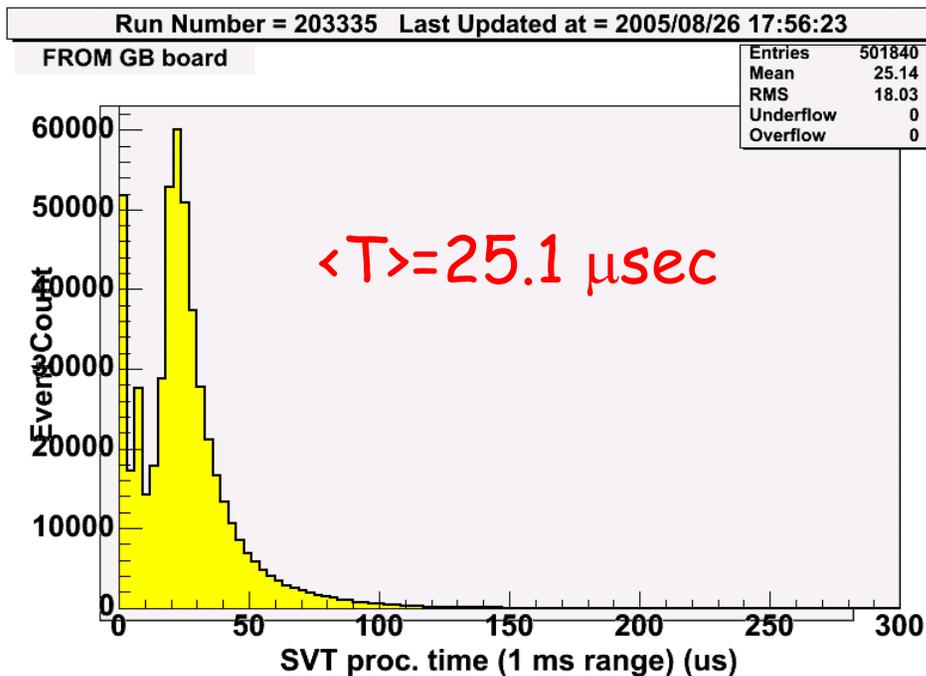
Gain: **2 μ sec** reduction on average **SVT** processing time
@Lum=[78-25]*10³⁰ due to RW moved before the HB.

August: Track Fitter installation (2nd step) SVT

After RW has been replaced by AMS/RW.

Just reprogram the 12 RW boards with TF firmware

2- 3 μsec gain at Lum=[91-81] $\times 10^{30}$

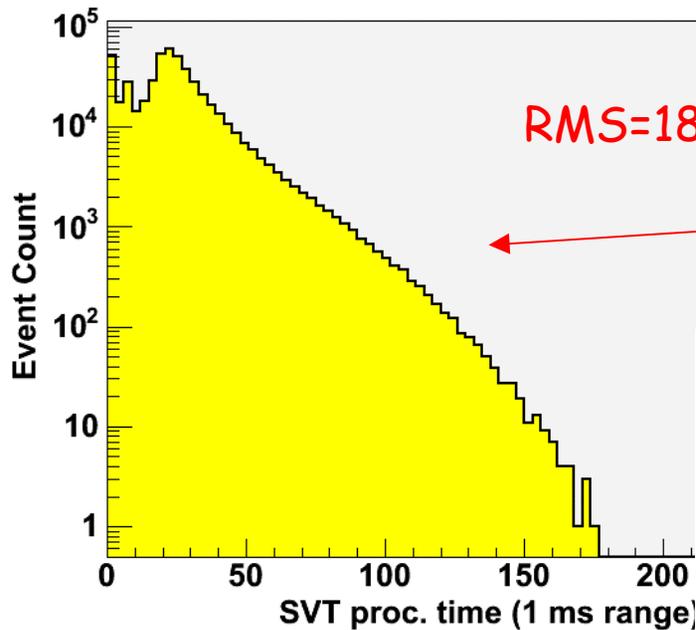


SVT timing w/TF++ SVT

Run Number = 203335 Last Updated at = 2005/08/26 17:56:23

FROM GB board

Entries	501840
Mean	25.14
RMS	18.03
Underflow	0
Overflow	0



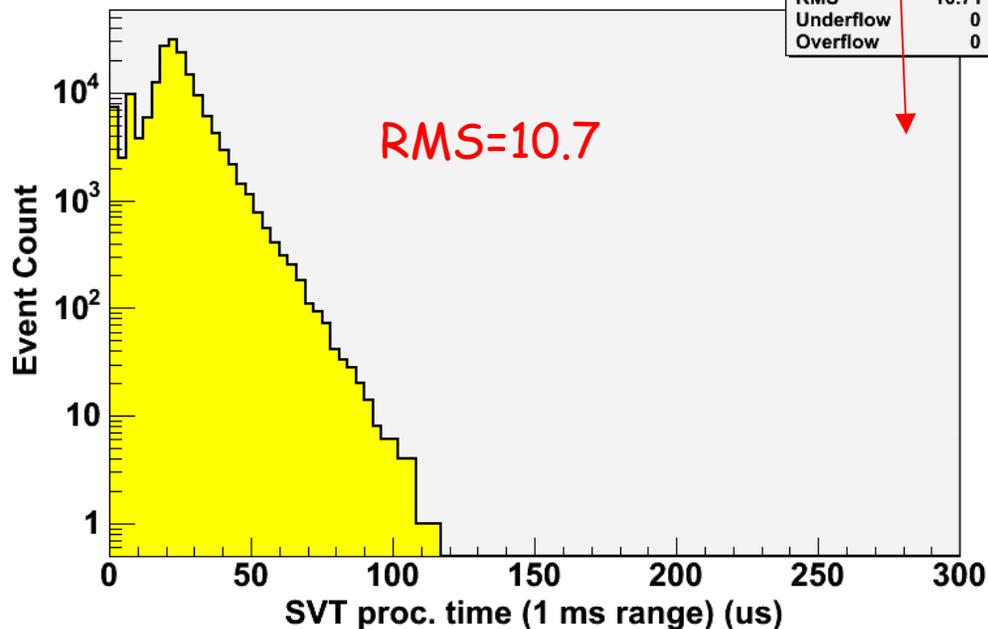
(Similar luminosities ~ 85)

TF++
Run w/TF last week

Run Number = 203625 Last Updated at = 2005/09/01 07:45:55

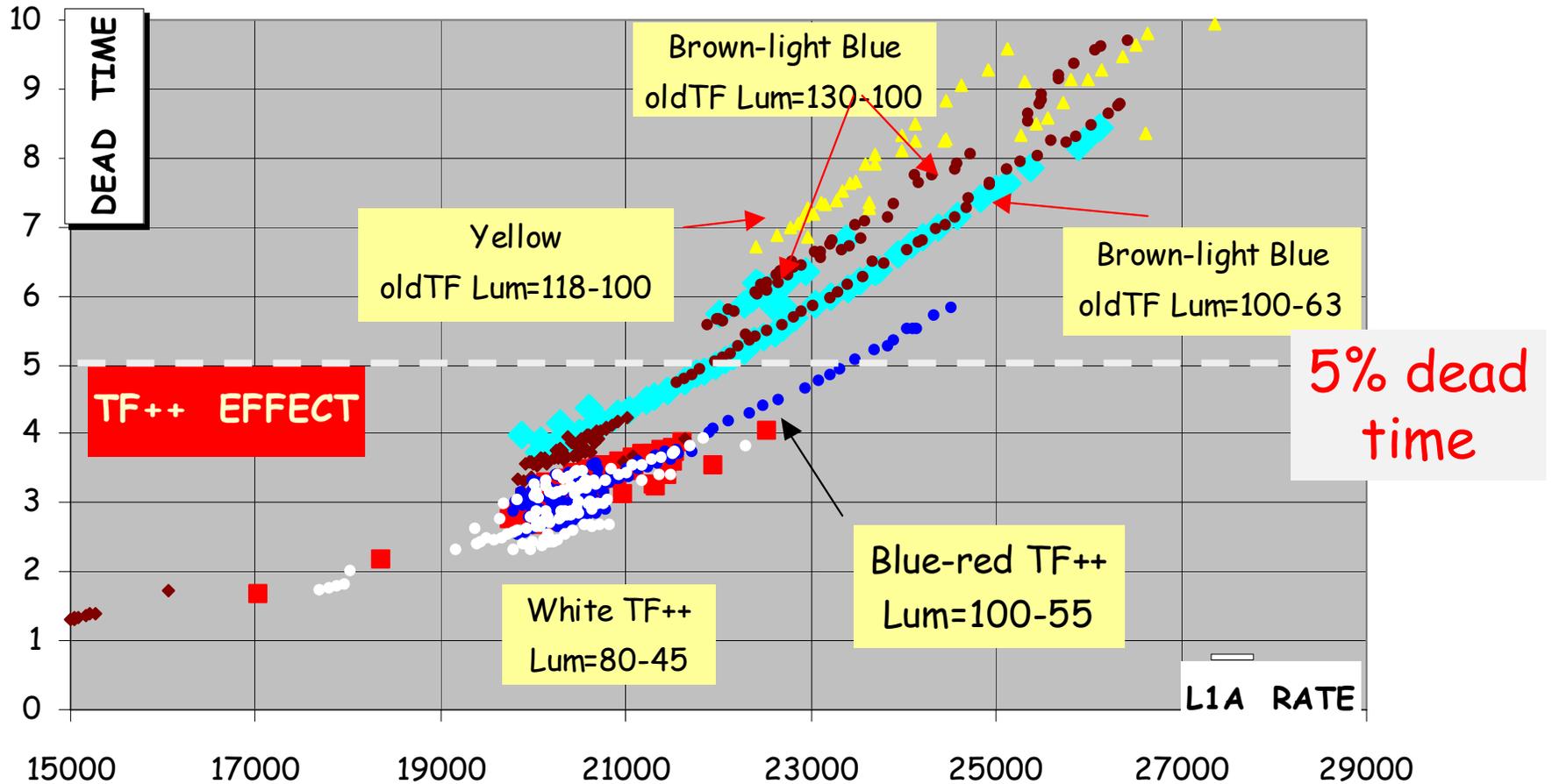
FROM GB board

Entries	168448
Mean	22.81
RMS	10.71
Underflow	0
Overflow	0

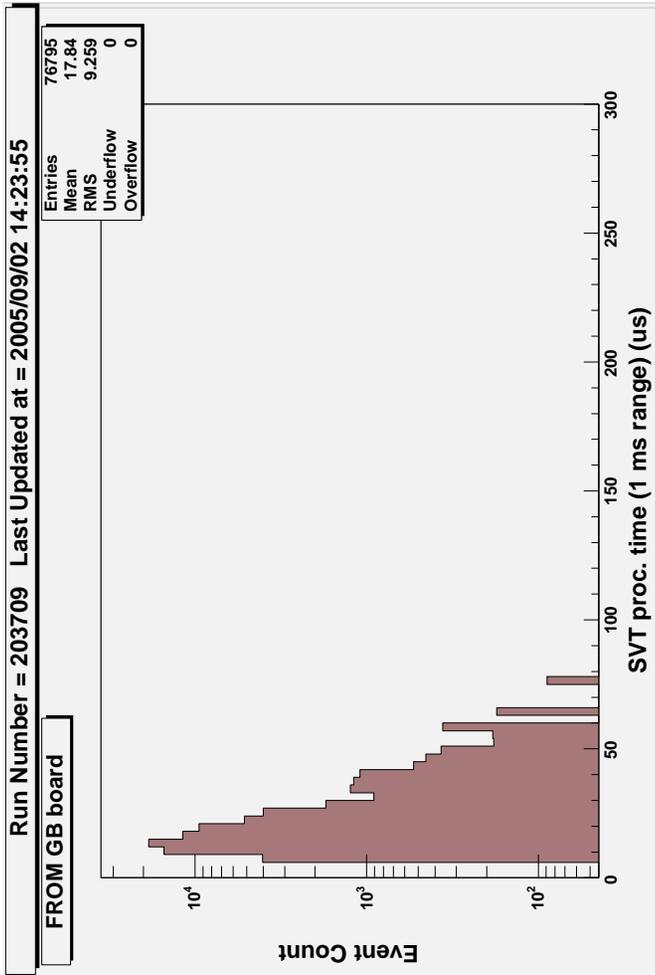


As expected, core of timing stays the same, but significantly reduced tails (look at RMS)

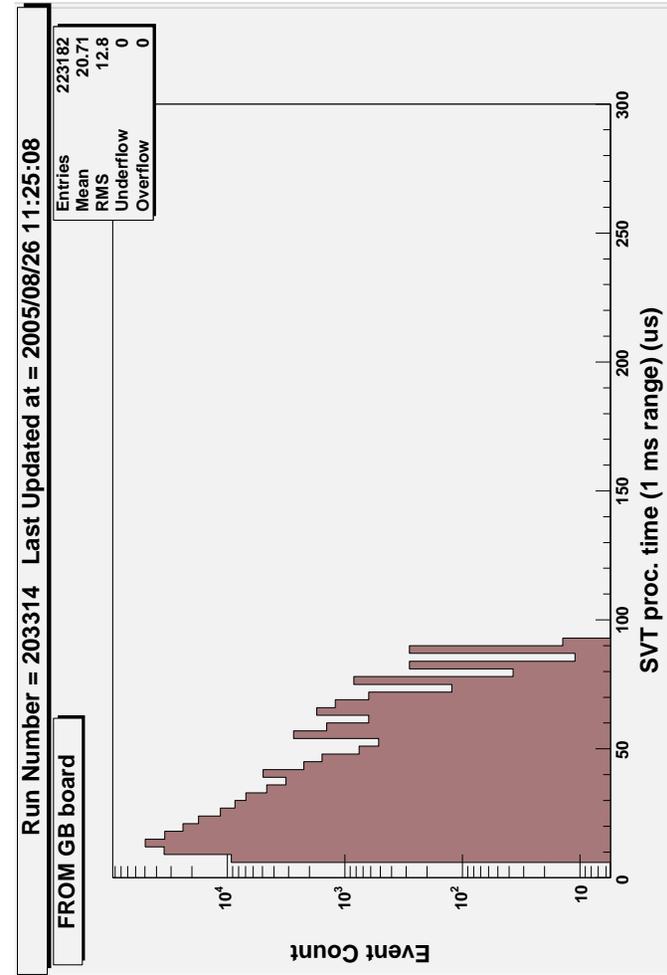
TF++ impact on L1 bandwidth



128 kpatterns vs 32 kpatterns (fakehits) SVT



$\langle T \rangle = 17.84$ RMS = 9.26

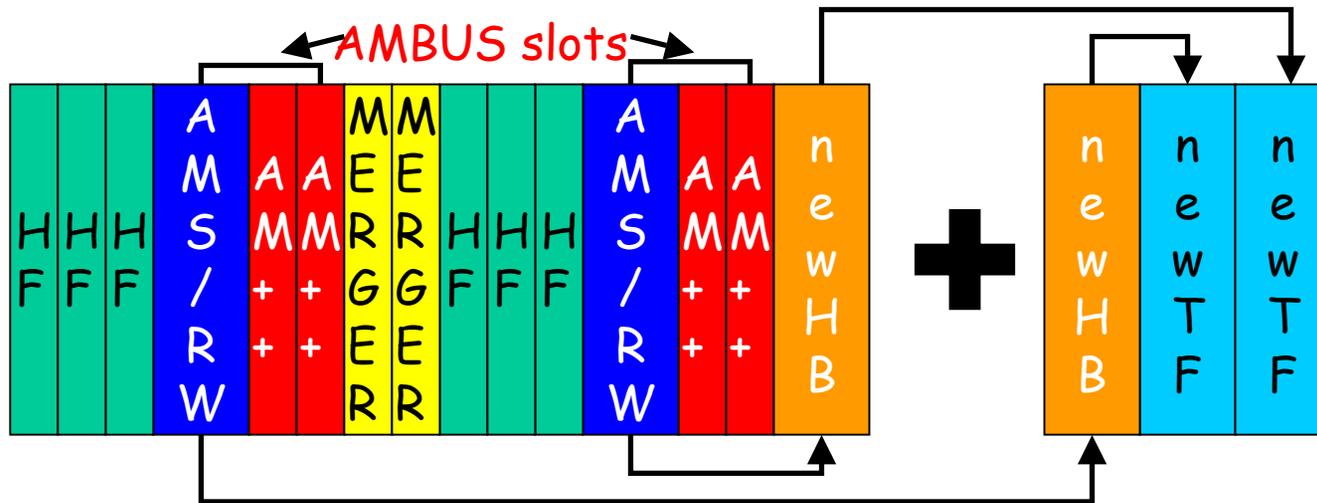
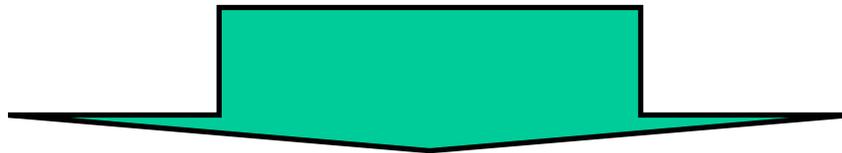


$\langle T \rangle = 20.7$ RMS = 12.8

November: HB + AM++ enlargement (3rd step) CVT



Status after
new HB
installation



Final
configuration
512 kpat/wedge

2006: better Timing → better algorithm (4th step)

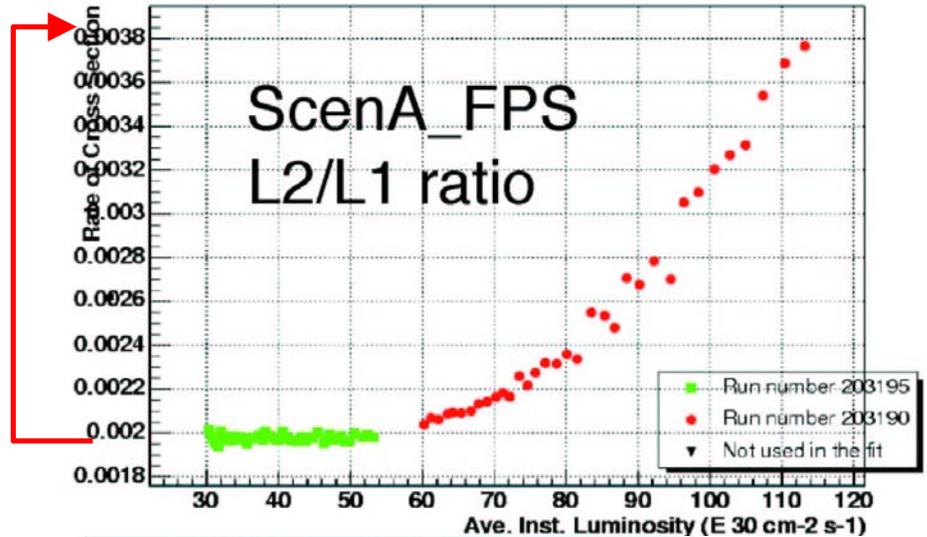
Increasing luminosity
→ Low SVT
Background rejection

x2

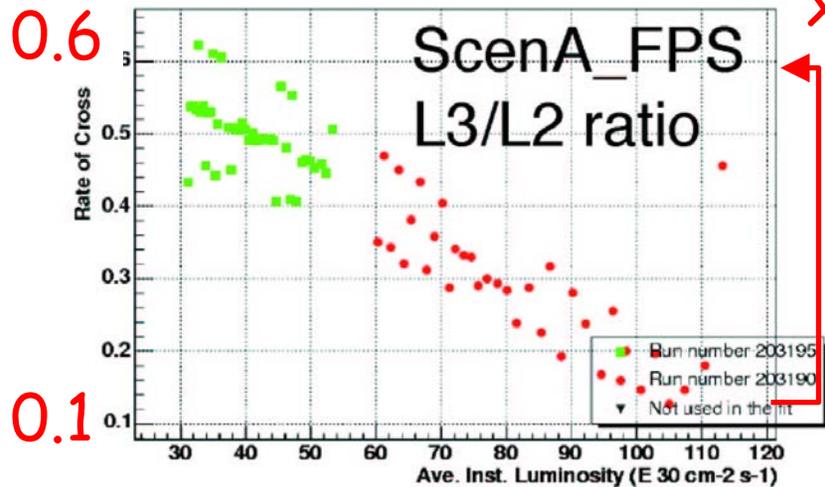
ScenA:

Two_TRK2_Oppq_Dphi135_Sumpt5.5

B_CHARM L1 FPS rate I1 I2 xsec vs. Inst. Lum



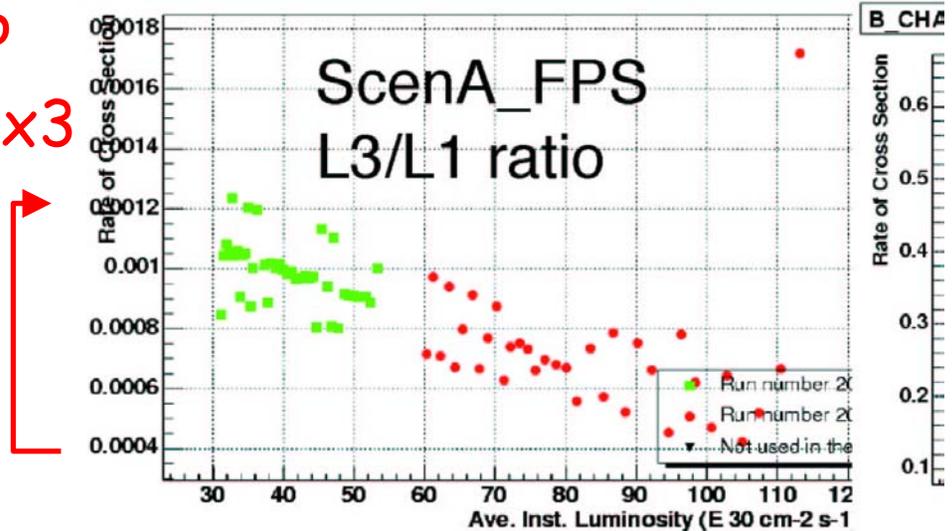
B_CHARM L1 FPS rate I2 I3 xsec vs. Inst. Lum



x6

x3

B_CHARM L1 FPS rate I1 I3 xsec vs. Inst. Lum

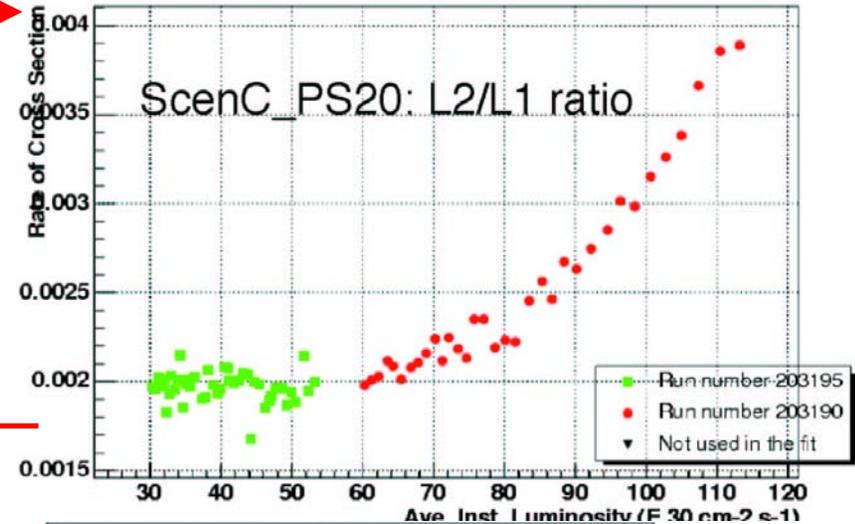


Also Scenario C shows exactly same problem VT

ScenC:

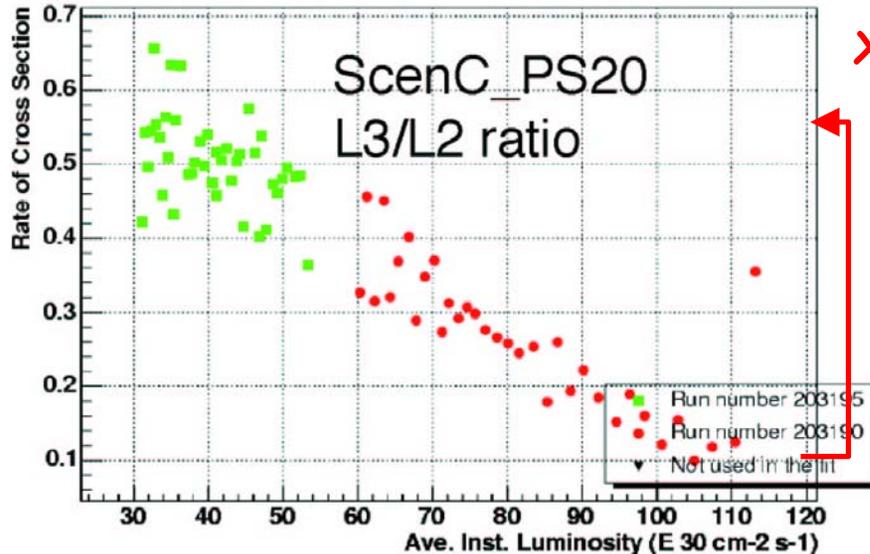
Two_TRK2.5_Oppq_Dphi135_Sumpt6.5

B_CHARM_HIGHPT_L1_PS20_rate_l1_l2_xsec vs. Inst. Lum



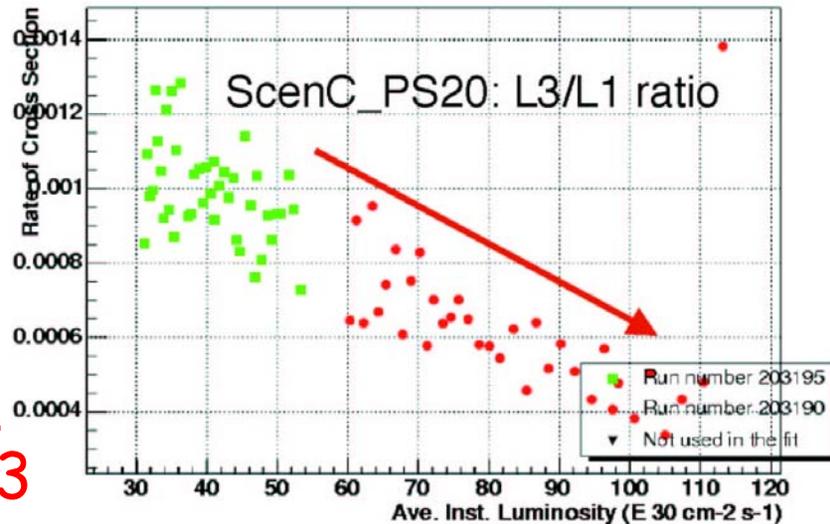
x2

B_CHARM_HIGHPT_L1_PS20_rate_l2_l3_xsec vs. Inst. Lum



x6

B_CHARM_HIGHPT_L1_PS20_rate_l1_l3_xsec vs. Inst. Lum

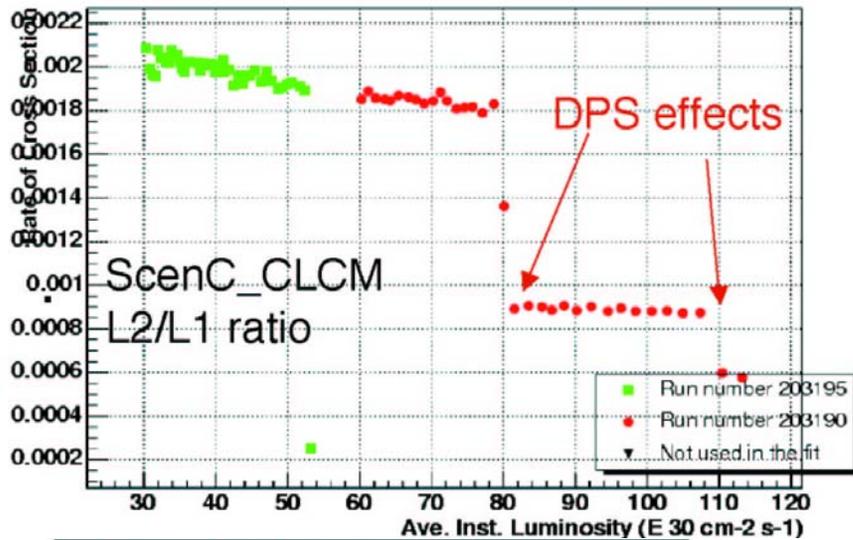


x3

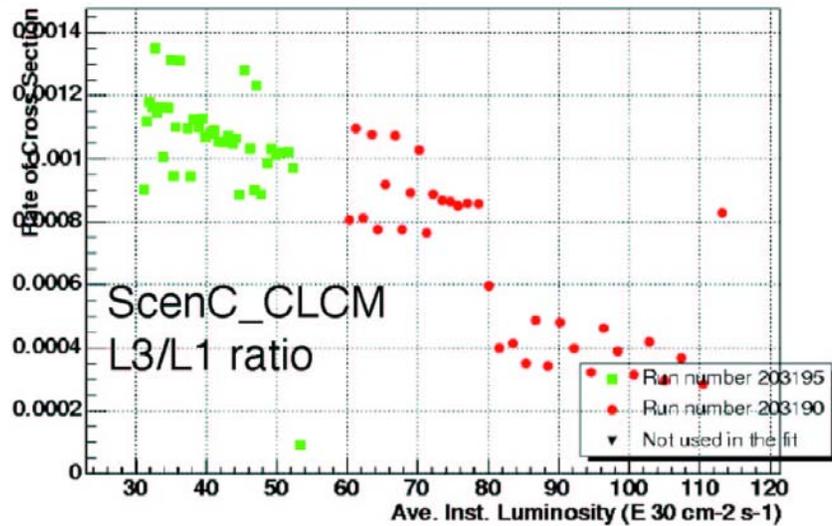
First very good idea: veto events with a large number of interactions

SVT

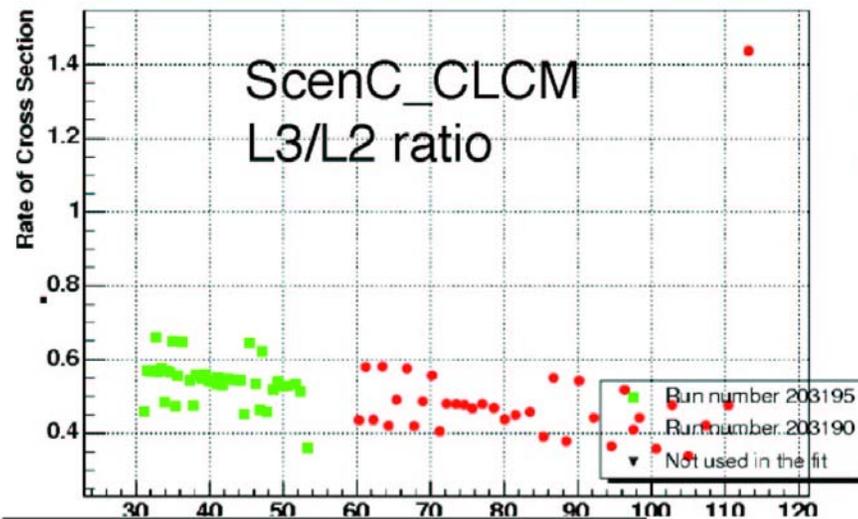
B_CHARM_HIGHPT_DPS_L1_CLCM_rate_I1_I2_xsec vs. Inst. Lum



B_CHARM_HIGHPT_DPS_L1_CLCM_rate_I1_I3_xsec vs. Inst. Lum



B_CHARM_HIGHPT_DPS_L1_CLCM_rate_I2_I3_xsec vs. Inst. Lum



MORE SVT studies:

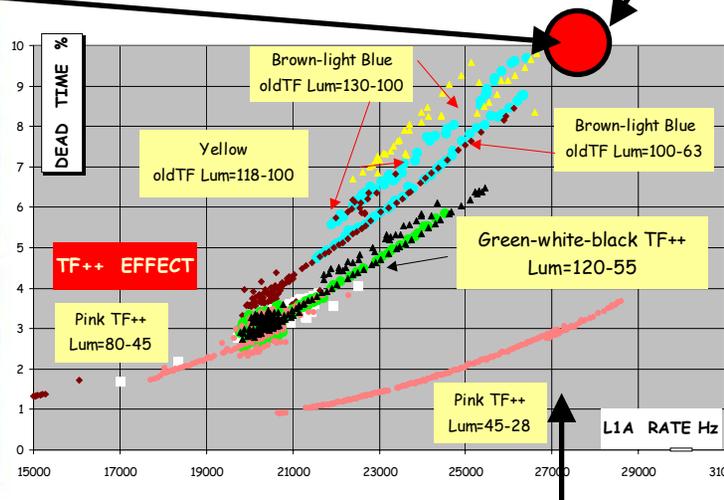
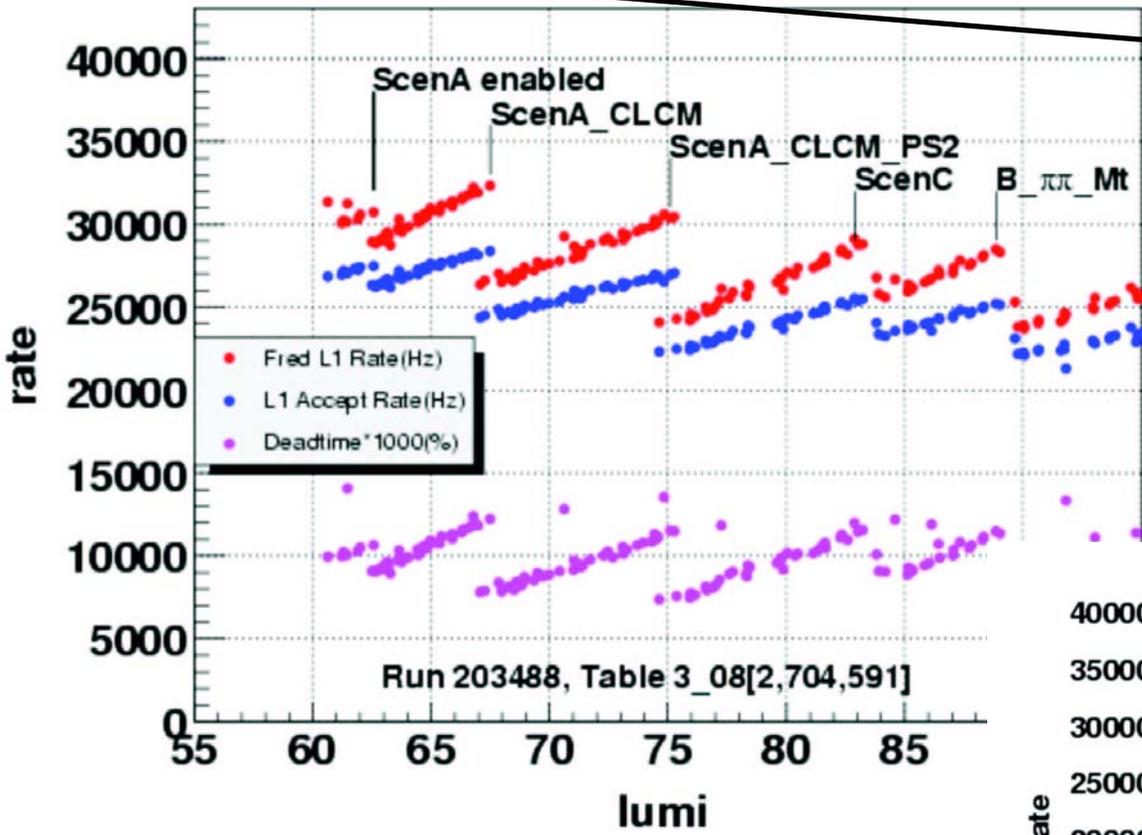
- 1) Limited # fits per road
- 2) Adjust Chi**2 cut
- 3) Adjust Hit Finder THR's
- 4) Use new XFT infos (z?)
- 5) Adjust L2 processor algorithms

B_CHARM_HIGHPT_L1_PS20_rate_I2_I3_xsec vs. Inst. Lum

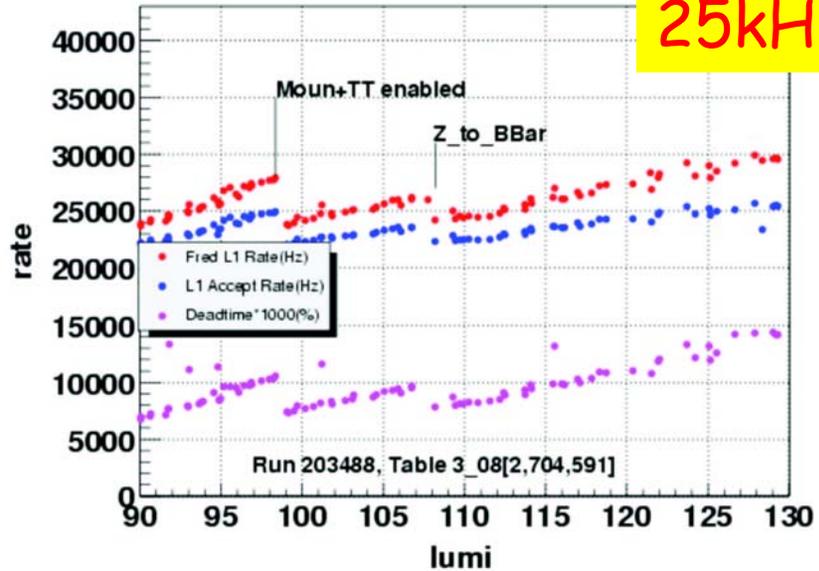
HOW to fill the available L1 bandwidth (step 4)??

New Trigger Table

10 % dead time



25kHz



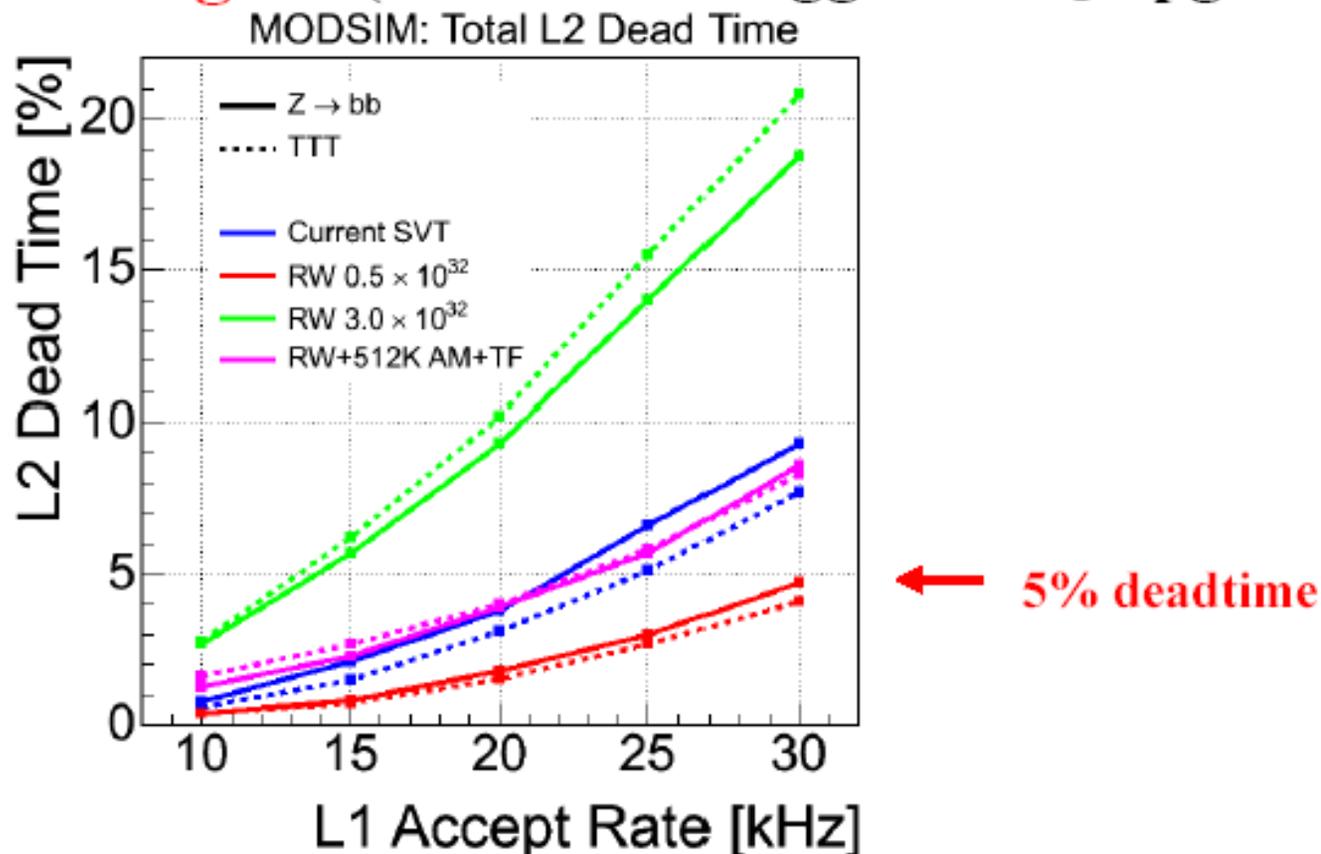
A lot of discussion!!

- **Parasitic tests** of all boards before installation
- **AMS/RW, AM++** and **TF** have been installed before the shutdown (**July- August**) **DONE**

- Complete the upgrade (**November 2005**)
- **A) Optimize Track finding: XFT-SVT-L2processors**
B) Fill L1 rate as much as possible (2006)
To be DONE
- **May be after 2006....**
GigaFitter (R&D proposed to Murst.)? More AM??

SVT
backup slides

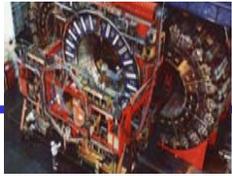
What we could gain (after other trigger/DAQ upgrades)



Maximum L1 SVT-trigger rates for 5% L2 deadtime @ 3×10^{32}

Current SVT	Upgraded SVT
13 KHz	23 KHz

CDF DAQ & Trigger



Detector
Raw Data

Level 1
pipeline:
42 clock
cycles

Level 1
Trigger

Level 1
• 7.6 MHz Synchronous Pipeline
• 5544 ns Latency

• 50 kHz accept rate

~20 kHz actual

L1
Accept

Level 2
• Asynchronous 3 Stage Pipeline
• 20 μ s average Latency
• 300 Hz accept rate

SVT here

~35 μ s actual

Level 2
Trigger

L2
Accept

Level 2
buffer:
4
events

DAQ
buffers

L3 Farm

To Mass Storage (50~100 Hz)



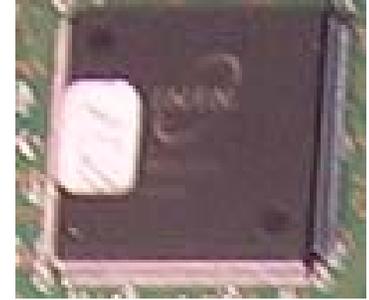
Tails are important

Year	chip	boards	devel.	Total
2003?	120 kE	10 kE (test b.)	5 kE	135 kE
2004	↑ Ferrara	10 kE (protot.)	30 kE	40 kE
2005	53 kE +40 kE +50 kE	100 kE (produc.)	+60 kE (MURST)	153 k +40 kE +50 kE

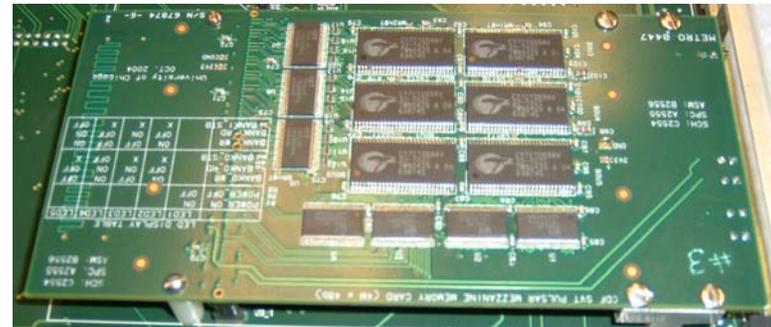
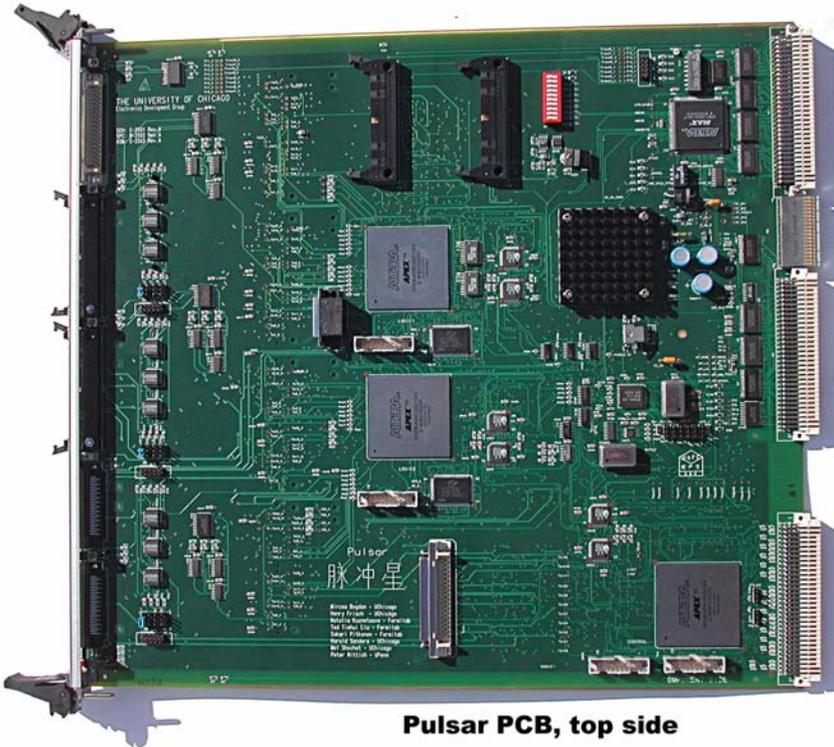
Pisa

Le Pulsar sono pagate dagli USA
totale secondo upgrade 310k\$

- Standard cell **AMchip prototype working >40MHz**
 - Production received: **evaluating yield**
- LAMB and AM++ vme board:
 - **3rd prototype build and tested**
 - **Need final test w/ board full of AMchips**
- **Building a 4th AM++ vme board prototype**
 - fix minor issues
 - Production available by **June**
- **ON SCHEDULE**



- AMS and RW firmware implemented and tested
- next step implement SVT firmware tools
- ON SCHEDULE

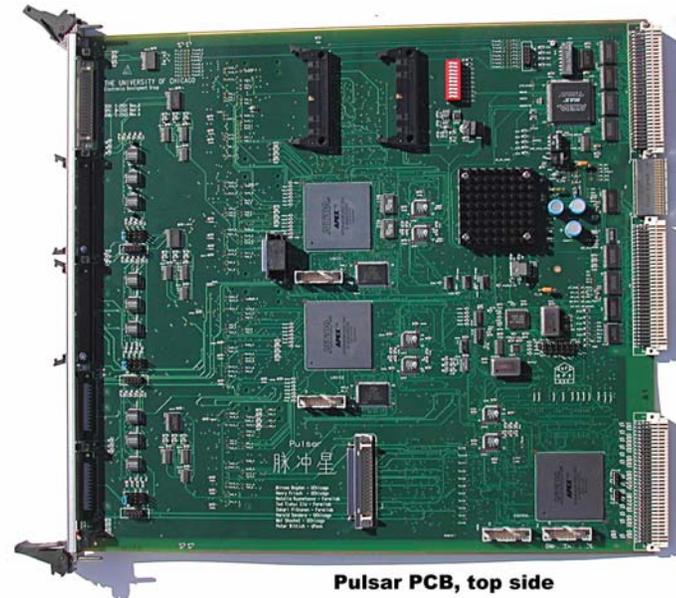
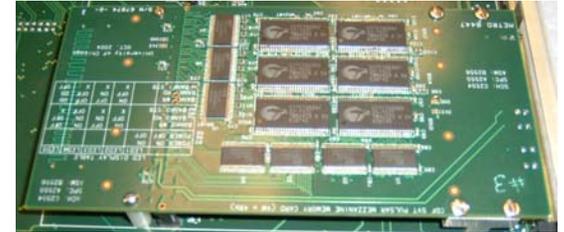


Pisa had the most risky responsibilities,
but we are now in very good shape

Non italian responsibilities

SVT

- Pulsars
 - Pulsar production arrived
 - Large RAM mezzanine production done
 - Small RAM mezzanine prototype under test
 - ON SCHEDULE
- TF
 - First firmware written
 - Standalone tests starting
 - ON SCHEDULE
- HB
 - Firmware writing just started
 - BEHIND SCHEDULE
 - More man power (firmware engineer joined)



Software and integration

SVT

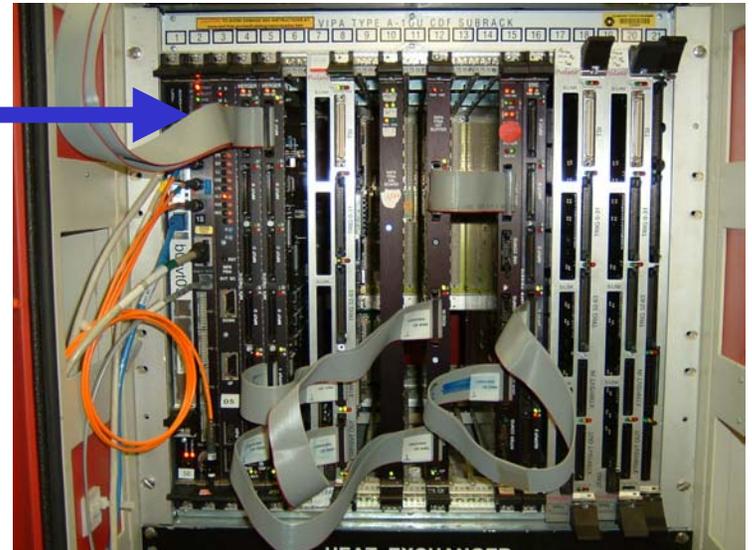
- SOFTWARE

- Work in progress
- **Critical** part for **test** and **installation**
- **BEHIND SCHEDULE**
- **project reorganized** after internal review
 - **4 main blocks** identified
 - coordinators assigned: **R. Carosi, A. Annovi, A. Cerri, M. Rescigno**
- **Additional man power** (w.r.t. baseline) **mostly Pisa people**
- **CAN RECOVER**

- INTEGRATION

- **Vertical slice parasitic test** begun with **AM++** and **AMS/RW**
- **Add boards** as they become available

Real data



Installation plan

- Fermilab goal was to install during the shutdown
- Shutdown postponed to October (at least)
- Plan to install 128k patterns per wedge by July/August
- Installing also new TF (as soon as it is ready)
- Take advantage, as soon as possible, of
 - better AM resolution
 - RW function moved before HB
 - faster TF