



# CDF Silicon in Run 2b

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J. Incandela

CDF Week

May 19, 2000

- Motivation
- Recent Workshop
- Key Issues
- Emerging View

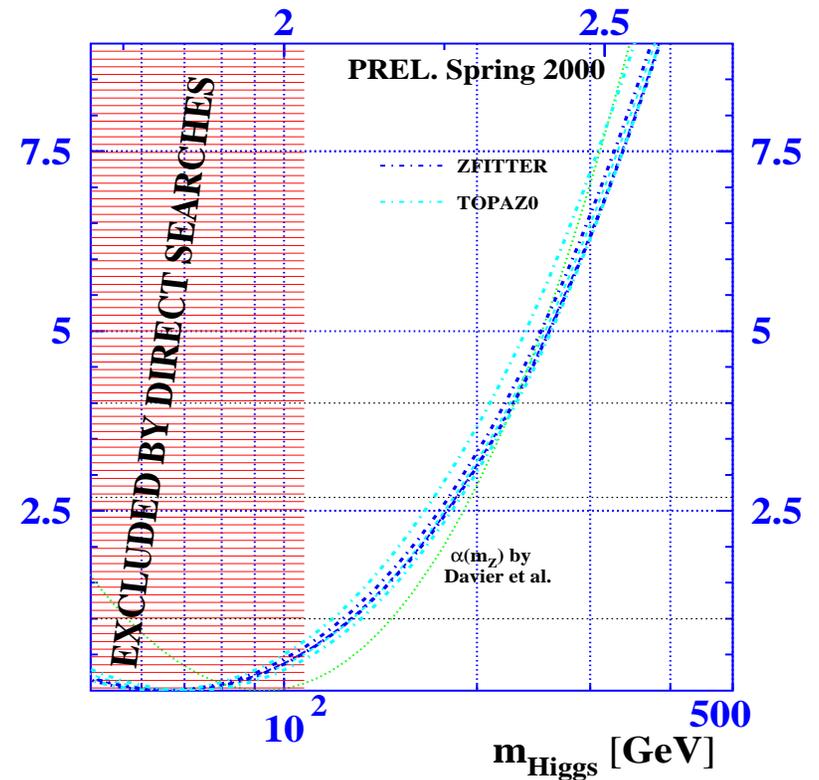
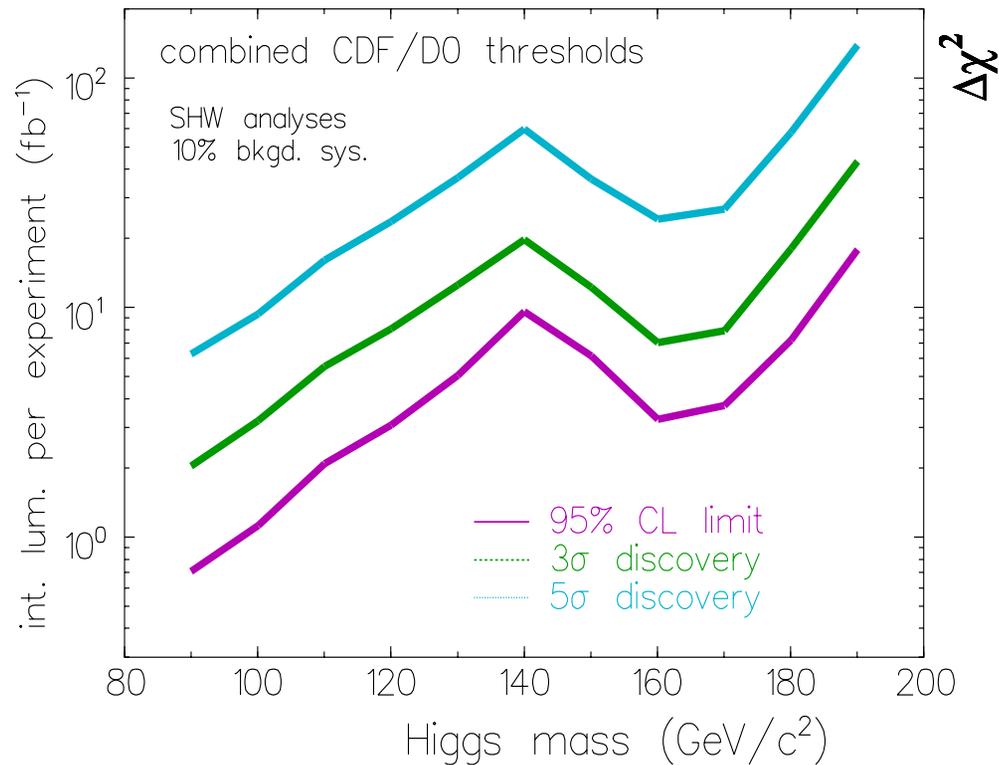


# Motivation

- CDF and DØ can make major advances with adequate data.
  - SUSY/Higgs workshop: 30 fb<sup>-1</sup> per experiment ⇒
    - SM Higgs evidence or exclusion up to ~180 GeV
    - Work in progress may yield more sensitivity
  - Significant new sensitivity to SUSY partners
  - Major advances in bottom, top, and W physics
- To maintain the energy frontier
- CDF and DØ silicon detectors were designed for ~3 fb<sup>-1</sup>
  - In hindsight, this was a mistake.
  - We need to replace the silicon after several years of operation and do so in a way that facilitates our ability to accumulate as much data as possible for as long as possible.



# Higgs Search



- Precision EWK and LEP2 measurements  $\Rightarrow 110 \leq M_H \leq 188 \text{ GeV}/c^2$  (95% CL)
- This has significant implications
  - CDF and D0 could be sensitive here IF we get enough data
  - This is arguably the toughest range for the LHC



# CDF Run 2b Si Workshop

- Workshop held March 15 at FNAL
- Large attendance
- Agenda
  - Beam conditions/expectations
  - Run 2a detector review
    - Radiation and lifetime
    - Performance
    - Material
  - Run 2b Issues
    - Rad-hard strips, pixels, diamonds
    - Electronics and DAQ issues
  - Formation of Working Groups
    - silicon technologies (S. Worm)
    - pixels (W. Wester)
    - chip development (M. Garcia-Sciveres)
    - overall layout (N. Bacchetta, C.Haber, & J. Incandela)

- Key Issues:
  - Strips, Pixels, Diamond
  - Low-risk, low-cost solution that allows for extended running
  - One-for-one replacement or SVX/L00 rebuild
  - Readout chips



# Beams Div. Plans for Run 2

- Presentation by Mike Martens of FNAL BD
  - Expect to operate in the range  $980 \leq E_{\text{BEAM}} \leq 1000$  GeV (traditional margin  $\sim 30$  GeV)
  - Luminosity Goals Run 2a (duration  $\sim 2$  years)
    - $L_{\text{peak}} = 2 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$  and switch to 103 bunches at  $\sim 1 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$
  - Luminosity Goals Run 2a (duration  $\sim 4$  years)
    - Increase pbar intensity by 2-3
    - $L_{\text{peak}} = 5 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$  @ 103 bunches
    - Luminous region anywhere from  $\sim 10$  to  $\sim 25$  cm depending on crossing angle, transverse emittance, and  $\beta^*$
  - Luminosity leveling possible (but looks kind of like luminosity dumping)
- Goal is to achieve
  - $2 \text{ fb}^{-1}$  by the end of Run 2a
  - **$15 \text{ fb}^{-1}$  by the end of Run 2b:**
  - Implement luminosity leveling and 132 ns bunch spacing to limit multiple interactions
  - There exist technical uncertainties and difficulties that will only be resolved by experimentation during Run 2a

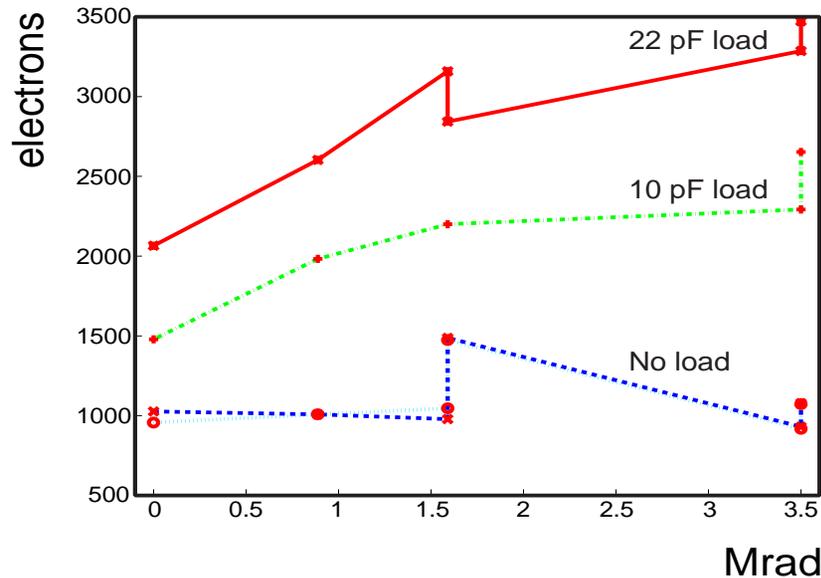


# Run 2a Component Lifetimes

- Lots of information, needs to be digested and refined a bit...
  - SVX3D Chip (CDF 4461 and Communications with M. Garcia-Sciveres, A. Sill)
    - Noise increases with dose
    - Chip continues to work to high dose but with increasing leakage currents
  - Compact Port Card (CPC) and DOIM (Y. Gotra)
    - CPC tested to > 400 krad and still working  $\Rightarrow$  lifetime of 10-20 fb<sup>-1</sup>
    - DOIM tested to 1.3 Mrad and still working but see that light output dips already at 400 krad. In some cases, it's very marginal.
    - May need replacement for extended running:
    - New technology exists, more robust and cheaper but engineering is needed.
    - We need a bit more information at higher radiation doses
  - Silicon (S. Worm, G. Bolla, N. Bacchetta)
    - Layer 0 dose rate most likely  $0.46 \pm 0.14 \times 10^{13} \text{ cm}^{-2}/\text{fb}^{-1}$
    - This may imply 5-7 fb<sup>-1</sup> for Layer 0 of SVXII, 7-10 fb<sup>-1</sup> for L1 and > 10 fb<sup>-1</sup> for L00
    - In past we used 75% higher damage rate due to uncertainty in run 1 dose rates

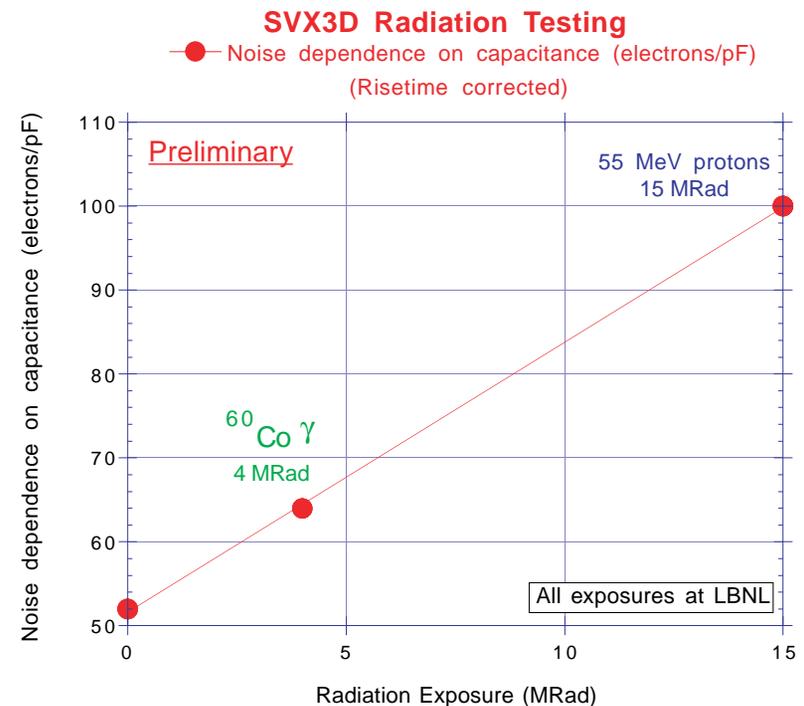


# SVX3 Irradiation



- Alan Sill et al. (very preliminary)
  - Noise vs capacitance depends on dose
    - Doubles after roughly 15 MRad
  - Noise at zero load also rises with radiation
    - Doubles after roughly 10 MRad

- D. Sjorgren et al. CDF Note #4461
  - 3.5 Mrad dose, 22 pF loaded channel saw noise increase > 50%.
  - Even at 2 Mrad ( $\sim 5 \text{ fb}^{-1}$  at  $R=2.8 \text{ cm}$ ) the noise increase is significant.
  - 1 chip was irradiated to 6 Mrad and no longer functioned.



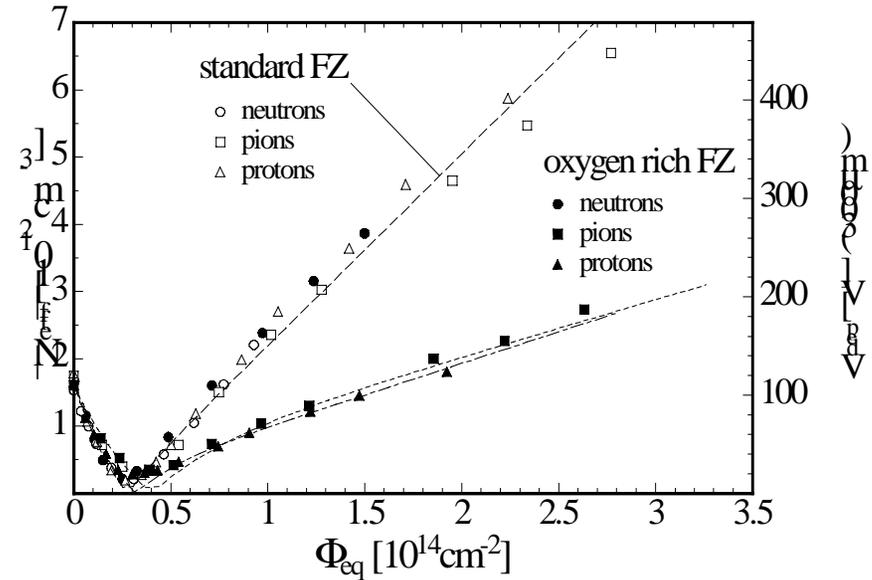
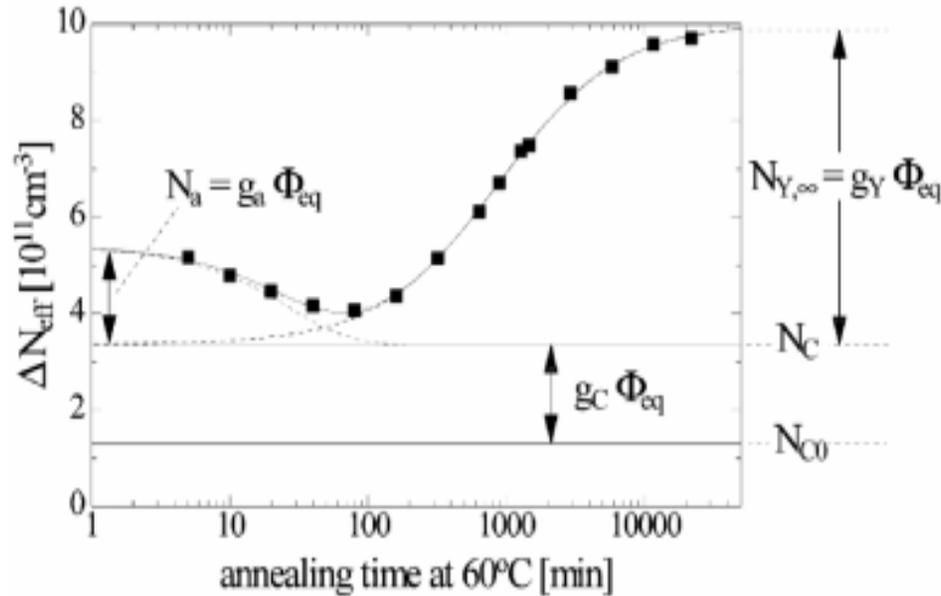


# FE Readout Chip

- Honeywell 0.8  $\mu\text{m}$  (Special rad-hard fabrication line)
  - Willing to make us more in next year or so at a cost of 20k\$ per wafer and 25-30% yield
- N. Bacchetta - 0.25  $\mu\text{m}$  technology (standard fabrication: IBM or TSMC)
  - Charge trapping in gate oxide eliminated because it's thin  $\Rightarrow$  electron tunneling.
  - CMS APV25 chip - recent results show no degradation at 80 Mrad
  - low cost, design tools very reliable - few submissions required. Yield  $\sim$  80-85 %.
  - D. Stuart, N. Bacchetta - APV25 in CDF, R. Lipton, A. Bean - APV25 in DØ
- O. Milgrome - translation of SVX3D to 0.25  $\mu\text{m}$ 
  - could conceivably do a translation in under 1 year
    - lose some functionality and noise higher unless tweaked/optimized for higher current
    - dynamic range would be reduced and power supplies would need modification
      - > (rails voltages are  $\pm 2.5$  V instead of  $\pm 5$  V)
- R. Yarema redesign SVX3D in 0.25  $\mu\text{m}$ 
  - Would want to redesign and simplify, clean up SVX3D design: 2 FTE for 2 years
  - 3-4 submissions at 30k\$ and 1-2 production runs at 160k\$ each + 3k\$ per extra wafer
  - 400 chips per wafer. Would have enough chips to
  - Total cost for everything is 1.1M\$ and including significant contingency
  - Issue is one of FNAL priorities



# Strips



- N. Bacchetta on Microstrips

- Reverse annealing

- doubles effective damage
    - strongly temperature dependent. Effectively eliminated near 0°C.

- Oxygenated detectors (will be installed in L00 for Run 2a)

- Smaller damage coefficients for charged particle but not for neutrons
    - Our neutron environment will probably be low enough to benefit
    - **15 fb<sup>-1</sup> at radius of 1.5 cm is achievable**



# Pixels and Diamonds

- **W. Wester on Pixels**

- R&D well-advanced
- pixel system for CDF would be attractive and may be achievable
  - Results for FPIX chip with ATLAS sensors  $\Rightarrow$  Very good impact parameter resolution
  - FPIX Chip developed for Tevatron experiments but only BTeV so far involved.
    - **Peripheral readout redesign required for CDF  $\Rightarrow$  not a big job.**
    - **Some new DAQ is of course required**
    - **Designed to be used in a fast trigger**
  - Lots of R&D on cooling and low mass designs.
  - Estimates of cost are not too terribly high.

- **J. Conway on Diamonds**

- Lots of improvements have been seen in the past 10 years but...
  - $\exists$  response non-uniformities
  - require extremely low noise readout ( $\sim 300$  enc for  $\sim 5$ -10 pf load)  
 $\Rightarrow$  still a ways off.



# Run 2a Problems

- **Double-sided silicon**
  - difficult to manufacture and to handle
  - not rad-hard
  - saves little material (silicon does not dominate the material budget)
- **Mounting hybrids on silicon increases technical difficulty and cost**
  - many constraints result for hybrid design
  - excess material (two ceramic substrates instead of one)
  - greater risk of damage
  - operational complications
    - **cooling**
    - **noise pickup**
    - **communication from one side of ladder to other via jumpers or folded flex**
- **Honeywell readout chips**
  - Small rad-hard production facilities carry many risks



# Summary of Lessons Learned

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- **Single Sided Silicon**
  - single sided microstrips are now an industrial product
  - rad-hard and high quality
- **Design and assembly**
  - Mount hybrids off silicon and, whenever possible, outside of the tracking region
- **R/O Electronics**
  - 0.25  $\mu\text{m}$  technology means lower cost and greater performance
    - better design tools for quicker design turnaround
    - cheaper and higher yield fabrication
      - **\$3k for 8" wafer with 80% yield vs \$20k for 6" wafer with 25-30% yield**
    - radiation hardness is extraordinary while noise is low
      - **APV25: 325 + 43.3 C  $\Rightarrow$  SNR ~ 18:1 for 15 cm long strips**
  - FE electronics and hybrids should be simple to manufacture and very robust
  - Electronics should begin to appear in quantity **well before** real module production starts
- **Cost & schedule Estimating:**
  - Applying these lessons, one can reliably estimate cost and schedule.



# Recent Experience

- CDF ISL Module Production

- Simple module design w/Hybrids mounted off silicon
- Construction is not difficult:
  - Assembly less than 1.5 h.
  - Wirebonding ~ 1 h.
  - Repair  $\leq$  1 h per module.

- Single-sided silicon

- An industrial product
- High quality, rad-hard
- Short lead times
  - From final specifications to delivery of all L00 silicon was ~4 months. CMS prototypes had similar experience.
- Commercial capacity:
  - HPK can start 10k wafers/month
  - ST-Catania has similar capacity

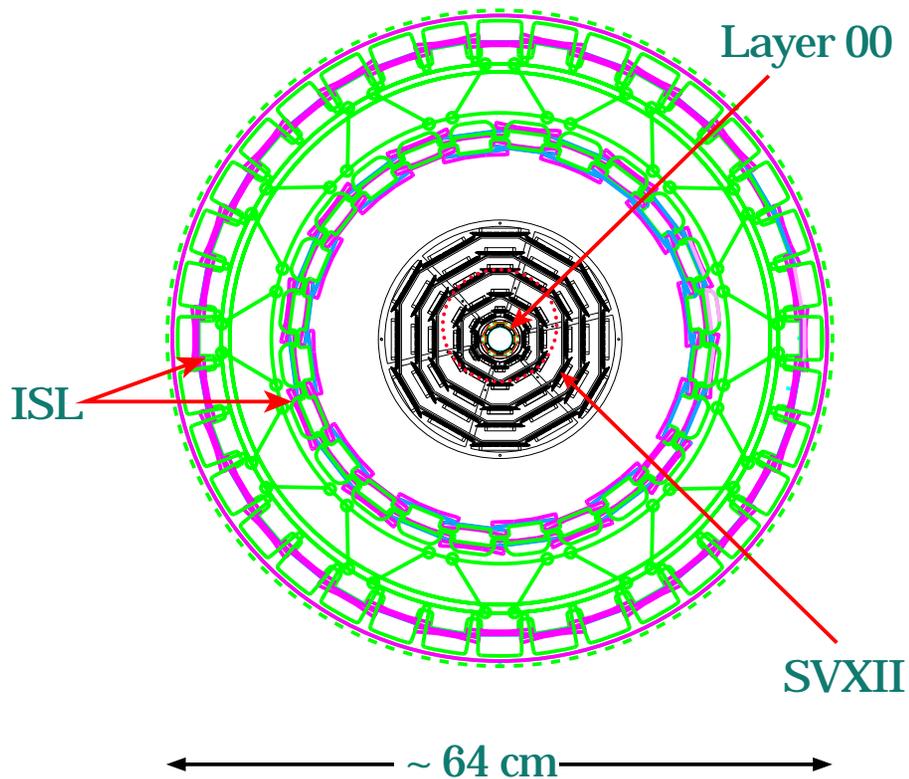
## Rad-tolerant Layer 00 Silicon (HPK)

| Specifications                 | wide                       | narrow         |
|--------------------------------|----------------------------|----------------|
| # channels                     | 256                        | 128            |
| active area (cm <sup>2</sup> ) | 9.7                        | 4.8            |
| implant pitch                  | <u>25<math>\mu</math>m</u> |                |
| readout pitch                  | 50 $\mu$ m                 |                |
| implant width                  | 8 $\mu$ m                  |                |
| Test Results                   |                            |                |
| bad strips (@100 V)            | 0.10 %                     | 0.047 %        |
| depletion voltage              | $\approx$ 65 V             | $\approx$ 65 V |
| current @ 500V (nA/strip)      | 0.5-1.0 typ.               | 0.5-0.8 typ.   |

single-sided *p-in-n* silicon



# Run 2a Detector



- CDF Run 2 tracker qualities
  - Pattern Recognition
    - 7 layers are double sided
      - 4 layers have 1.2° stereo
      - 3 layers have 90° stereo
  - Full Coverage to  $|\eta| \sim 1.9$
  - Impact Parameter Resolution

$$\sigma_{xy} \sim 6 \oplus 21/p_T [\mu\text{m}]^*$$
$$\sigma_z \rightarrow 40 [\mu\text{m}]$$

CDF Tracker (Si + COT),  
is unrivaled !

We will become addicted...



# One-for-One

- Replacement of only those layers which are damaged
  - Technical Challenges: How much disassembly & re-assembly ? How much time ?
  - Required shutdown could be long and may involve some risks
    - Handling, disassembling, and rebuilding SVXII barrels carries schedule risks: requires reconstruction and testing time during the shutdown period.
      - Extract ISL and transport to SiDet
      - Remove SVXII spacetube and split it open: fair amount of fixture setup and use
      - Uncable and remove L00/beampipe: more fixture setup and use
      - Remove all 3 Barrels and transfer to barrel assembly fixtures
      - Remove ladders
        - Could possibly remove only those ladders which are damaged
        - If bulkhead alignments are affected or questionable, or if we want to survey locations of newly installed ladders then complete disassembly and re-alignment of bulkheads is required.
      - Install new ladders, survey & test
      - Reinstallation and barrel to barrel alignment in spacetube
      - Reinstallation of Layer 00 and beampipe into SVXII, surveyed and aligned, beampipe mounts installed
      - Reinstallation of SVXII into ISL, and ISL into COT, surveyed, aligned, retested



# One-for-One continued

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- What would we get ?
  - Bulkhead structure means we retain the Run 2a geometry
  - Electronics mounted on silicon would be a source of heat to silicon
    - **single-sided silicon** ⇒ lose z vertex resolution
    - **No direct silicon cooling** ⇒ could lose rad-hardness
    - **double-sided silicon** ⇒ Micron may be the only remaining manufacturer
    - **SVX3D chip does not hold up well to radiation**
  
- Whatever we install at Layer 0 would have inadequate lifetime

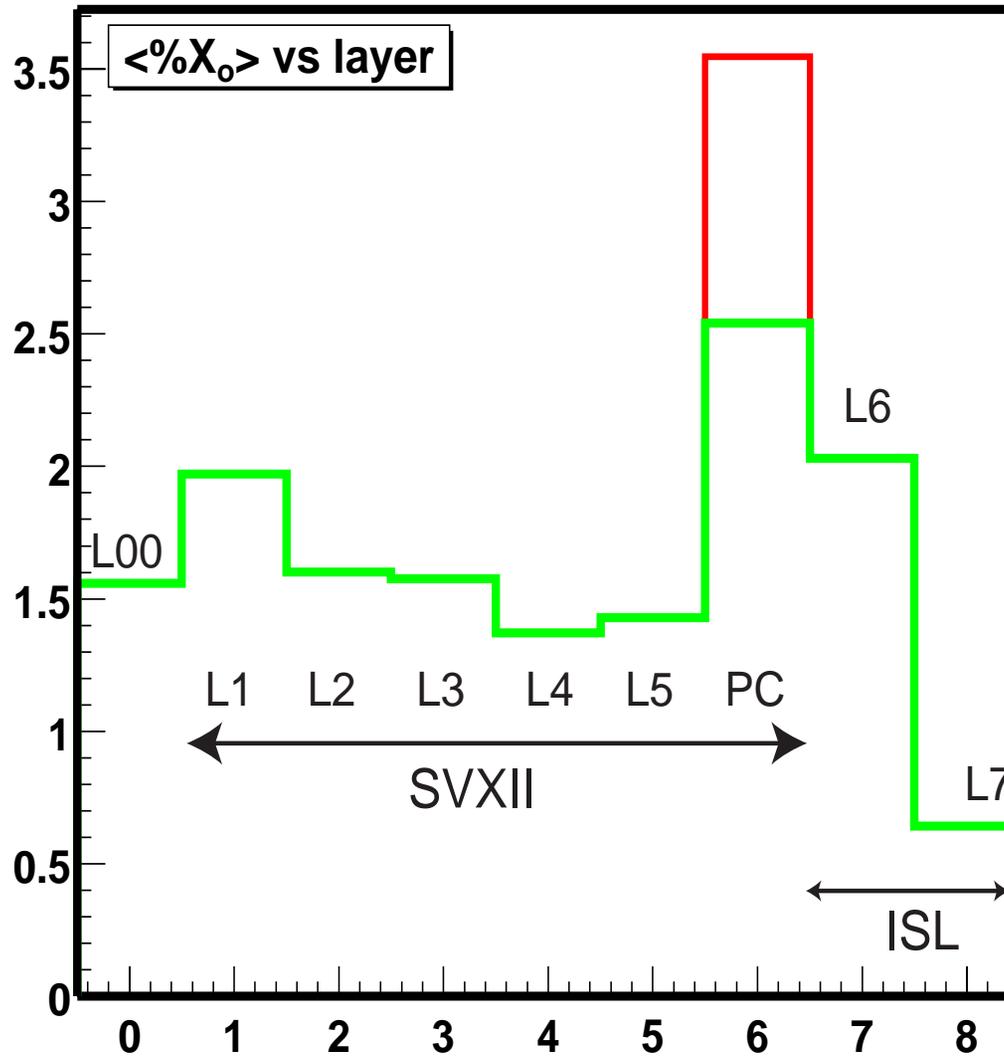


# All-for-All

- **SVXII/L00 replacement : A big undertaking but big advantages**
  - **Could be ready prior to Tevatron shutdown  $\Rightarrow$  5 - 6 months beam-to-beam**
    - Use single sided silicon  $\Rightarrow$  rad-hard at low cost with fast production & predictability
    - An inner layer could be pixels if ready on time. Build strips in any case.
    - Universal module types  $\Rightarrow$  low cost, fast production, predictability
    - Take advantage of new concepts of mechanical support and cooling
    - Design to include an inner radius section that is easy to swap out so that
      - **any future shutdowns can be minimal - as little as 5 months.**
      - **any future required replacements would be at a small scale**
      - **we could recover from a major accident or upgrade to pixels**
    - Integrate cooling with silicon (ala CMS or L00)
  - **Reduce overall material budget from  $\sim 13.5\%$  to  $\sim 10.5\% X_0$ .**
    - Some things add material
      - **2 sensors/layer adds  $0.3\% X_0$ /layer (currently we have  $\sim 1.5$ - $2.0\% X_0$ /layer in SVXII).**
      - **Integrated cooling adds small average mass (cf. L00)**
    - Other things subtract
      - **Removing portcards from the tracking region cuts material by  $\sim 3.5\% X_0$ .**
      - **Using ISL style double-sided hybrids reduces ave. material by  $\sim 0.5\% X_0$ /layer**



# Material

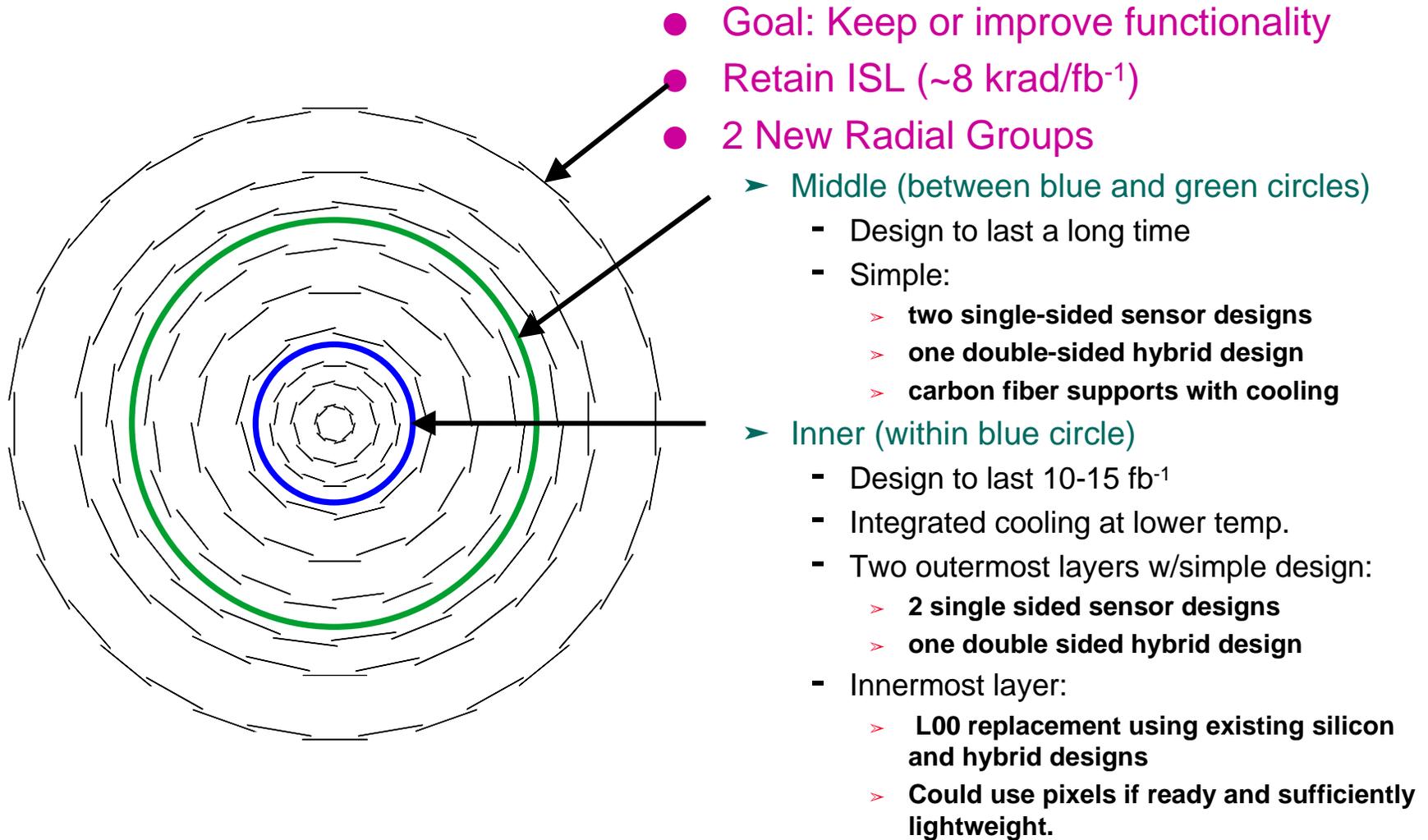


D. Stuart

CDF Note #5268



# A Full Replacement Example



- Goal: Keep or improve functionality
- Retain ISL ( $\sim 8 \text{ krad/fb}^{-1}$ )
- 2 New Radial Groups
  - Middle (between blue and green circles)
    - Design to last a long time
    - Simple:
      - two single-sided sensor designs
      - one double-sided hybrid design
      - carbon fiber supports with cooling
  - Inner (within blue circle)
    - Design to last 10-15  $\text{fb}^{-1}$
    - Integrated cooling at lower temp.
    - Two outermost layers w/simple design:
      - 2 single sided sensor designs
      - one double sided hybrid design
    - Innermost layer:
      - L00 replacement using existing silicon and hybrid designs
      - Could use pixels if ready and sufficiently lightweight.



# Detailed Example

| Layer | R [cm] | Nphi | chips | pitch  | hybrid pitch | width  | total chips | cumulative | phi coverage |
|-------|--------|------|-------|--------|--------------|--------|-------------|------------|--------------|
| L0A-1 | 1.35   | 6    | 1     | 0.0025 | 0.005        | 0.84   | 36          | 36         | 59%          |
| L0A-2 | 1.65   | 6    | 2     | 0.0025 | 0.005        | 1.48   | 72          | 108        | 86%          |
| L1A   | 3.5    | 12   | 2     | 0.0035 | 0.007        | 1.992  | 144         | 252        | 109%         |
| L1S   | 3.5    | 12   | 2     | ?      | 0.007        | 1.992  | 144         | 396        | 109%         |
| L2A   | 5.25   | 18   | 2     | 0.0035 | 0.007        | 1.992  | 216         | 612        | 109%         |
| L2S   | 5.25   | 18   | 2     | ?      | 0.007        | 1.992  | 216         | 828        | 109%         |
| L3A   | 8      | 12   | 4     | 0.0028 | 0.0084       | 4.5008 | 288         | 1116       | 107%         |
| L3S   | 8      | 12   | 3     | ?      | 0.0112       | 4.5008 | 216         | 1332       | 107%         |
| L4A   | 12     | 18   | 4     | 0.0028 | 0.0084       | 4.5008 | 432         | 1764       | 107%         |
| L4S   | 12     | 18   | 3     | ?      | 0.0112       | 4.5008 | 324         | 2088       | 107%         |
| L5A   | 16     | 24   | 4     | 0.0028 | 0.0084       | 4.5008 | 576         | 2664       | 107%         |
| L5S   | 16     | 24   | 3     | ?      | 0.0112       | 4.5008 | 432         | 3096       | 107%         |

- Total installed chip count of SVXII + L00 = 3168+108 = 3276
  - Need to not exceed this in order to limit impact on DAQ
- This example has 3096 installed chips.
- Pattern Recognition (A. Yagil)
  - Our silicon system does not compromise tracking at even  $10^{33} \text{ cm}^{-2} \text{ s}^{-1}$
  - Nevertheless Pixels are attractive: improves/simplifies pattern recognition.



# Shell Support Concepts



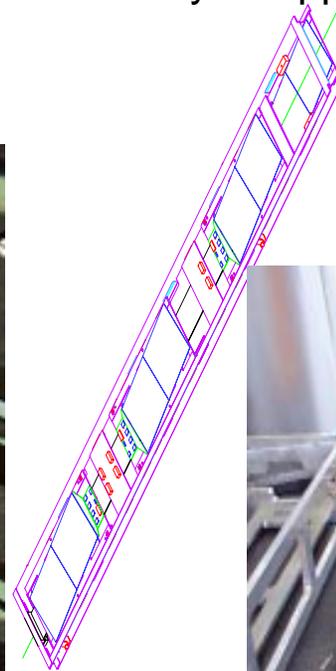
- At small radii, Carbon Fiber shells can be used to support modules
  - CMS is using molded cylinders with integrated cables and cooling
    - Modules are installed on both the exterior and interior in order to maintain z overlap
  - In Layer 00 we use molded shells with cooling tubes running under ledges
    - Silicon is installed on the flat sections and all electronics are outside the tracking region



# CMS Rod Support Concept



Uses only stereo modules made up of two single-sided modules. These are installed back to back with small overlap in z in boxlike “rod”. Rods install in C-fiber endplate system like COT field sheets. CMS achieves very high precision alignments from one rod to next. They are also easily swapped in and out.





# Practical Considerations

- **SVX4 deep sub-micron (1.1M\$):**
  - Estimate for all development and production
    - 2-3 engineers ( ~2 FTE ) for ~ 2 y
    - Need to start soon !
  - The alternative is ~2.5 M\$ for Honeywell production of SVX3 chips
- **New Portcards and Cables (? M\$)**
- **Extra Be beampipe (0.25 M\$)**
- **Silicon (< 1.5 M\$)**
  - Many manufacturers for rad-hard single sided microstrips.
  - Oxygenation.
  - Have asked for rough quotations.
    - Production time would be short and predictable
    - Quality would be exceptional
      - **99.9% good strips**
      - **$V_{BD} \geq 700V$**
- **Module production (~0.75M\$)**
  - Use all single-sided equivalent modules
    - Stacked for stereo views
  - 1152 single sided equiv. (SS) modules
  - Production requirements are modest. Based on ISL experience:
    - **2 technicians could fabricate, and 1-2 technicians could inspect, wirebond and repair 6 SS modules per day on one CMM (includes contingency)**
    - **6-7 technicians could complete all modules in 26 weeks**
- **576 Hybrids (~0.7M\$)**
  - Off silicon, and use adequate real-estate to make robust, simple, easy to manufacture
- **Support/Assembly (1 - 2 M\$ )**
  - Model after CMS/L00:
    - nested cylinders at small radii
    - rods at intermediate radii



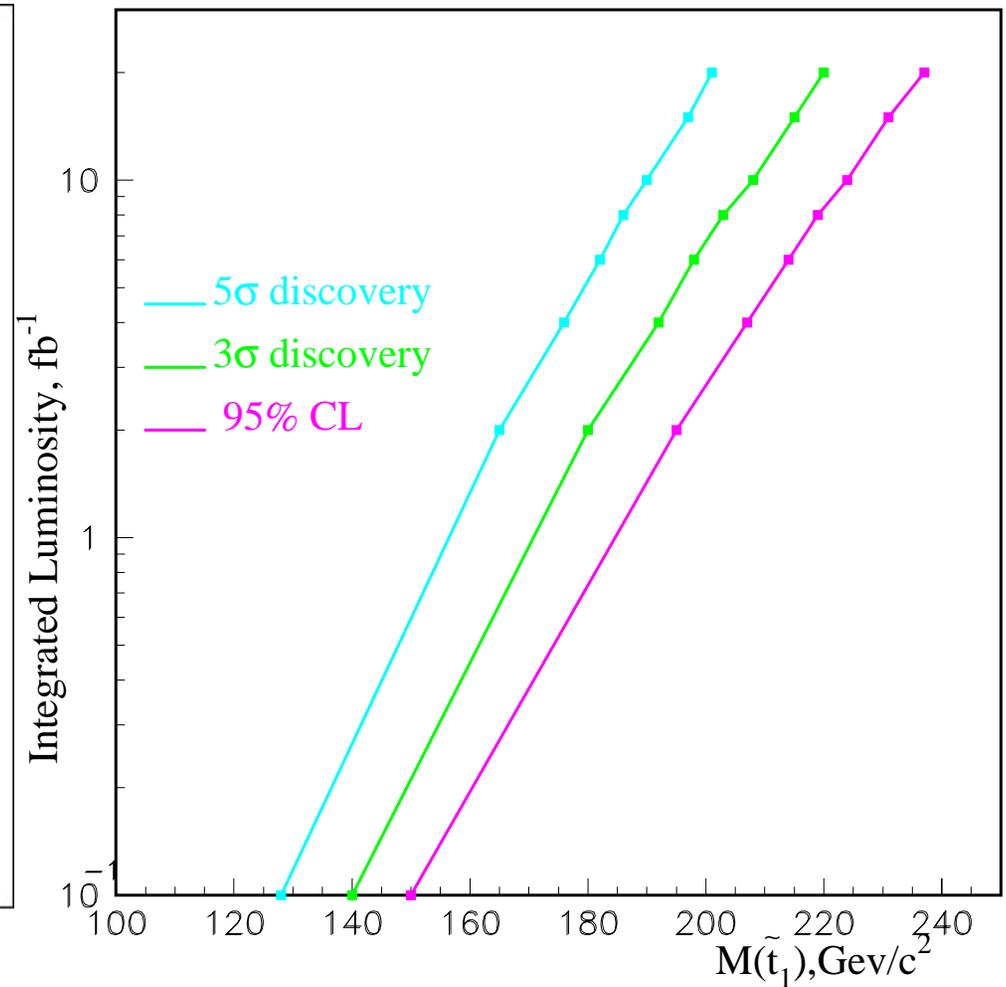
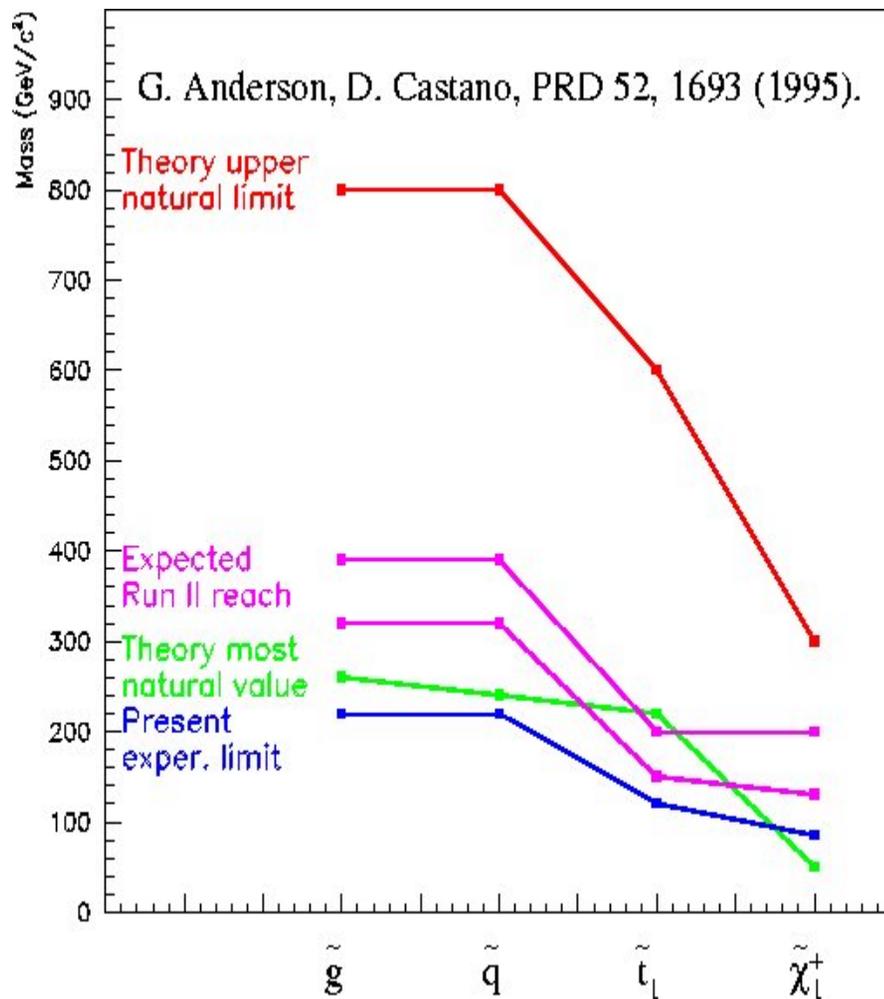
# Summary

- The physics case for much more luminosity is strong.
- Replacing only radiation-damaged layers would not get us there.
  - Could cost as much time as it buys
  - More detailed studies are in progress
- A full-replacement is **NOT** a repeat of the Run 2a silicon project.
  - It can very likely be achieved at reasonable cost and low technical risk
    - does not require an all-new DAQ
    - better performance
    - minimize lost running time
    - provide a simpler replacement path for continued running or to pixels
- We plan to complete our studies  $\Rightarrow$  a proposal this summer.
- But we need to work on a sub-micron SVX4 chip
  - This need is independent of the replacement scenario we will choose
  - If we start now, we'll be able to avoid the main risk of delay.
- **SECOND WORKSHOP WILL BE HELD JUNE 14 AT FNAL**



# SUSY

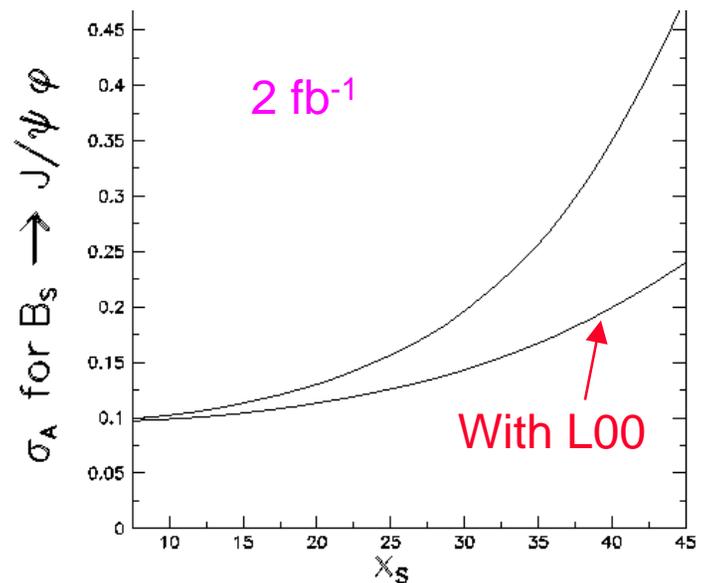
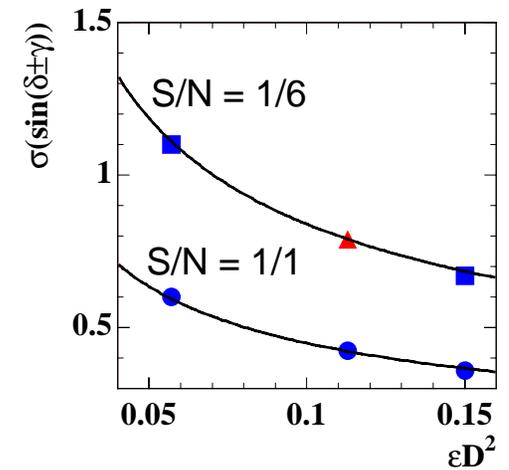
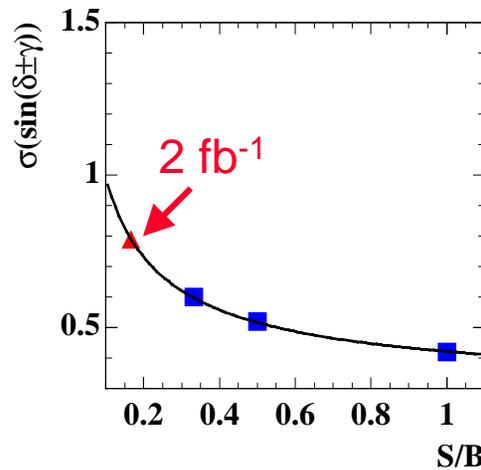
Tevatron Reach for Supersymmetric Top





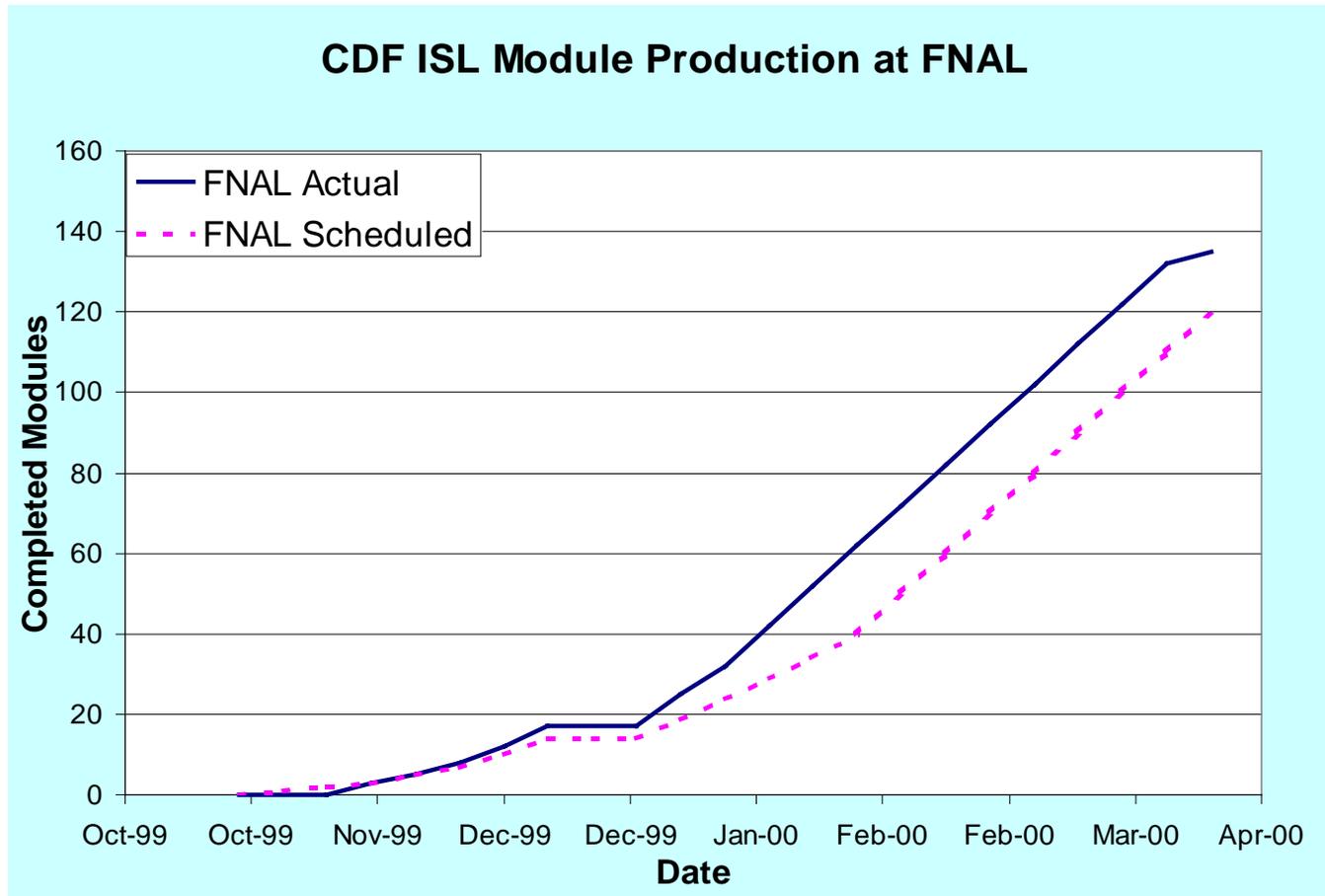
# B Physics

- $\gamma$  measurement with  $B_s \rightarrow D_s K^+$
- CP asymmetries in  $B_0 \rightarrow \pi^+ \pi^-, K^+ K^-$  (Related to  $\alpha, \gamma$ )
- CP asymmetries in  $B_s \rightarrow J/\psi \phi$
- $\Delta\Gamma(B_s)$
- Rare penguins  $B_0/B_s \rightarrow \mu^+ \mu^- K^*/\phi$
- Rare radiative decays  $B_s \rightarrow K^*/\phi \gamma$
- $B_c$  and b-baryon spectroscopy



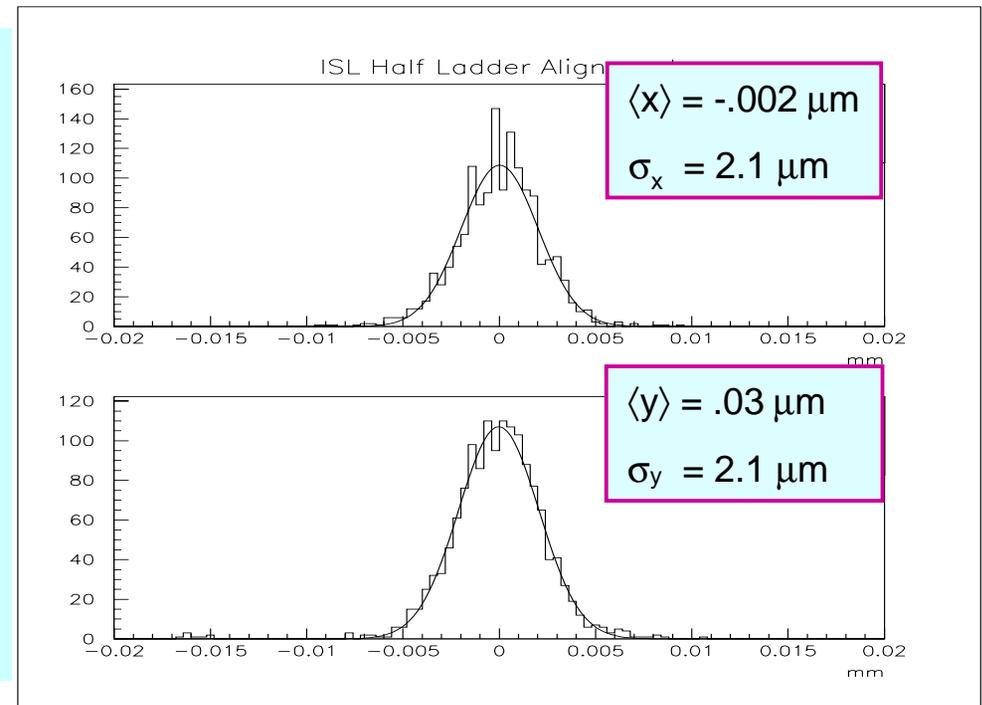
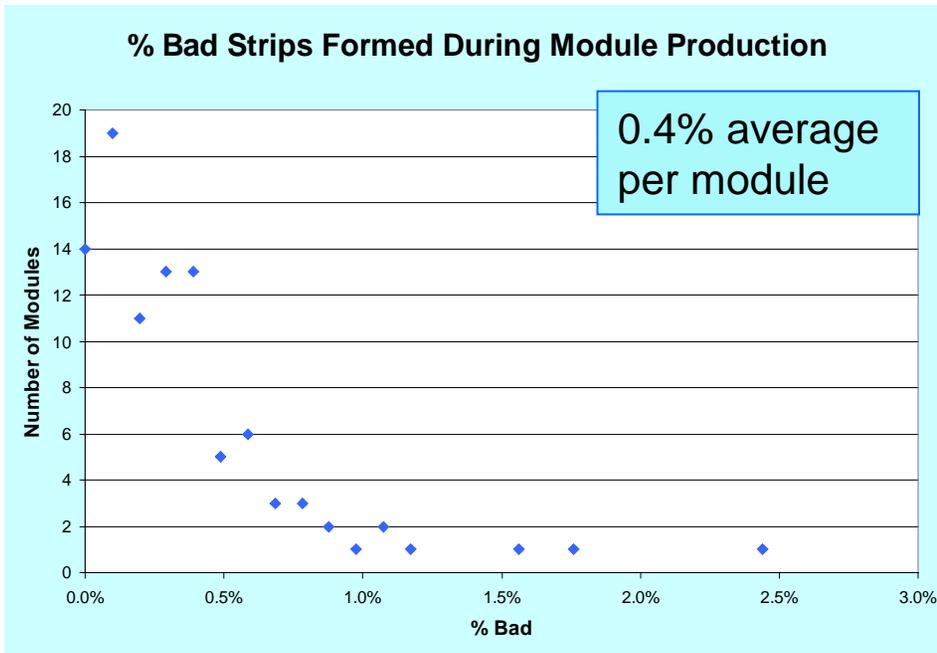


# ISL Production at FNAL





# Low damage & good quality



- Very low damage - 0.4% bad strips formed during construction and testing
- Very good quality
  - 96% all ladders produced were grade A (would have been 98% if not for a bonder glitch)
  - Alignments are good:  $\pm 2 \mu\text{m}$  for strips,  $\pm 5 \mu\text{m}$  to mounting hole,  $\pm 22 \mu\text{m}$  flatness