



# CDF in Run 2b

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*Michael Schmidt*

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*Chair, CDF Run 2b Upgrades Committee*

*For the CDF Collaboration*

*Fermilab PAC Meeting*

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# CDF Run 2b Upgrades

- Run 2b Upgrades Steering Committee

- Members:

- G.Bauer/MIT, G.Chiarelli/Pisa, F.Chlebana/FNAL, H.Frisch/Chicago, M.Lindgren/UCLA, P.Lukens/FNAL, T.Ohsugi/Hiroshima, L.Ristori/Pisa, M.Schmidt/Yale, J.Spalding/FNAL, A.Yagil/FNAL

- Charge

- Review options for silicon replacement keeping in mind the guidance from the Laboratory following Aspen PAC meeting:
  - ~2.5 million \$ with contingency
  - six month shutdown late 2003--early 2004
  - effective operation for high luminosity running up to  $15 \text{ fb}^{-1}$
- Review upgrades for non-silicon systems
  - Internal proposals due later this month



# Objectives

- Preserve and extend CDF's physics capabilities into Run 2b
  - Search for a low mass Higgs and continue the search for SUSY
  - Precision measurements of CKM elements
  - Top quark production and decay properties
  - Continued studies in QCD and electroweak physics
- Much of the program depends on the performance of the silicon tracker
  - b-tagging
  - silicon (standalone) tracking for pseudorapidity between 1 and 2
  - 3D tracking and vertex finding
  - excellent impact parameter resolution (especially in transverse plane)
  - compatibility with Silicon Vertex Trigger
- Run2 silicon designed to survive  $2 \text{ fb}^{-1}$  with high degree of confidence
  - Identify what needs to be done now to insure that CDF can go the distance



# CDF Run 2b Silicon Working Group

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*Workshops Held March-August 2000  
Full Report Submitted to PAC October 2000*



# Lifetime Calculations

- Evaluate two characteristics of each layer:
  1. Signal-to-Noise Ratio (S/N):
    - Require  $S/N > 6/1$  for L00
      - L00 is not required absolutely for pattern recognition.
    - Require  $S/N > 8/1$  for ISL and SVXII
      - Below 8/1 track efficiency drops precipitously for  $1 < |\eta| < 2$ .
      - SVT trigger efficiency is similarly sensitive to S/N in SVXII
  2. Bias voltage required for full depletion ( $V_{dep}$ ).
    - When  $V_{dep}$  greater than the bias voltage that can be applied, the  $r$ - $\phi$  strip information will be lost.
- Prescription:
  - For each layer, estimate the uncertainties quantitatively
  - Inflate uncertainties by a safety factor (1.5)
  - Adjust quantities by these uncertainties to obtain "safe" lifetimes
- Safe lifetimes are the maximum integrated luminosities that can be reached with reasonably good probability.
- No guarantee that the safe lifetimes will be exceeded.



# Lifetime Calculations (detail)

- Use Run 1 and test beam Data together with theoretical models of radiation damage effects to make predictions for Run 2:
  - Sensor Radiation damage: mainly nuclear reactions in the bulk
    - Leads to both higher leakage current ( $I_L$ ) and changes in dopant concentration which affect the depletion voltage
  - Run 1 data: direct normalization of  $I_L$  vs integrated luminosity.
    - Use this to extract fluences
  - Combine with theoretical model to predict Run 2 sensor depletion voltages and leakage currents vs integrated luminosity
  - Chip damage: mainly surface damage:
    - Combine Run 1 ionizing dose data with test beam studies on SVX3D
    - Determine shot noise vs integrated luminosity



# Uncertainties (detail)

- Uncertainties which can be bracketed systematically:
  - Damage coefficient  $\alpha$
  - Temperature variations and radial dependence of dose
  - Variation of dose in  $\phi$ 
    - Run 1 data obtained for ladders farthest from the plane of accelerator.
    - Radiation monitors indicate 10% higher dose in the plane of the accelerator
- Intangibles:
  - Temperature cycles: even brief warm-ups increase rad-damage
  - Radiation: Many things changed and are hard to predict
    - More material & calorimeter hermeticity means more secondaries & neutrons
    - Higher luminosity means more beam-gas and halo backgrounds.
- Safety Factor
  - Use a safety factor of 1.5 (as used by LHC experiments) to inflate uncertainties and thereby diminish lifetimes to reasonable "safe" limits.



# Longevity by Layer

Layer	$R_{\min}$ [cm]	Safe Lifetime [fb <sup>-1</sup> ]	Cause of Death
L00	1.35	7.4	$V_{\text{dep}}$
L0 SVX-II	2.54	4.3 (5.6)	S/N ( $V_{\text{dep}}$ )
L1 SVX-II	4.12	8.5 (10.9)	S/N ( $V_{\text{dep}}$ )
L2 SVX-II	6.52	10.7#	$V_{\text{dep}}$
L3 SVX-II	8.22	23 (30)	S/N ( $V_{\text{dep}}$ )
L4 SVX-II	10.1	14#	$V_{\text{dep}}$
L6 ISL Central	20.0	> 40	N/A
L7 ISL Forward	22.0	> 40	N/A
L8 ISL Forward	28.0	> 40	N/A
SVX port-cards	14.1	5.7	DOIM*
ISL/L00 port-cards	27.3	14.6	DOIM*

\* DOIM = Dense Optical Interface Module, located on port-card

# Assumes biasing possible after type inversion (NOT clear!)

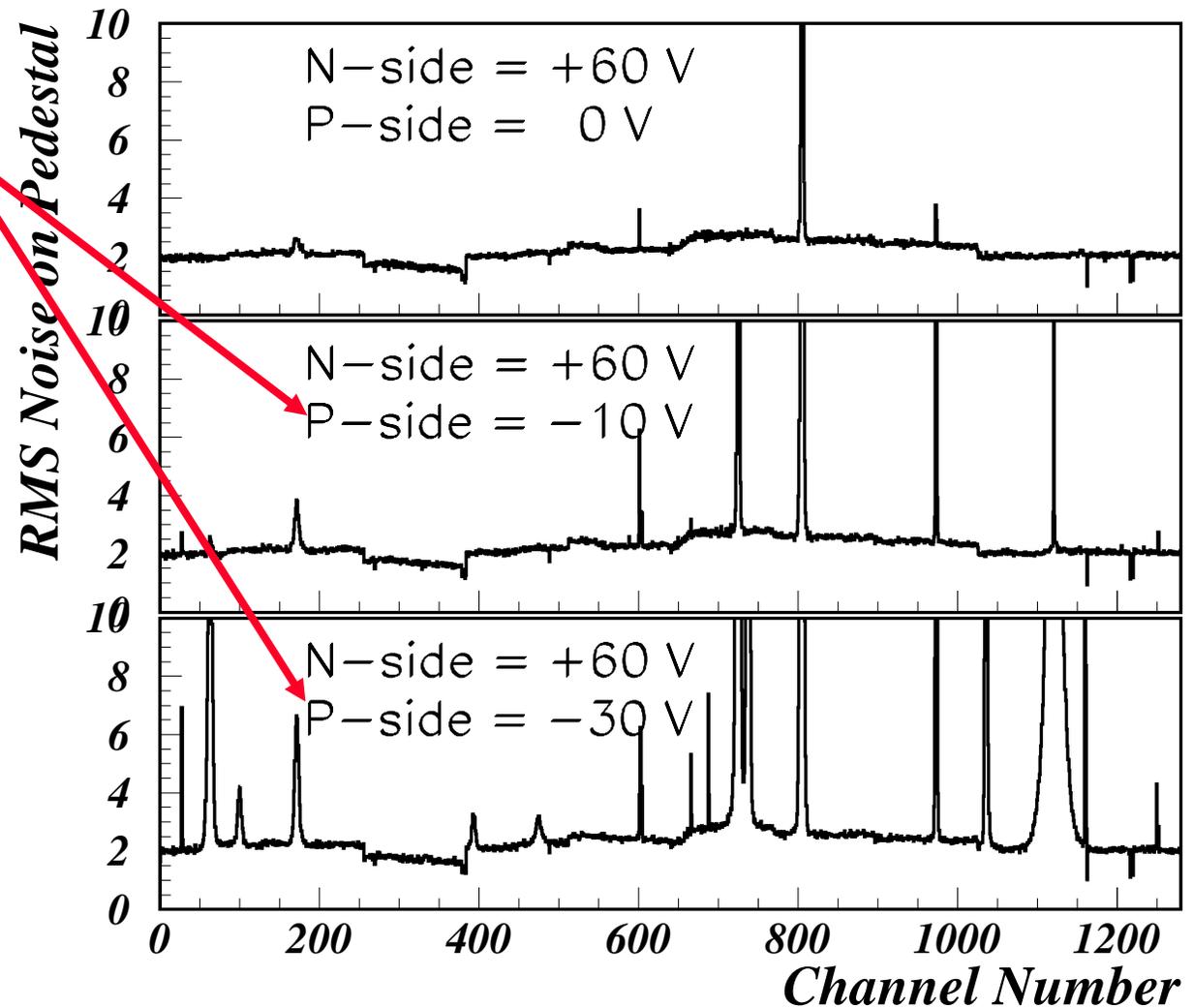


# SVX-II: L2 and L4 (details)

We can't apply much bias to the p-side of Micron silicon without generating a lot of noisy strips.

When this silicon type-inverts, there's a chance it can no longer be biased. *We have not assumed this worst-case condition in our lifetime estimates.*

After inversion, it will not be possible to deplete it for as long as we had hoped.





# PAC Questions for CDF

- What are the relative merits and implications of the following strategies ?
  - A. Replace only Layer 00
  - B. Replace Layer 00 and only the inner 1 or 2 layers of SVXII
  - C. Complete rebuild of Layer 00 and SVXII
- Working Group (WG) short answer:
  - A. Reasonable only *if* Layer 00 and the inner most layer of SVXII (L0) are the *only* layers unable to survive Run 2b
  - B. Some serious problems:
    - L00 and the 1<sup>st</sup> 2<sup>nd</sup> 3<sup>rd</sup> and 5<sup>th</sup> layers of SVXII may all need to be replaced
    - Requires a shutdown of ~1 year (even for only one or two layer replacement)
    - A large project with many technical risks
    - Possible degradation of performance
  - C. More promising:
    - Scale of project is not that much larger than a partial SVXII project.
    - A shutdown of 6 months or less is required
    - Fewer technical risks and it is easier to retain or even improve performance.



# Just Replace SVXII ?

- Exact replacement of SVXII layers:
  - Requires double-sided (DS) silicon.
    - Micron and less experienced companies are the only vendors.
      - HPK has said they will not make DS silicon anymore
    - DS silicon is not radiation hard, so not gain much.
  - What about using single-sided (SS) silicon ?
    - 2 sensors for each 1 used before
    - At small radii need direct bulk cooling to  $\leq 5^\circ \text{C}$  & high bias voltages
  - A very significant challenge to design a double-thick silicon ladder with integrated cooling that fits into existing SVXII bulkheads. The latter are not designed to provide internal cooling.
  - Such a ladder would be more complicated than anything dealt with for Run 2a.
  - Unattractive alternative is to drop stereo and use only axial sensors



# Time Required

- Reuse of any part of the existing SVXII would require an estimated 9.5 to 14 month shutdown
  - Even if one or two layers of ladders are saved and transferred and all other layers are pre-built on new supports before the shutdown, the estimated time off the air is 9.5 to 14 months.
  - Re-use of the existing bulkheads means the required shutdown would be much longer.
  - In all cases, the shutdown period would be entirely **time-critical**:
    - Any delays that occur in rebuilding add to the time off the air.
    - There is essentially NO contingency
    - There are risks.
      - Damage to ladders during disassembly
      - Damage to port-cards and cables



# Complete Replacement Scenario

- Build a complete SVXII + Layer 00 replacement
  - Not a small project but it appears to be the most reasonable choice
- There are advantages
  - When the new system is ready, then do a complete swap.
    - The shutdown would be 6 months, maybe less.
    - All the most critical construction steps could be completed before the shutdown
  - The new system could be better as a matter of course
    - More radiation hard, providing some insurance
    - Somewhat less material, especially important at small radii
- What's required
  - **Must get started on the chips !!!**
  - Take advantage of analysis of the Run 2a projects and new radiation hard technologies and streamlined designs and construction techniques developed for CERN LHC trackers (e.g. CMS).



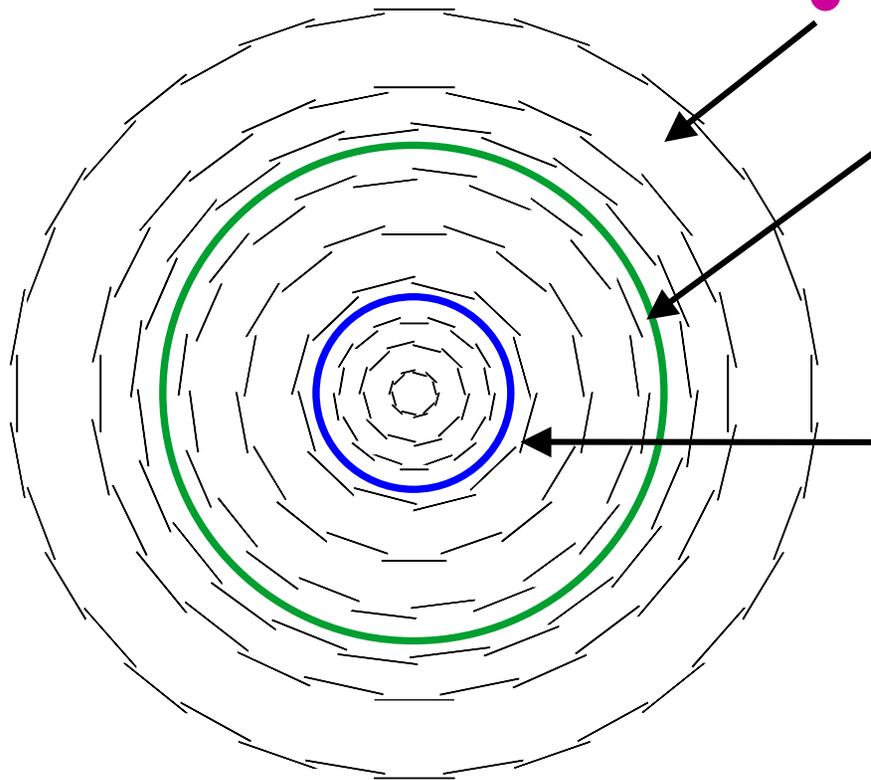
# An Example

- The Working Group developed an example of a complete replacement of SVXII and Layer 00
  - This is not a proposal for a specific layout. Some time remains for detailed studies to decide on:
    - Number of layers
    - Radii of layers
    - Strip pitches
    - Stereo angles
    - Pixels
  - The example does however identify:
    - The approximate scale for a complete replacement
    - A methodology for streamlined, low cost production
    - Components that need to be addressed very soon as a result of long development or production lead times.



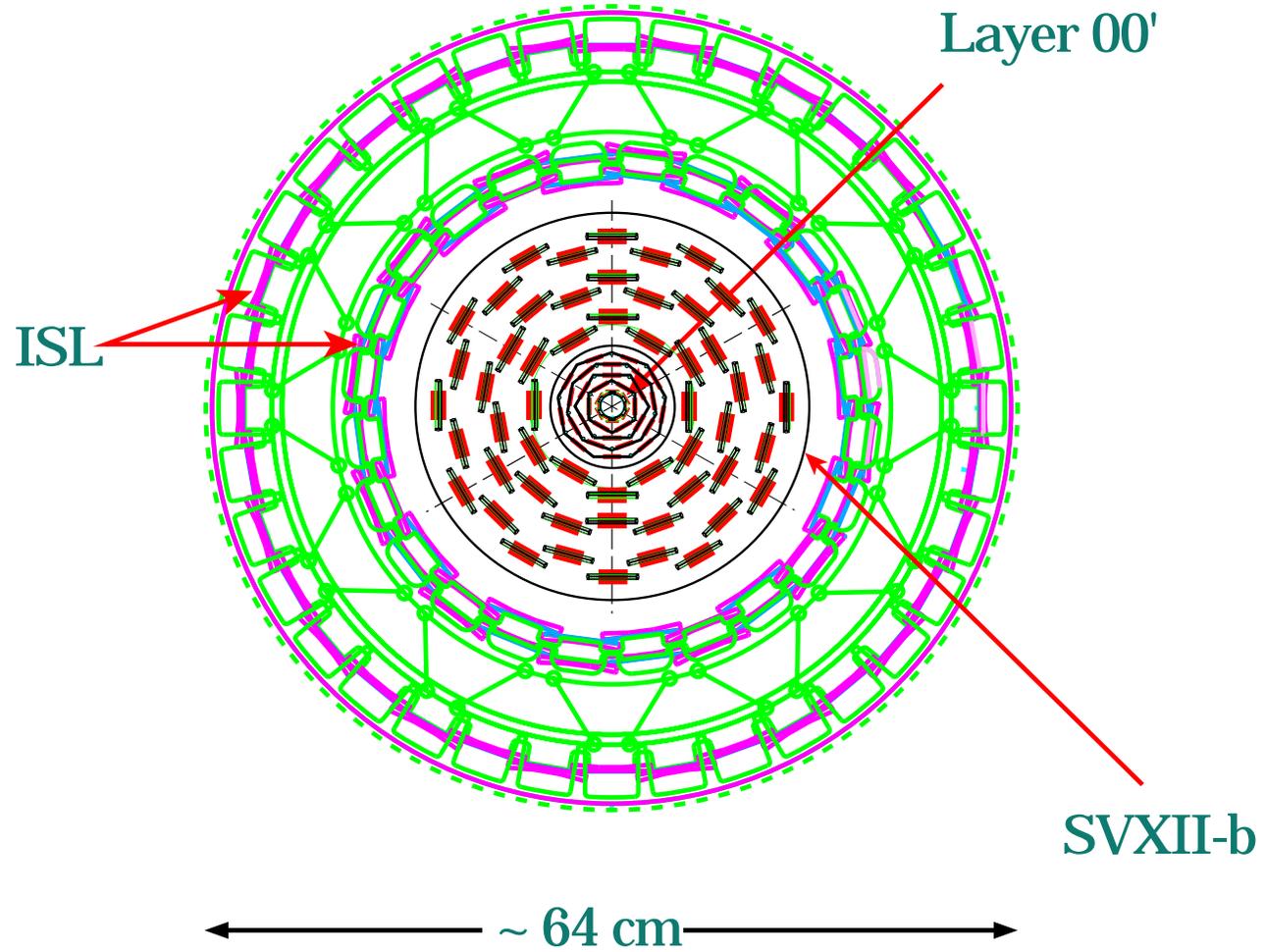
# Basic Concept

- Leave ISL as is
- 2 New Radial Groups inside ISL
  - Outer (just inside green circle)
    - Keep it simple:
      - > Only two single-sided sensor designs
      - > Only one double-sided hybrid design
      - > carbon fiber supports with cooling
  - Inner (inside blue circle)
    - Design to last minimum of  $15 \text{ fb}^{-1}$
    - Integrated cooling at lower temp.
    - Two outermost layers w/simple design:
      - > Only two single sided sensor designs
      - > L00 style hybrid design
    - Innermost layer: L00 replacement
      - > Exact replacement
      - > Pixels



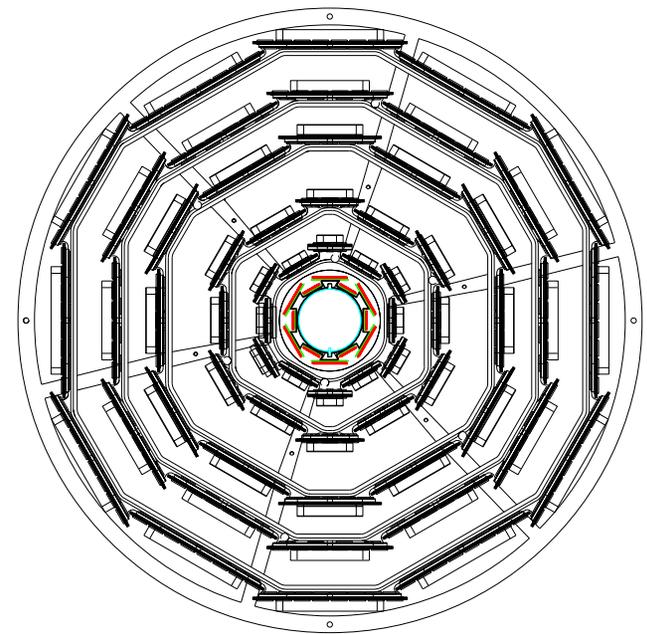
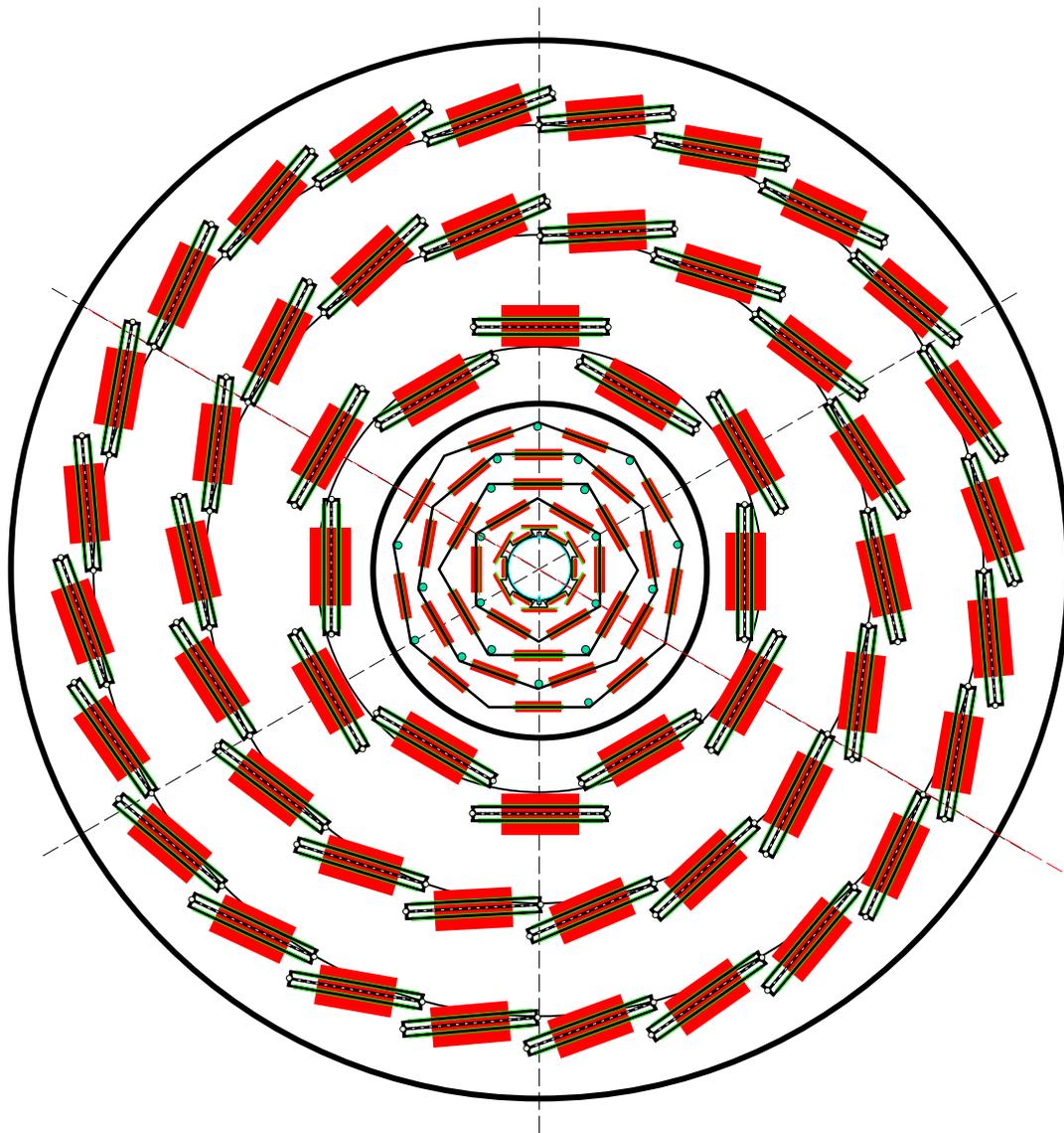


# The Example (detail)





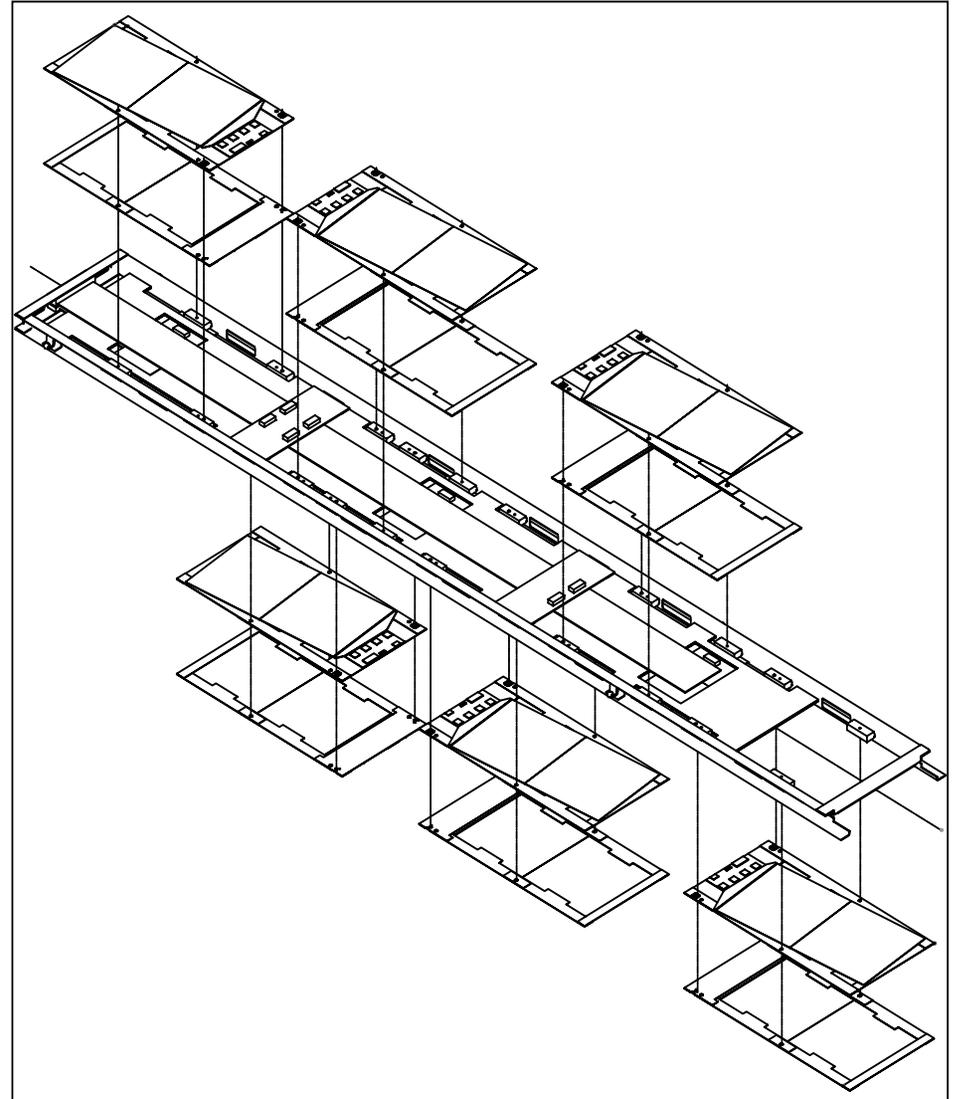
# Comparison with SVXII (detail)





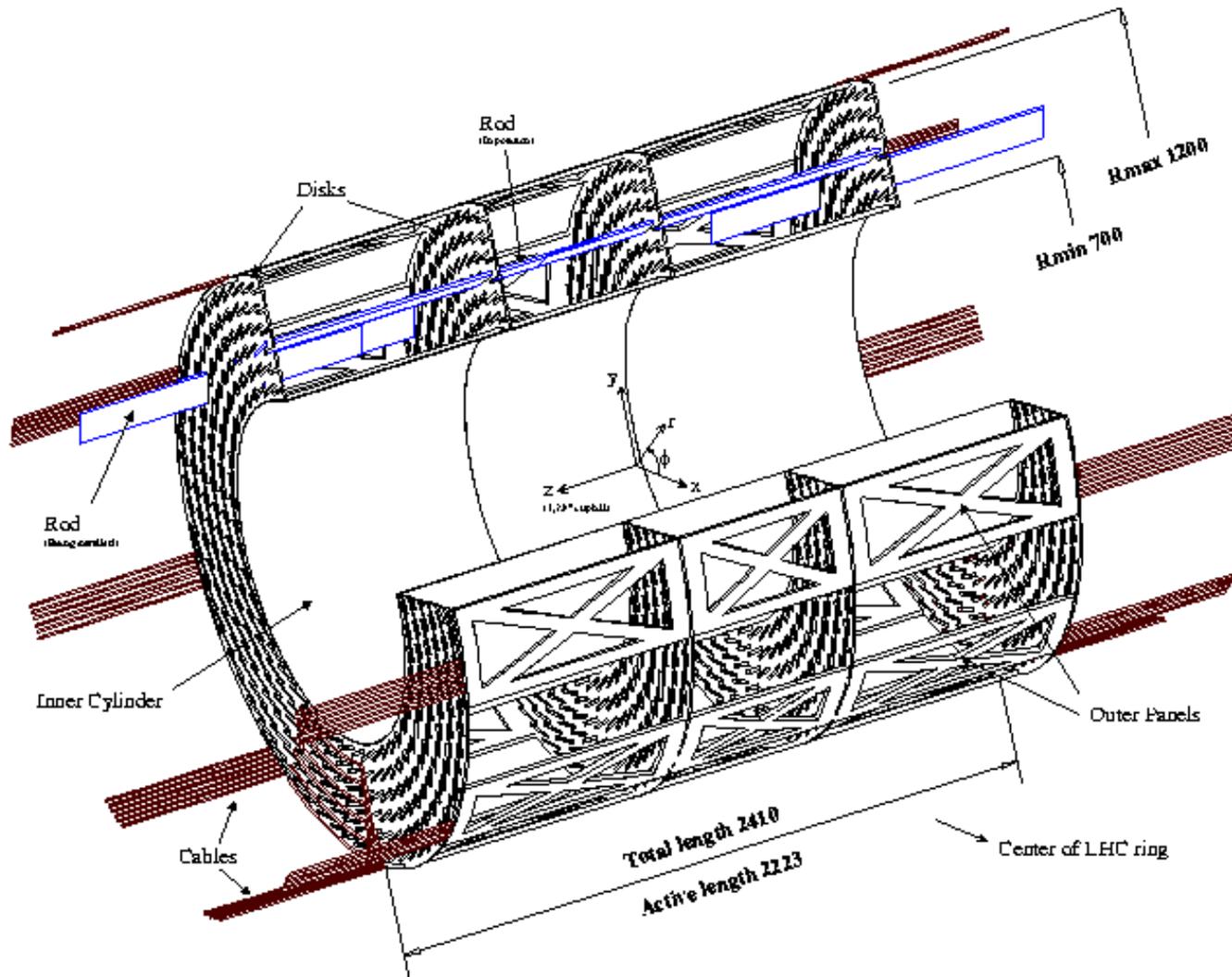
# CMS Concept (detail)

- Outer Section uses simple single-sided modules and CMS rod concept
  - Axial strip modules
  - Shallow stereo modules
- Rod
  - Integrates cooling and cables
  - Dual views obtained by stacking single sided modules
- Rods install into simple wheel supports





# CMS Wheel Support (detail)

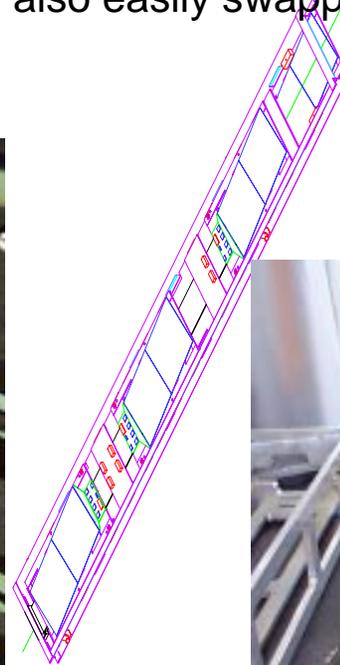




# CMS Rod Support (detail)

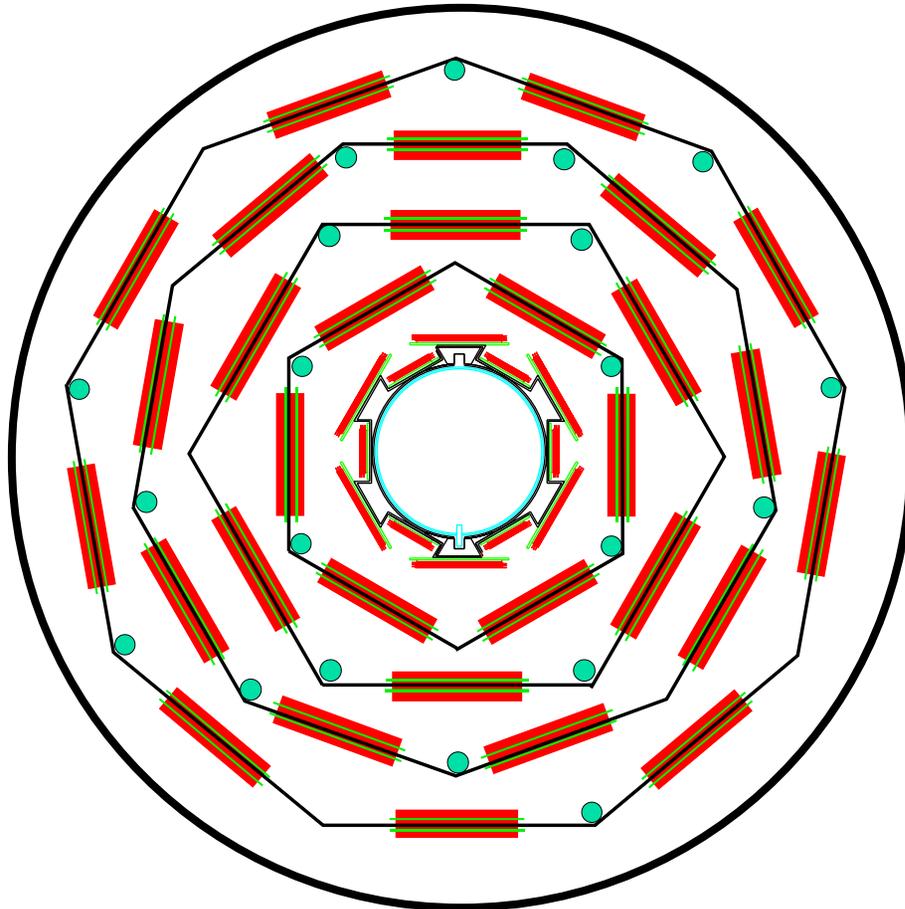


Uses only stereo modules made up of two single-sided modules. These are installed back to back with small overlap in z in boxlike “rod”. Rods install in C-fiber endplate system like COT field sheets. CMS achieves very high precision alignments from one rod to next. They are also easily swapped in and out.





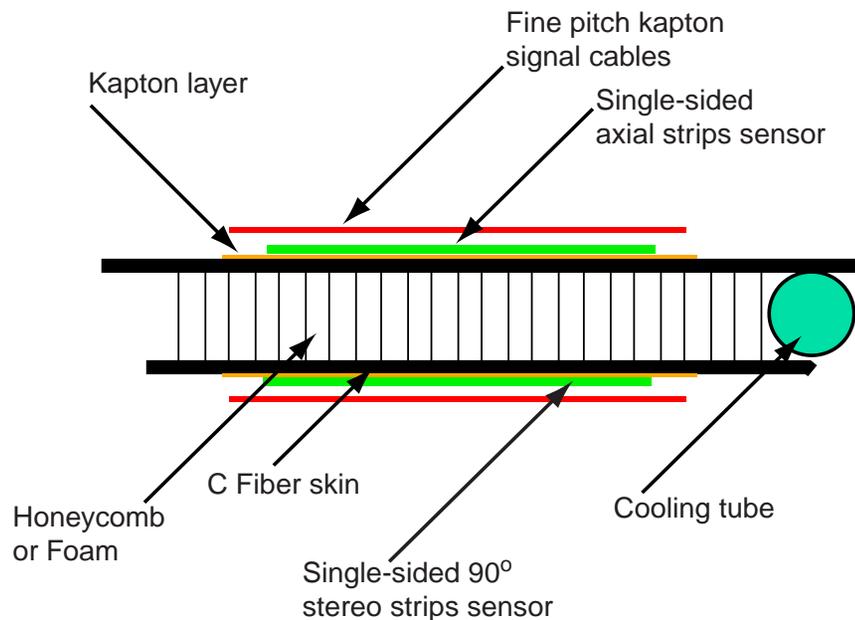
# The Example: Inner Section



- Innermost layer on beam pipe could be the same as Layer 00 or it could be pixels.
- The other two layers can be like Layer 00 with electronics outside the tracking volume:
  - Integrate cooling & support structure mechanics as in L00 and CMS. With all electronics outside the tracking volume, the cooling system inside the tracking volume is minimized.
  - Low mass inner layers for excellent impact parameter resolution and minimization of secondaries.
  - Could remove z ambiguities with fine-pitch cables.



## 2 layers outside L00 (detail)



- Build C-fiber support cylinders with polygonal cross-section
- Install single sided silicon using long kapton readout cables
  - This is similar to Layer 00
  - Traces can have larger pitch and less capacitance
- Cooling can be integrated into them directly
- Silicon can be mounted inside and outside to obtain stereo views
- Stereo can be shallow or 90°
  - Need not decide now



# Shell Support (detail)



- At small radii, Carbon Fiber shells can be used to support modules
  - CMS is using molded cylinders with integrated cables and cooling
    - Modules are installed on both the exterior and interior in order to maintain z overlap
  - In Layer 00 we use molded shells with cooling tubes running under ledges
    - Silicon is installed on the flat sections and all electronics are outside the tracking region



# The Example (details)

Layer	R [cm]	Nphi	chips	pitch	hybrid pitch	width	total chips	cumulative	phi coverage
L0A-1	1.35	6	1	0.0025	0.005	0.84	36	36	59%
L0A-2	1.65	6	2	0.0025	0.005	1.48	72	108	86%
L1A	3.5	12	2	0.0035	0.007	1.992	144	252	109%
L1S	3.5	12	2	?	0.007	1.992	144	396	109%
L2A	5.25	18	2	0.0035	0.007	1.992	216	612	109%
L2S	5.25	18	2	?	0.007	1.992	216	828	109%
L3A	8	12	4	0.0028	0.0084	4.5008	288	1116	107%
L3S	8	12	3	?	0.0112	4.5008	216	1332	107%
L4A	12	18	4	0.0028	0.0084	4.5008	432	1764	107%
L4S	12	18	3	?	0.0112	4.5008	324	2088	107%
L5A	16	24	4	0.0028	0.0084	4.5008	576	2664	107%
L5S	16	24	3	?	0.0112	4.5008	432	3096	107%

- Total installed chip count of SVXII + L00 = 3168+108 = 3276
- This example has 3096 installed chips.



# The Chips

- Presently Honeywell SVX3D
  - There are too few remaining for ANY level of rebuild
  - Honeywell Issues:
    - CDF experience with Honeywell was not so good
      - Low and inconsistent yields
      - High failure rate after dicing and on hybrids
      - Long lead times
    - Honeywell has boosted price significantly to ~30k\$ per wafer with almost no yield or schedule assurances.
- Options
  - 1. Honeywell at high cost and risk  $\Leftarrow$  WG recommends against this.
  - 2. Use an existing LHC chip (e.g. CMS APV25)
    - This requires significant changes to DAQ and cable infrastructure.
  - 3. Develop Sub-micron SVX  $\Leftarrow$  WG recommends this option.
- Great progress at Nov. 1 meeting of IC experts on Option 3

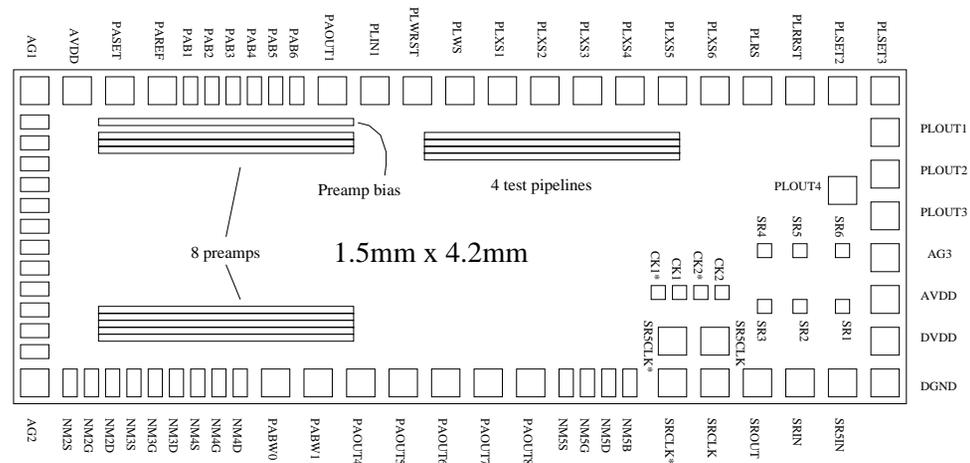


## Sub-micron Chip (detail)

- Option 3 recommended:
  - Technology has evolved: commercially available 0.25  $\mu\text{m}$  process has been studied and applied for HEP (e.g. CMS APV, FNAL FPIX)
    - Better performance (lower noise)
    - Intrinsically radiation hard with special design rules
    - Low cost, high yields, reasonable lead times
  - Two possible approaches for CDF
    1. Complete redesign using appropriate models and design rules
      - Longer lead time, chips available 2003
    2. Transform existing circuit, redo only those elements that must be redone
      - Exploratory study underway (LBL/Padova)
      - Possible submission this month (MOSIS - TSMC)
        - New pre-amp with lower noise has been included
        - Verify models and process
      - ~1 year estimated by LBNL but there is some technical risk



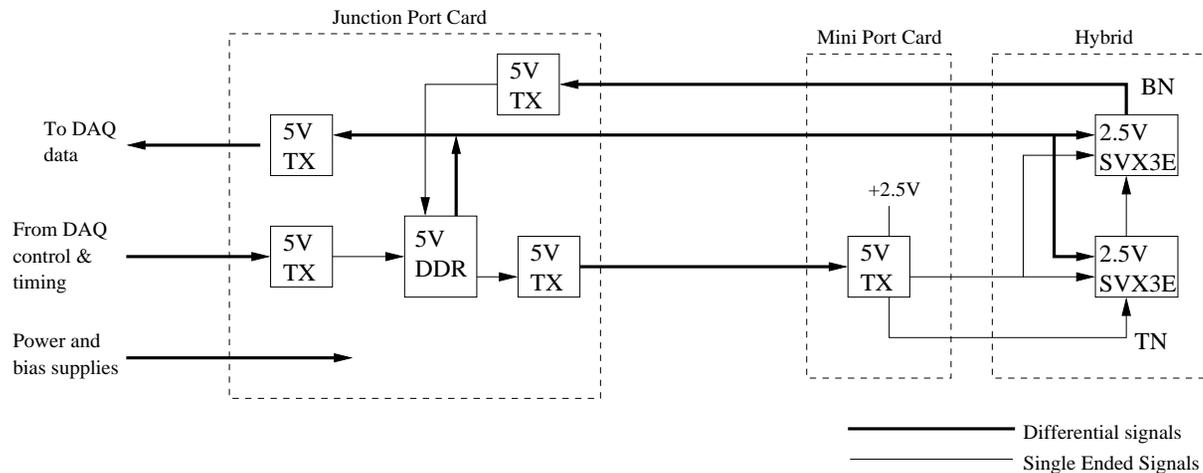
# 0.25 $\mu\text{m}$ Conversion (detail)



- Preamp layout done, pipeline and shift register layout in progress
- New manpower from Padova
- Interface scheme worked out
- Analog test chip (shown above) to MOSIS 11/25/00
  - 8 preamps with transistor variations
  - 4 pipelines
  - Enclosed transistor test structures
  - 6 cell shift register



# Interface to 2.5 V chip (detail)



- Mini-PC scheme works for both SVX3D or new 0.25  $\mu\text{m}$  chip
  - Honeywell XCVR chip differential outputs can be configured as complementary CMOS outputs
  - Differential outputs have dedicated power pin that can be connected to 2.5V



# Portcards/DAQ (detail)

- Issues for current portcard (PC)
  - Compatibility with a new chip (2.5 V levels needed)
  - PC Material in track volume
  - Voltage regulators may not survive dose
  - DOIMs may not survive dose and have to be replaced with Copper DOIMs or VCSELs
- New Mini-PC (mPC) and Junction PC (JPC) Scheme
  - XMIT/RECV scheme like ISL where PC is far from ladders
  - JPC outside tracking volume and mPC near or on the hybrid
    - Low mass cable between mPC and JPC
  - JPC uses existing Honeywell XCVR and DDR chips
    - Have enough XCVR, need DDRs
  - mPC would use existing XCVR (believed compatible with 2.5 V)



# Schedule Issues

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- Final chips needed one year before the date to install a completed system inside ISL.
  - With chips in hand by end of 2002 or early 2003 we can be ready for a shutdown somewhere in the period from late 2003 to mid 2004.
- Need to immediately begin an R&D effort and prototype
  - Module and support mechanics and cooling
  - Fine pitch cables (qualify new vendors)
  - Mini-PC scheme/address Cu DOIM issues
  - Hybrids (use existing SVX3D chips)
- Should finalize layout early in 2002.
  - Silicon ordered in early to mid-2002 with delivery by early 2003.



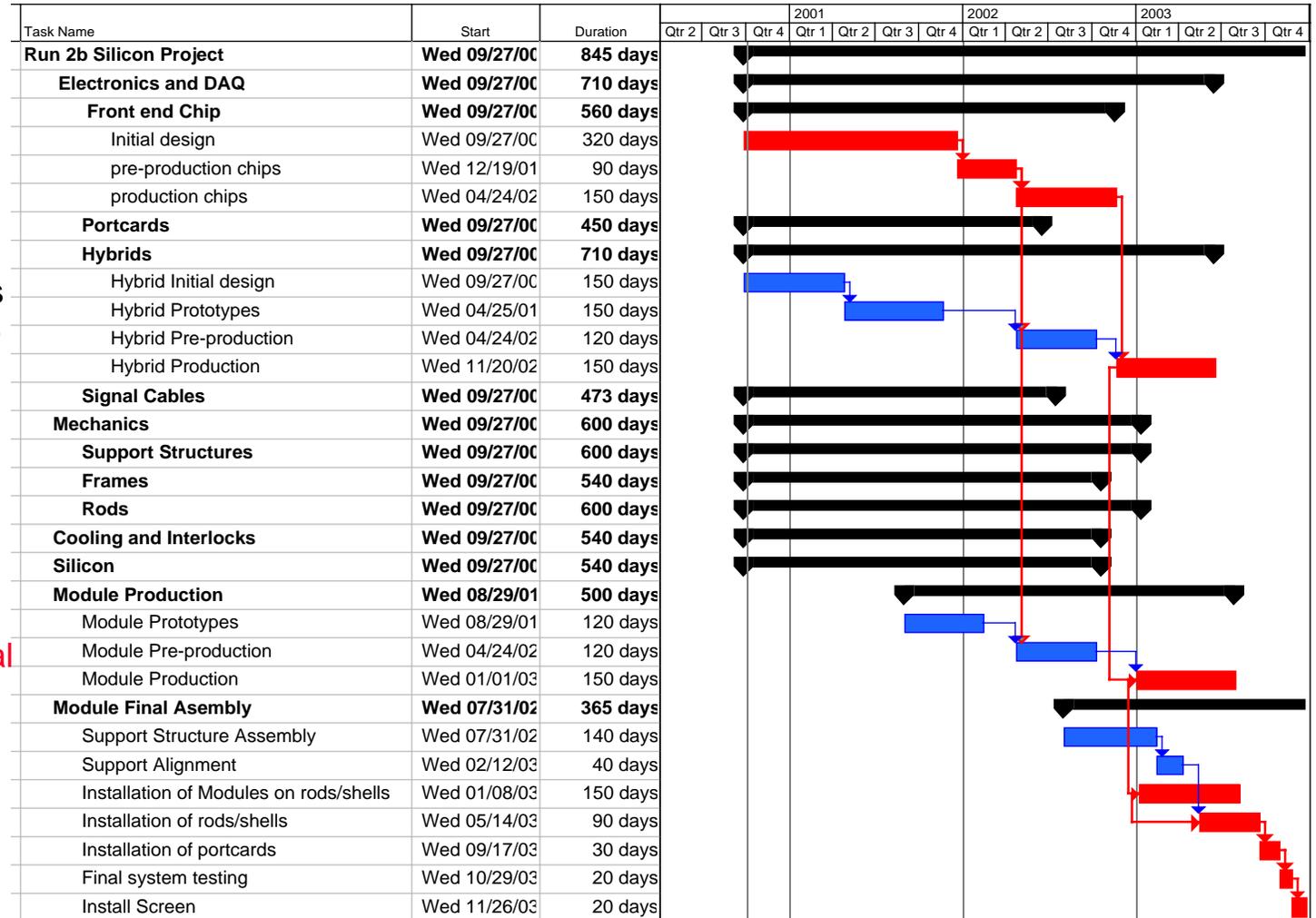
# Schedule Considerations

Chips are needed for all plausible and likely replacement scenarios.

Availability of production chips for hybrids precedes completion of system by ~ 1 year.

Production chips can be here by early 2003 or sooner if we apply resources in earnest now.

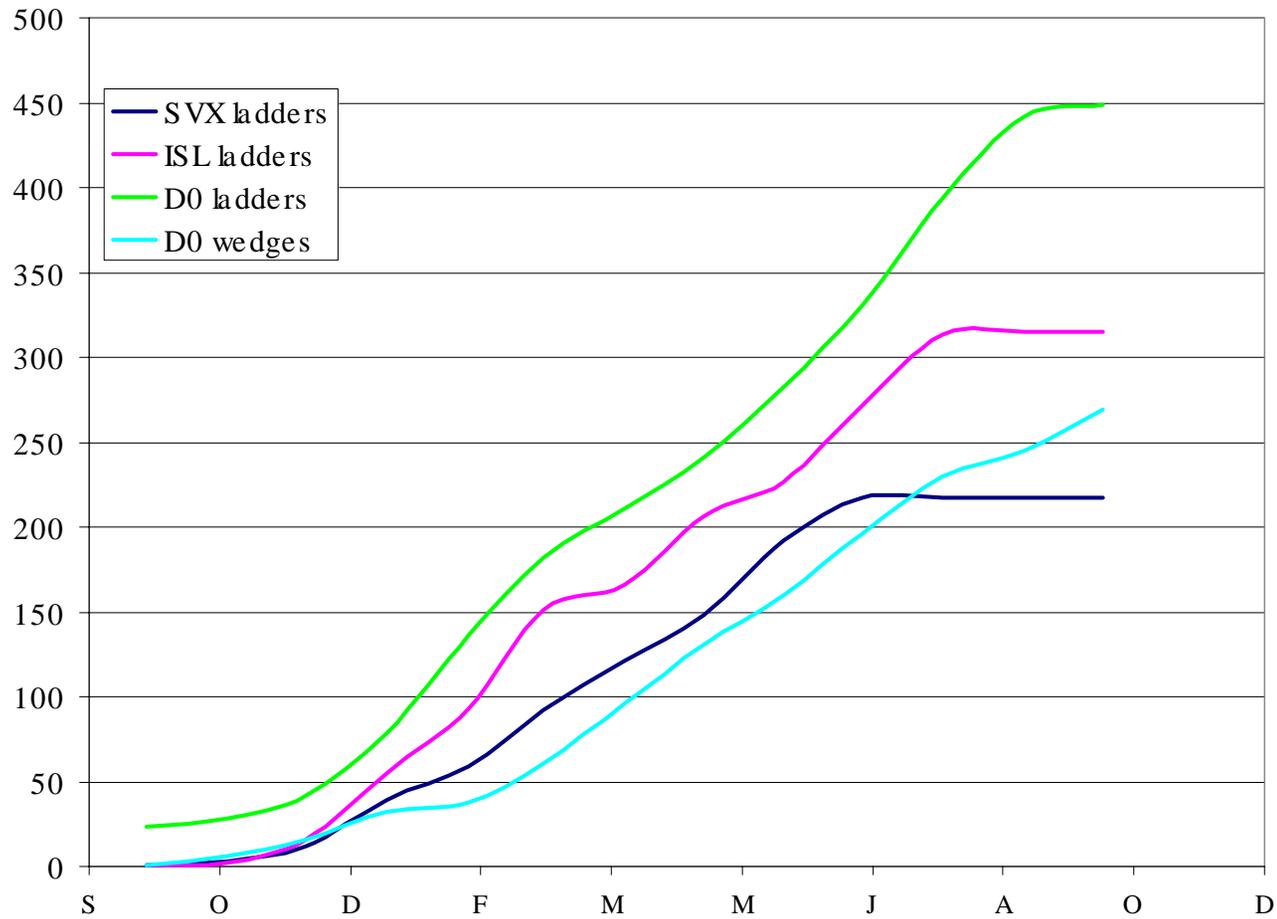
Critical path: chips → hybrids → modules → final assembly





# Run 2 Assembly Record

Cummulative Ladder and Wedge Production at SiDet





# Preliminary Cost Estimate

Item	Estimated Cost k\$	Contingency	Total Costs
0.25 $\mu\text{m}$ Chip submissions	300	150	450
Silicon	800	300	1,100
Fine-pitch Cables	200	200	400
Hybrids & Pig-tails	600	200	800
Power Supplies	200	100	300
Port cards	500	350	850
Mechanics & Cooling	400	400	800
Be beam pipe	150	50	200
Total M&S	3,150	1,750	4,900
Manpower	Estimated (FTE-years)	Contingency	Total
IC Engineers	2.5	1.5	4.0
Mech. Engineers	6.0	3.0	9.0
Module Labor	8.0	4.0	12.0
Final Assembly Labor	4.0	2.0	6.0

Table 2: Costs involved in making a full SVX-II replacement.

- Full replacement scenario:
  - mechanics and cooling needs refinement
    - FY01 R&D is critically important



# Pixel Concept

L00 Replacement:

50  $\mu\text{m}$  x 400  $\mu\text{m}$  pixels

18 x 160 pixels/chip

8 chips per module

12 modules/stave

12 ATLAS staves (in  $\phi$ )

144 modules

1152 readout chips

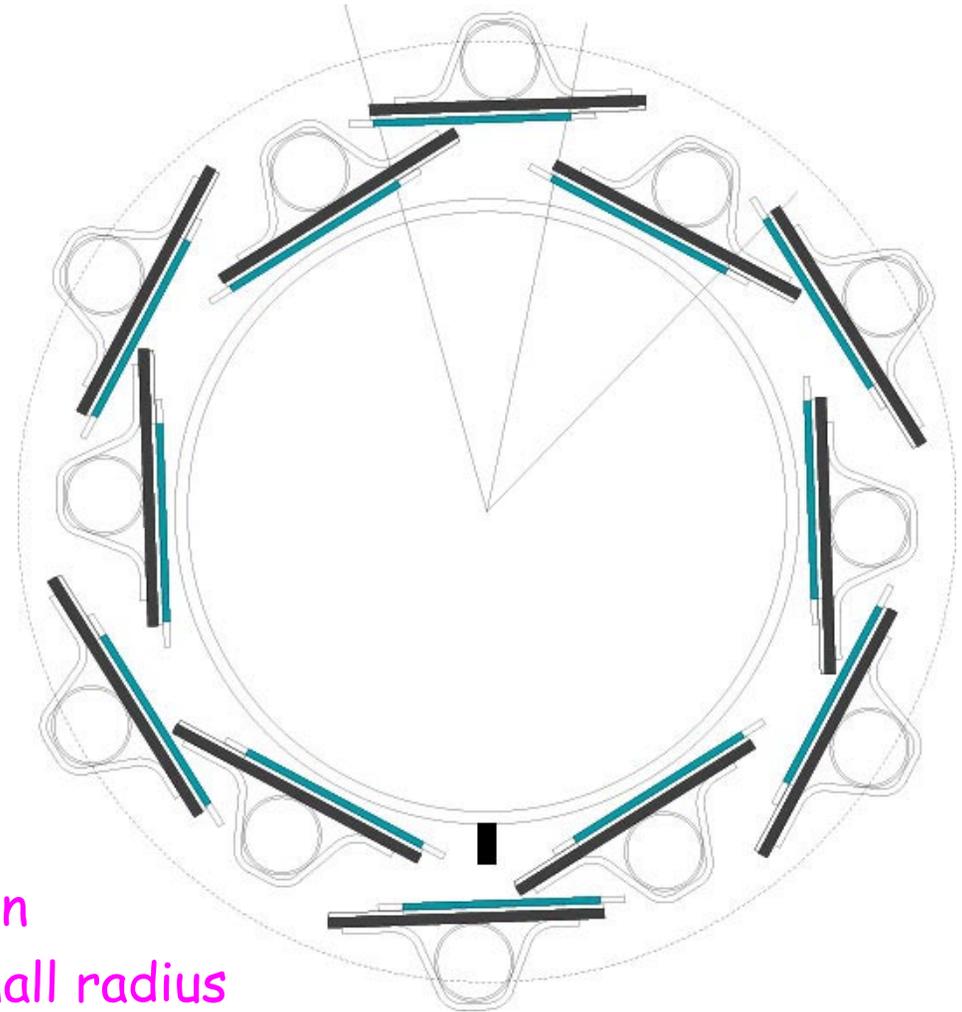
3.3 M total channels

30 Mrad survivability

S/N > 50:1, good r- $\phi$  resolution

z resolution 60 - 120  $\mu\text{m}$  at small radius

Challenge: keep material below 2.5%  $X_0$



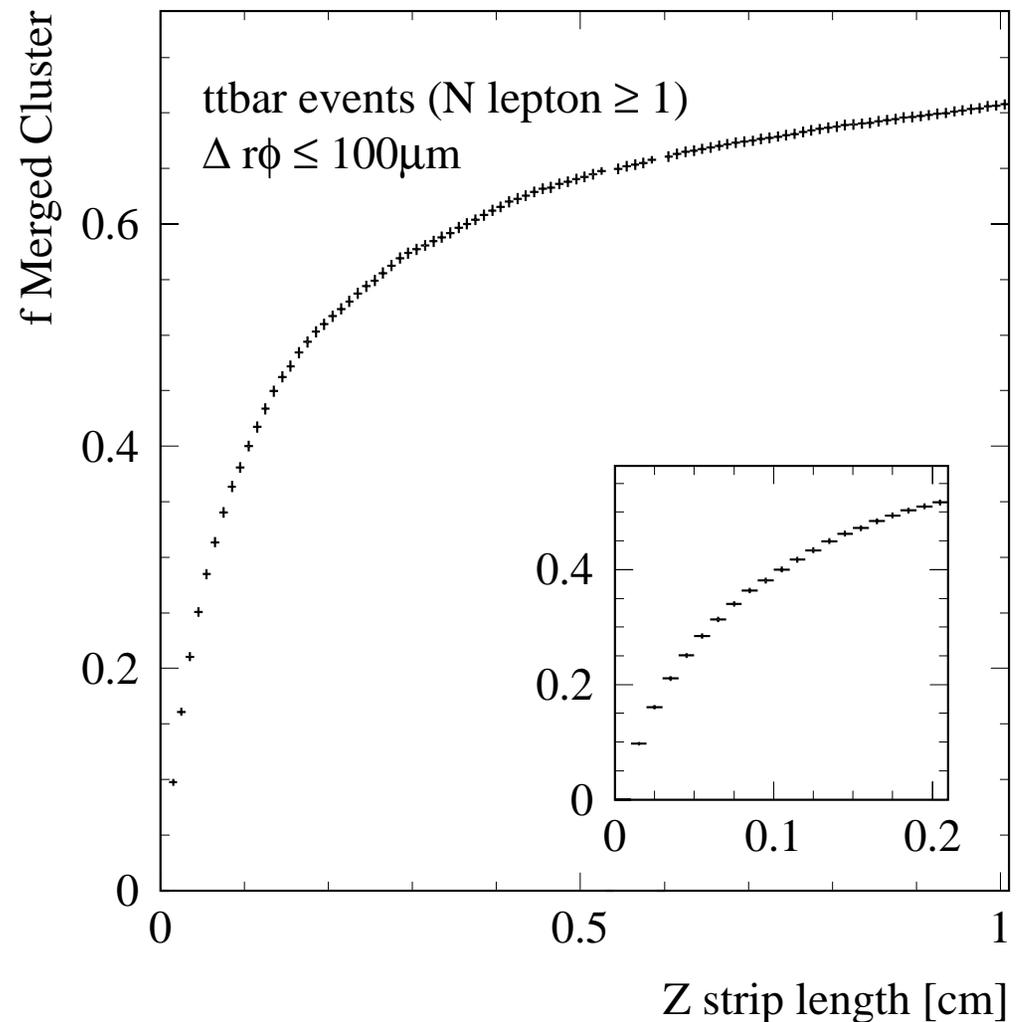


# Pixels

Pixels provide superior pattern recognition capabilities by virtue of fine segmentation in  $z$ .

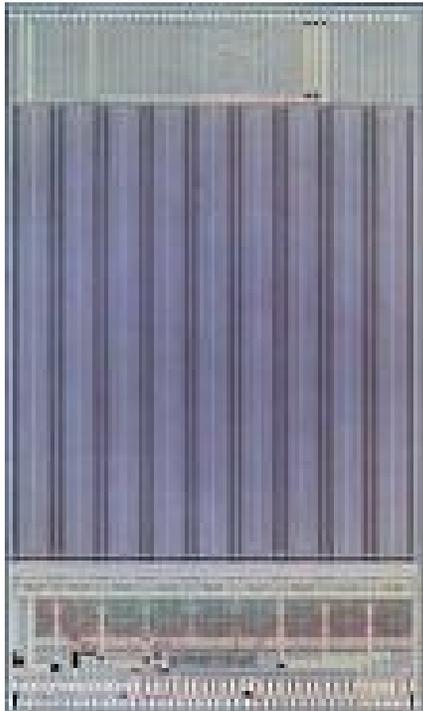
Important for resolving tracks from  $b$ 's in high  $p_T$  jets from top.

Especially attractive option if a pixel replacement for L00 could provide sufficient  $z$  information to compensate for the loss of L0 (maybe even L1?)

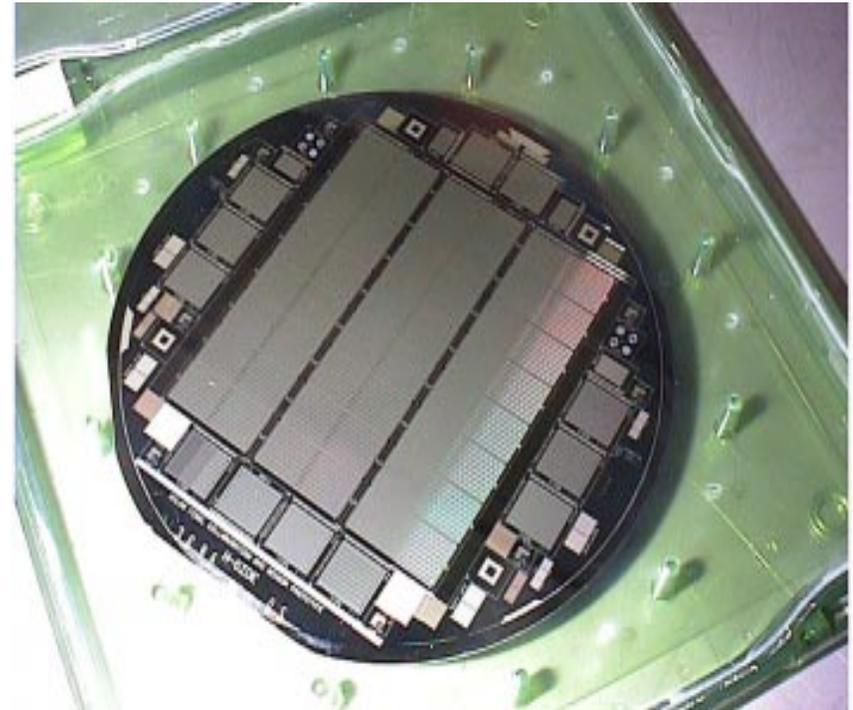




# Pixel Concept



FPIX1 chip  
Exists in 0.25  $\mu\text{m}$  and  
survives 30 Mrad  
Next version is expected to  
be the production chip



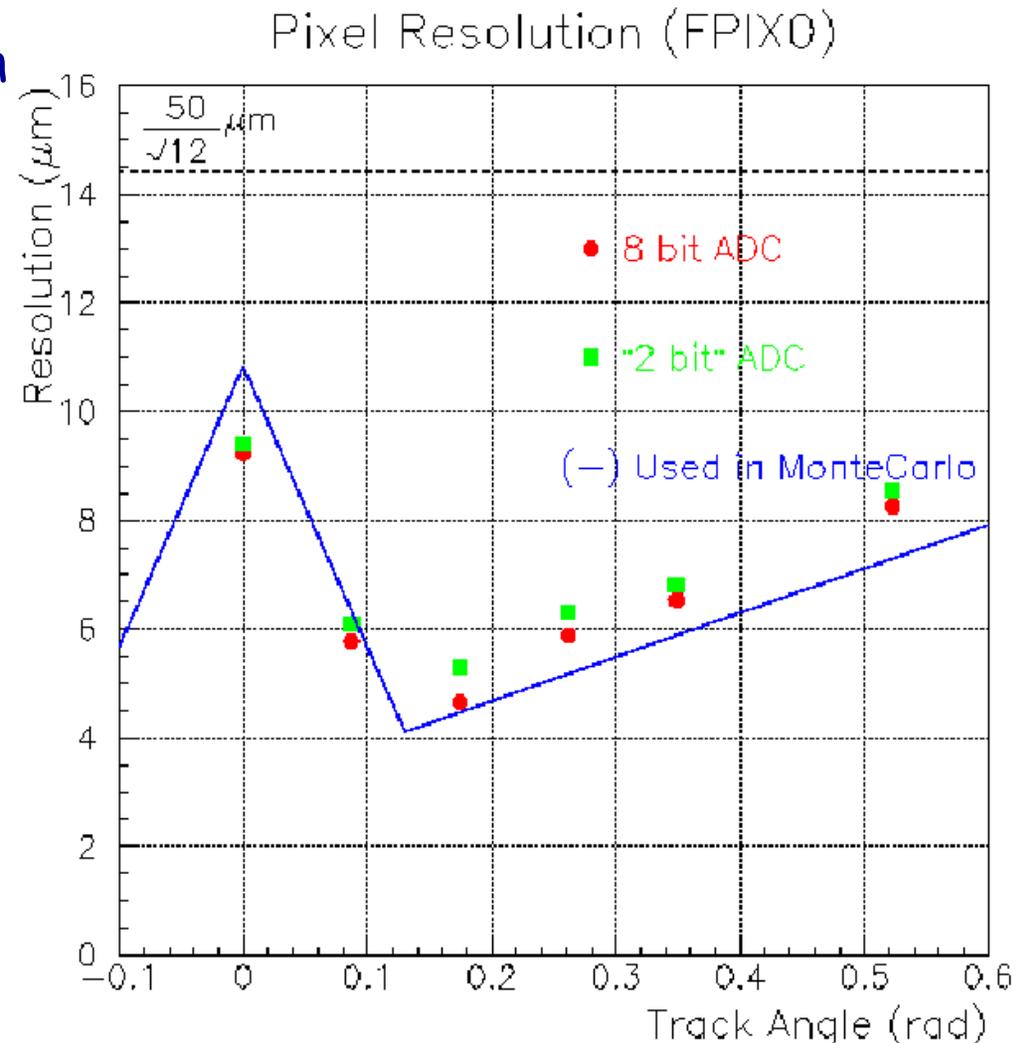
ATLAS Wafer  
Sensors in production  
Small modifications needed for  
use in CDF



# Pixels (detail)

Position resolution studies in December 1999 test beam work by Fermilab radiation hard vertex group using ATLAS style sensors and FPIX (BTeV) chips.

Precision tracking in the high radiation environment of the collider could be key for making discoveries prior to the turn on of the LHC.





# Pixel Cost and Schedule

Description	Quantity			Unit (\$K)	Units	Cost (\$K)	Cost w/ contingency
	Base	Spare	Total				
Sensors NRE	0.5		0.5	25	each	12.5	16.3
Sensors	24	26	50	1	wafers	50.0	65.0
FPIX	1152	1700	2852	0.03	chips	96.0	124.8
Bump bonding	24	14	38	2.9	wafers	110.2	165.3
Module R&D	12		12	4	modules	48.0	72.0
Modules	144	84	228	0.58	modules	132.2	198.4
HDI cables	144	84	228	0.50	cable sets	114.0	171.0
Pixel port card	24	6	30	3	boards	90.0	135.0
High voltage	24		24	3	supplies	72.0	108.0
Low voltage	24		24	2	supplies	48.0	72.0
Monitoring	1		1	20	system	20.0	30.0
Interlocks	1		1	20	system	20.0	30.0
Pixel-Fib	24	6	30	5	boards	150.0	195.0
Opto-electronics	1152	348	1500	0.03	each	45.0	67.5
DAQ cables	24	6	30	1	bundles	30.0	45.0
Staves R&D	2		2	20	each	40.0	60.0
Staves	12	3	15	3	each	45.0	67.5
Stave support	1		1	20	system	20.0	30.0
Cooling manifold	1		1	20	system	20.0	30.0
Cooling system	1		1	20	system	20.0	30.0
<b>Total</b>						<b>\$1,178</b>	<b>\$1,705</b>

Cost sharing with BTeV and D0 could cut the CDF *alone* cost in half.

2001:

Accomplish FY01 R&D items

2002:

Order sensors and readout chips

Build mechanical and DAQ prototypes

Begin module assembly

2003:

Finish module assembly and testing

Build and assemble staves

DAQ production

Final assembly and test



# Silicon Working Group Conclusions

- Lifetimes estimates for the Run 2a silicon:
  - Can not guarantee that L00, SVX-II L0,L1,L2,L4 will survive Run 2b.
    - With data ( $\sim 0.5 \text{ fb}^{-1}$ ), it will be possible to be more precise about how extensive the replacements will have to be.
    - May only need to replace L00 ... but may also need to replace most of SVX-II as well.
- Need to prepare for the worst and hope for the best:
  - Push ahead quickly with a new chip in order to have production chips available in early 2003 or sooner.
  - Request a relatively modest amount of resources for R&D in FY01:
    - Develop and prototype new port-card, hybrid, mechanics, and cooling.
    - Pursue DAQ issues for pixel option and prototype mechanics and cooling.



# FY01 R&D Request

Item	Estimated Cost k\$	Contingency	Total Costs
FE Chips submissions	60	30	90
Hybrids (LBNL)	55	25	80
Port cards	20	10	30
Module Mechanics	20	10	30
Support Mechanics & Cooling	100	50	150
<b>Total M&amp;S</b>	<b>255</b>	<b>125</b>	<b>380</b>
Manpower	Estimated (FTE-years)	Contingency	Total
IC Engineers	1.5	0.5	2.0
Port-card Engineering	0.5	0.25	0.75
Technicians	2.0	1.0	3.0
Mech. Engineering	1.5	0.75	2.25

Table 4: Resources required for micro-strip R&D in FY01.

Item	Estimated Cost k\$	Contingency	Total Costs
DAQ Test stand	15	7.5	22.5
System Mechanics	20	10	30
Staves prototypes	20	10	30
Cooling	15	7.5	22.5
<b>Total M&amp;S</b>	<b>70</b>	<b>35</b>	<b>105</b>
Manpower	Estimated (FTE-years)	Contingency	Total
Mech. Engineering	1.0	0.5	1.5
ESE	0.5	0.25	0.75
Design	1.0	0.5	1.5
Technician	1.0	0.5	1.5

Table 5: Resources required for Pixel R&D in FY01.

- **Strips:**

- Priority is the chip design: The chip has the longest lead time. FY01 R&D must include prototypes of new hybrid and port-card. Simple module concept and simple support/cooling structures should be prototyped.

- **Pixels:**

- Much chip/sensor work is on-going (for BTeV)
- Need to focus on CDF specific mechanical (e.g. cooling) and DAQ issues

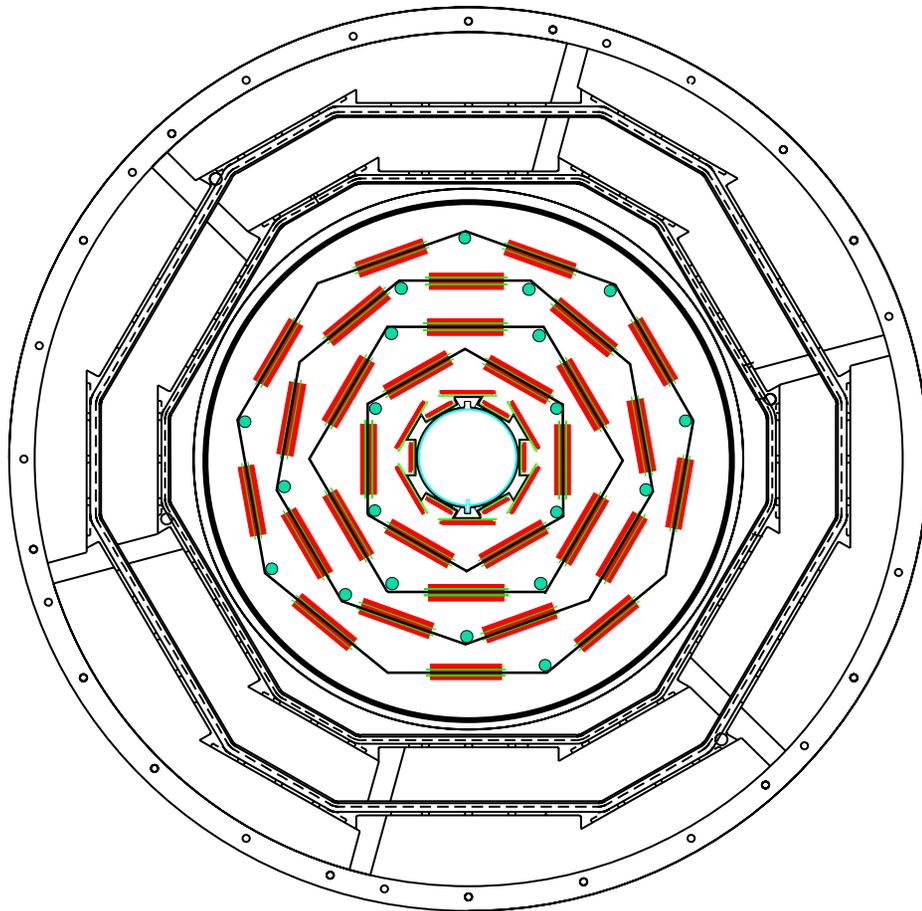


# Conclusions

- Although desirable to hope that the radiation estimates are too pessimistic, it is not wise.
- The FY01 R&D request represents the best insurance for continued and effective operation of CDF in Run 2b. CDF requests that there be a decision to support this R&D program coming out of this PAC meeting.
- CDF wants to determine the appropriate silicon replacement strategy and prepare for the replacement to take place in 2004. This requires:
  - R&D in FY01
  - Continued dialogue with the Laboratory on particulars of the accelerator upgrade schedule
  - Effort to extract the maximum information on the silicon performance in Run2a
  - Detailed studies of particular 'what if' scenarios.
- We need to decide upon and start a replacement project in FY02



# Partial Replacement (detail)



- Pre-build as much as possible (e.g. the inner section)
  - Layer 00 with single-sided hybrids would be built as default
  - Pixels could be installed if ready
  - L0, L1, with simple single-sided hybrids and long readout cables
    - Single sided sensors back-to-back with 90 degree stereo
- Outer section
  - Make new annular bulkheads to support SVXII ladders
  - Would seek to reuse SVXII layers 3,4
    - Spares needed (~15%?) means more double-sided silicon needs to be made
  - Pre-assemble as much as possible then transfer ladders from SVXII



# Preliminary Cost Estimates

Item	Estimated Cost k\$	Contingency	Total Costs
0.25 $\mu$ m Chip submissions	300	150	450
Silicon	800	300	1,100
Fine-pitch Cables	200	200	400
Hybrids & Pig-tails	600	200	800
Power Supplies	200	100	300
Port cards	500	350	850
Mechanics & Cooling	400	400	800
Be beam pipe	150	50	200
<b>Total M&amp;S</b>	<b>3,150</b>	<b>1,750</b>	<b>4,900</b>
Manpower	Estimated (FTE-years)	Contingency	Total
IC Engineers	2.5	1.5	4.0
Mech. Engineers	6.0	3.0	9.0
Module Labor	8.0	4.0	12.0
Final Assembly Labor	4.0	2.0	6.0

Table 2: Costs involved in making a full SVX-II replacement.

Item	Estimated Cost k\$	Contingency	Total Costs
Chip submissions	300	150	450
Silicon	700	350	1,050
Hybrids & Pig-tails	300	150	450
Fine-pitch Cables	200	200	400
Power Supplies	200	100	300
Port cards	350	175	525
Mechanics & Cooling	350	175	525
Be beam pipe	150	50	200
Assembly fixtures	100	50	150
<b>Total M&amp;S</b>	<b>2650</b>	<b>1,400</b>	<b>4,050</b>
Manpower	Estimated (FTE-years)	Contingency	Total
IC Engineers	2.5	1.5	4.0
Mech. Engineers	4.0	2.0	6.0
Module Labor	11.0	6.0	17.0
Final Assembly Labor	6.0	3.0	9.0

Table 3: Costs involved in making a partial SVX-II replacement.

- Both require silicon, chips, hybrids, port-cards, cables, beam-pipe
- Full replacement scenario:
  - mechanics and cooling needs refinement
    - FY01 R&D is critically important
- Partial replacement scenario:
  - (Does not include additional CMM's for barrel assembly stations)
  - FY01 R&D will include work on "barrel 4" to understand disassembly issues