



CDF In Run 2b

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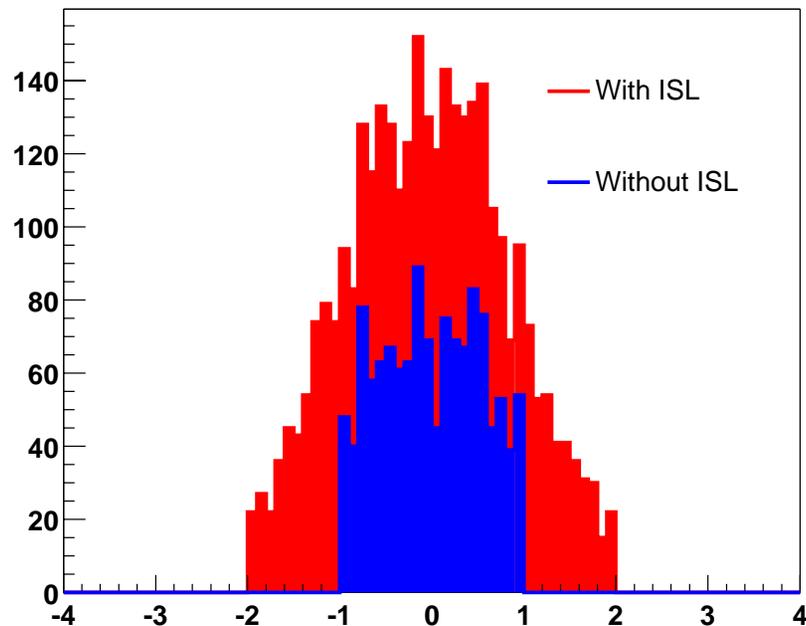
Fermilab PMG

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CDF Run 2b Silicon

Acceptance - Trileptons



- Goal: maximum sensitivity to Higgs and SUSY in 15 fb^{-1}
- Depends mainly upon 3 things:
 - **B Tagging**
 - For $W/Z+H, H \rightarrow b\bar{b}$ the ability to tag b jets in $1 \leq |\eta| \leq 2$ accounts for roughly 2/3 of our sensitivity in this channel.
 - We need the highest possible b tag efficiency while also maintaining low tag rates for charm, light quark, and gluon jets.
 - **Lepton id**
 - For SUSY channels with 3 leptons the ability to track and determine particle momenta in $1 \leq |\eta| \leq 2$ accounts for the majority of our sensitivity.
 - **Energy resolution**
 - Jet energy and missing E_T resolution need to be optimal.



Silicon's Role

- Silicon is not only the primary instrument for b tagging in CDF, it is a key tracking device
 - In the region $1 \leq |\eta| \leq 2$ silicon is our only tracking.
 - Impaired performance at large radius would mean
 - ▶ Loss of momentum resolution which degrades impact parameters.
 - ▶ Loss of extrapolation to end cap calorimeters which limits lepton coverage.
 - Impaired performance at any radius results in
 - ▶ Loss of a track constraint which affects track purity.
 - IP resolution limits b tagging for jets in our silicon acceptance.
 - Tracking improves jet energy measurements



CDF Silicon Issues

● Material

- Material is particularly excessive in the forward regions. Splash will impair ISL performance.
- In the central region, the material will hurt pattern recognition as a result of secondary particle production, loopers etc.
 - Loss of even one layer of SVXII significantly increases the fake rate for SVXII track primitives. (1996 TDR track studies). If ISL occupancy is high due to secondaries, we will not be able to recover.

● Stereo

- Ambiguities in 90 degree layers increase inversely with radius
- Stereo IP resolution is not comparable to Axial resolution

● Accessibility

- SVXII & L00 are not accessible for repairs/replacements.

● Lifetime

- The inner layers will not last 15 fb-1.



Longevity by layer

Layer	R_{min} [cm]	Safe Lifetime [fb ⁻¹]	Cause of Death
L00	1.35	7.4	V_{dep}
L0 SVX-II	2.54	4.3 (5.6)	S/N (V_{dep})
L1 SVX-II	4.12	8.5 (10.9)	S/N (V_{dep})
L2 SVX-II	6.52	10.7	V_{dep}
L3 SVX-II	8.22	23 (30)	S/N (V_{dep})
L4 SVX-II	10.1	14	V_{dep}
L6 ISL Central	20.0	> 40	N/A
L7 ISL Forward	22.0	> 40	N/A
L8 ISL Forward	28.0	> 40	N/A
SVX port-cards	14.1	5.7	DOIM*
ISL/L00 port-cards	27.3	14.6	DOIM*

* DOIM = Dense Optical Interface Module, located on port-card

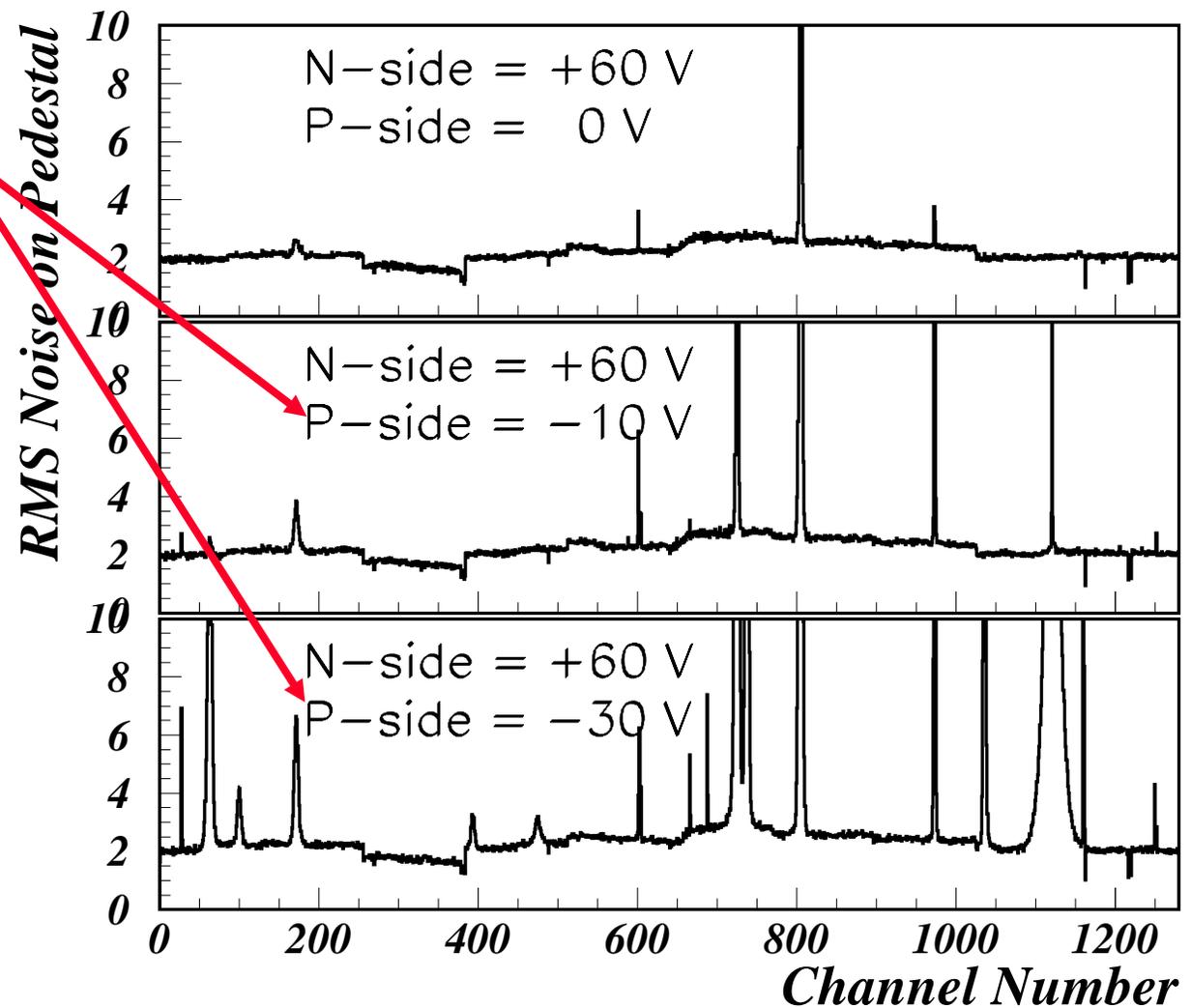


SVX-II: L2 and L4 (bk)

We can't apply much bias to the p-side of Micron silicon without generating a lot of noisy strips.

When this silicon type-inverts, there's a chance it can no longer be biased. *We have not assumed this worst-case condition in our lifetime estimates.*

After inversion, it will not be possible to deplete it for as long as we had hoped.





Progress & Plans

- **Work in Progress**

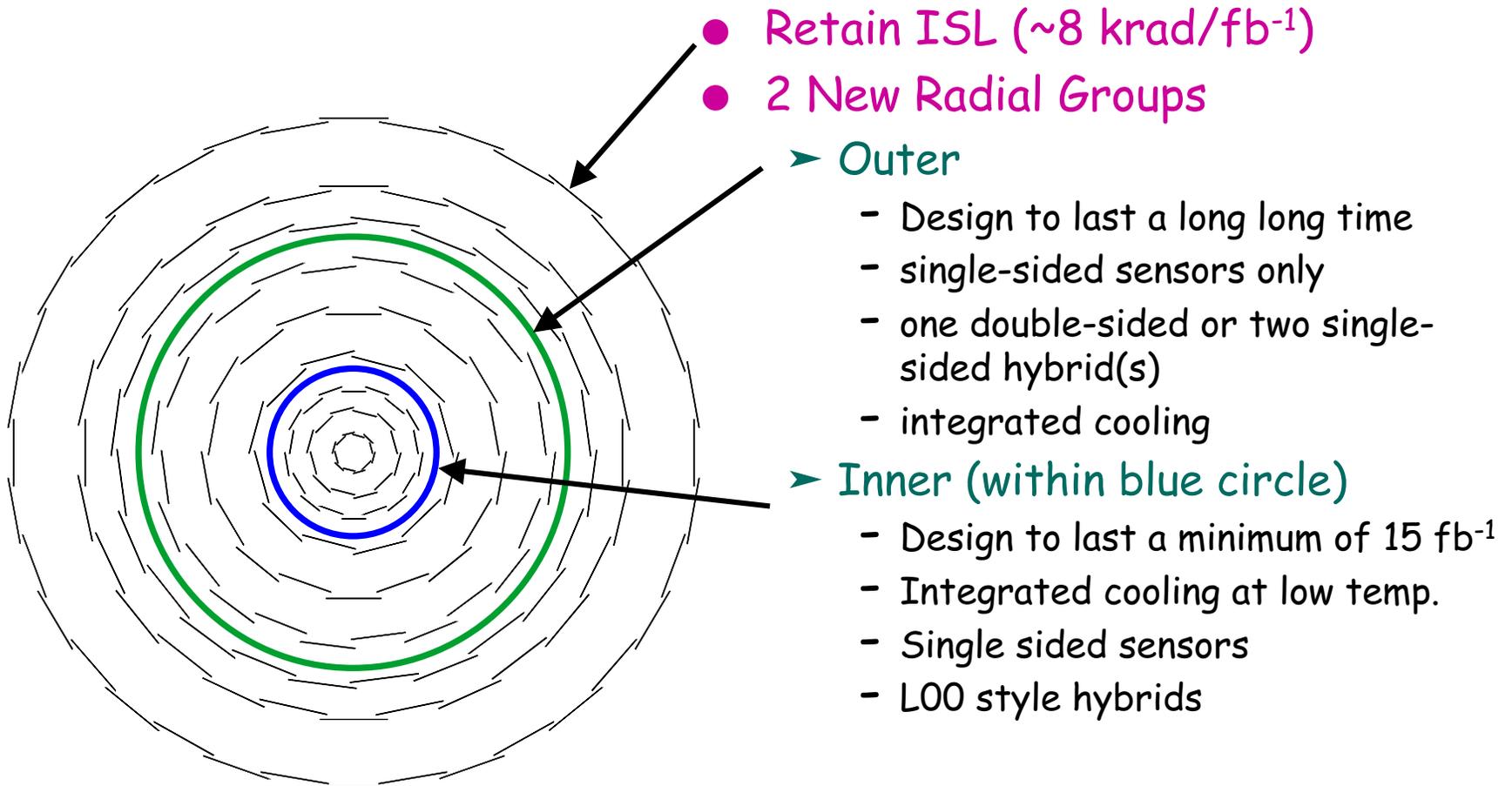
- Layout & performance
- Mechanics & cooling
- Chips & Hybrids
- DAQ & Power Supplies
- Silicon & Lightweight cables

- **Planning**

- Organization
- R&D/Prototyping
- Performance studies & Finalizing the design
- Radiation monitoring
- Cost & Funding



Layout: Basic Concept*



* Has remained constant since inception.



Performance Issues

- **Current Goals**

1. **Improve stereo reconstruction**

- More shallow stereo layers with better resolution
- 3D Resolution: σ_z comparable to σ_ϕ
- Minimize ambiguities in 90° layers

2. **Retain or improve axial layer performance**

- Retain current IP resolution
- Retain SVT

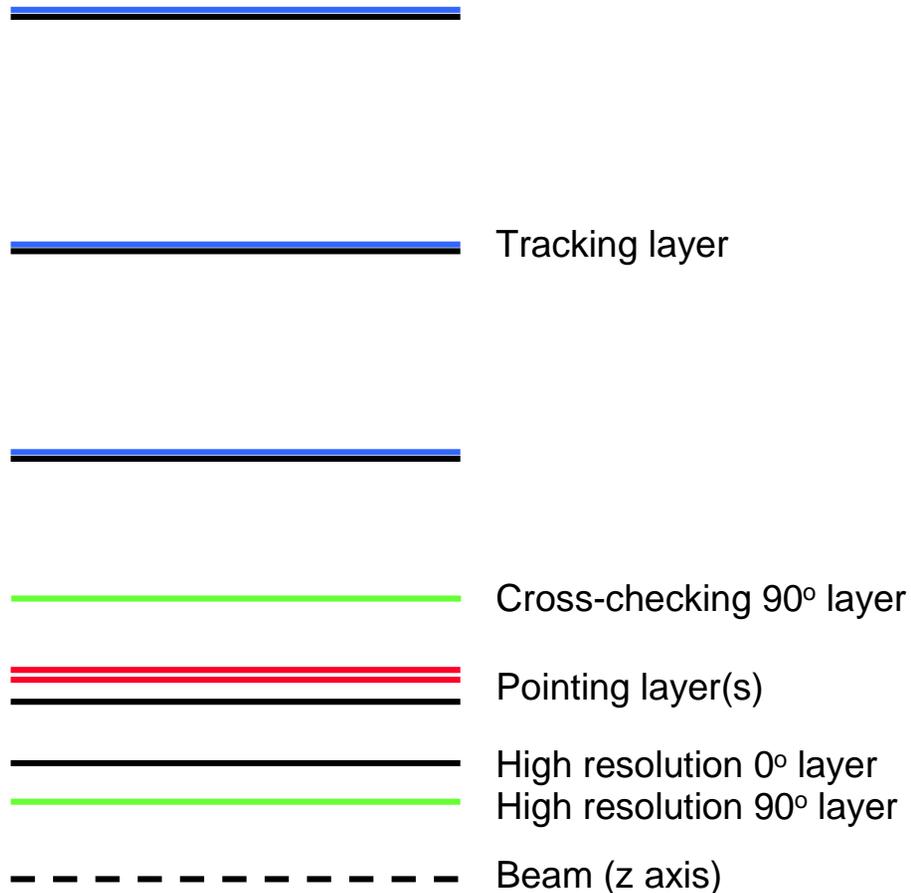
- **Outcome:**

- **True 3D vertexing** \Rightarrow

- Higher b tag efficiency & better discrimination from c,u,d,s and g.
 - ▶ **Transverse vertex mass.**
 - ▶ **Separation of tracks in z which are overlapped in ϕ with adequate resolution for significant displacement to be seen.**



Layout: Current thoughts*



- **Outer region: Tracking group**
 - 3 layers made up of identical modules: Axial + Shallow stereo
 - Modules may use long strips to reduce chip count
 - 50/100 μm pitch/readout
- **Inner region: Vertexing Group**
 - 90° layer for stereo focus & cross-checking (may be unnecessary)
 - Pointing group:
 - 0°, + α , - α triplet with good resolution in z and minimal ghosts
 - This layer may need to be pixels
 - **High resolution layers**
 - Outer layer axial with 25/50 μm pitch/readout
 - Innermost layer 90° with 0 or possibly 2-fold ambiguity and 50/100 μm pitch/readout

*Likely to change...

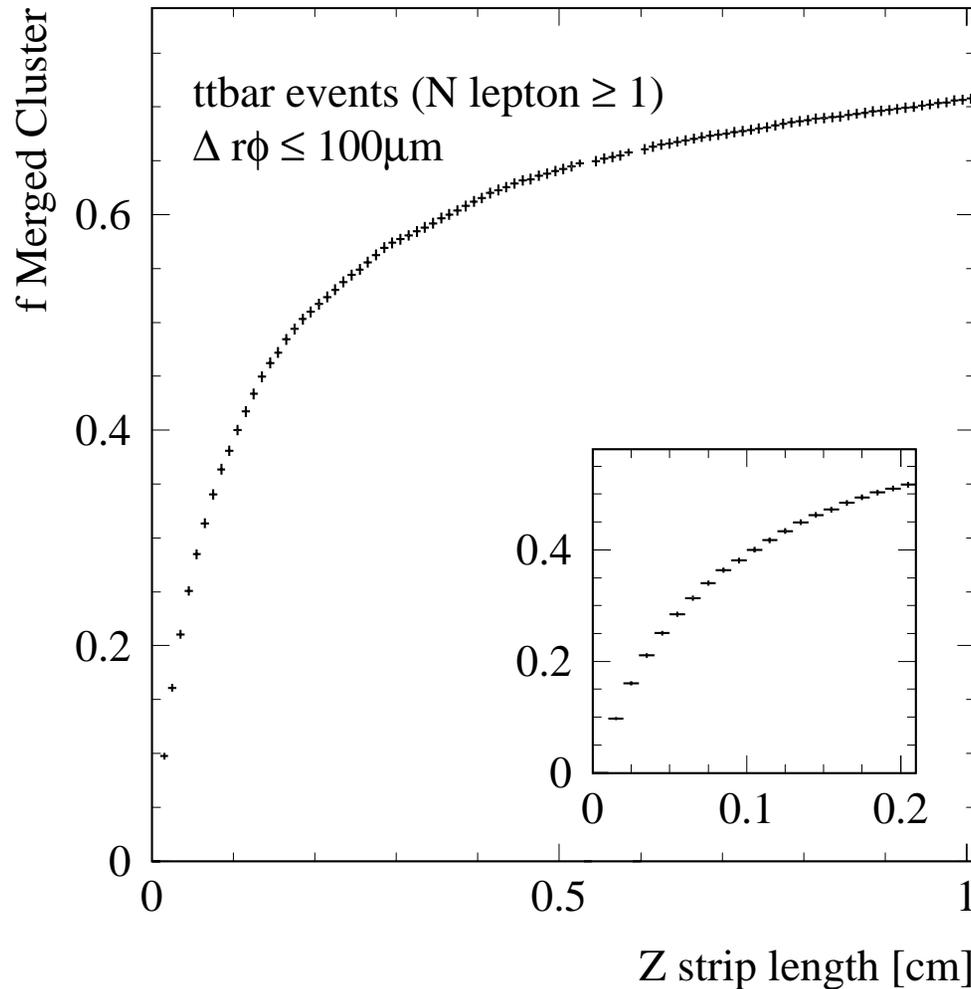


Layout: Motivation

- Outer layers
 - use a single universal module
 - provide reasonable hit resolution
 - $\sigma_z \sim 750 \mu\text{m}$, $\sigma_\phi \sim 15 \mu\text{m}$
 - Combine with ISL for high purity
 - 5 total layers of shallow stereo/axial layers in the forward region
- Inner group
 - Pointing group focuses tracks onto the resolution layers with pointing resolution comparable to strip pitch on those layers
 - High resolution layers then provide exceptional IP resolutions
 - $\sigma_z \sim 15 \mu\text{m}$, $\sigma_\phi \sim 8 \mu\text{m}$
- Material
 - Expect roughly x2 reduction relative to Run 2a in the tracking region.
 - Expect to eliminate almost all the material beyond the silicon in the forward regions



3D Versus 2D



- Beneficial to physics

- Improved pattern recognition
- Separation of hits which would be overlapped in Layer 00
 - In high energy b jets up to 30% of hits are shared in Layer 00
 - 10% or less of these hits are near to each other in z by less than $250\mu\text{m}$ (see figure).
- Good z resolution would provide significant improvements in b tagging purity and even in b tagging efficiency.

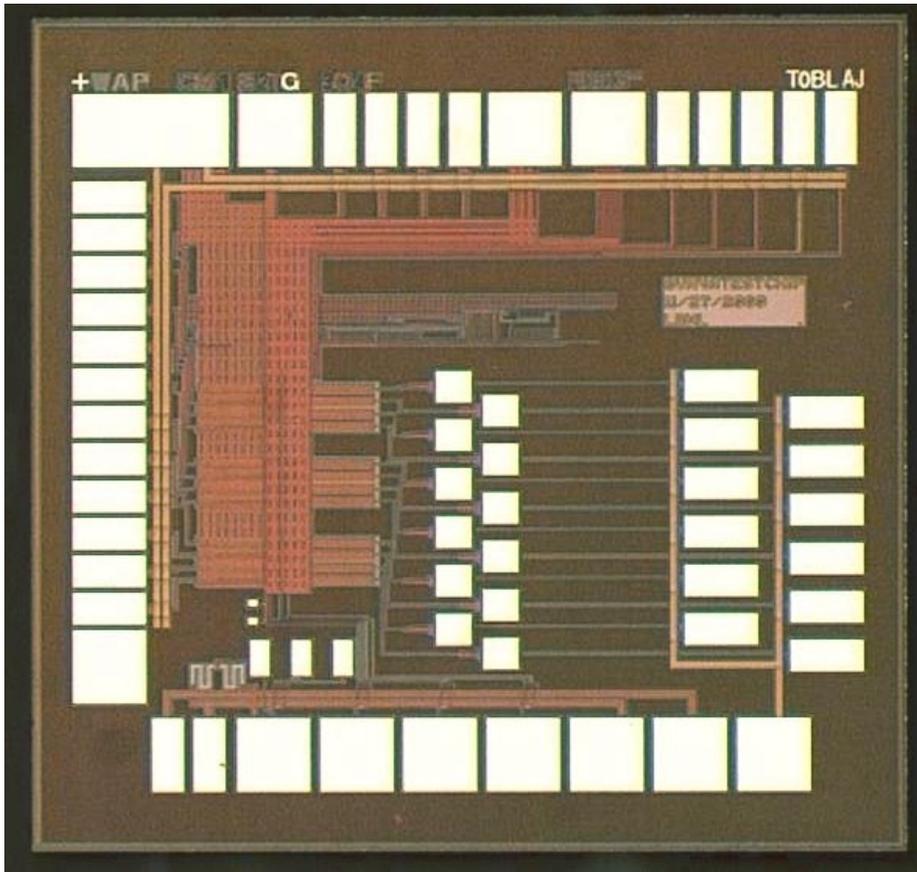


Mechanics

- CERN Visit: G.Derylo, M.Hrycyk, R.Plunket, P.Tipton, and J.Incandela
 - Extensive tours in mid-January
 - CMS engineering and prototyping work for the CMS silicon tracker
 - ATLAS engineering and prototyping work for pixels
 - Learned a lot about materials, cooling concepts etc.
 - CMS will use C_6F_{14} which allows them to cool to -25 C
 - ▶ maybe something we should at least consider ?
 - ATLAS pixels taught us that cooling is a major consideration.
 - ▶ 5 years of R&D on two phase cooling system at CERN
 - ▶ Beautiful low-mass, self-regulating system.
- UCSB involvement: D.Hale and S.Kyre have joined the design team.
 - Valuable Babar & CLEO low-mass, high precision mechanics experience.
- Current activities:
 - Meet bi-monthly with Mike Hrycyk and A small handful of top experts from CDF silicon community
 - Converging fast
 - Established the relevant ranges of possibilities for specifications
 - Mike has started thinking about a simple layout and its assembly



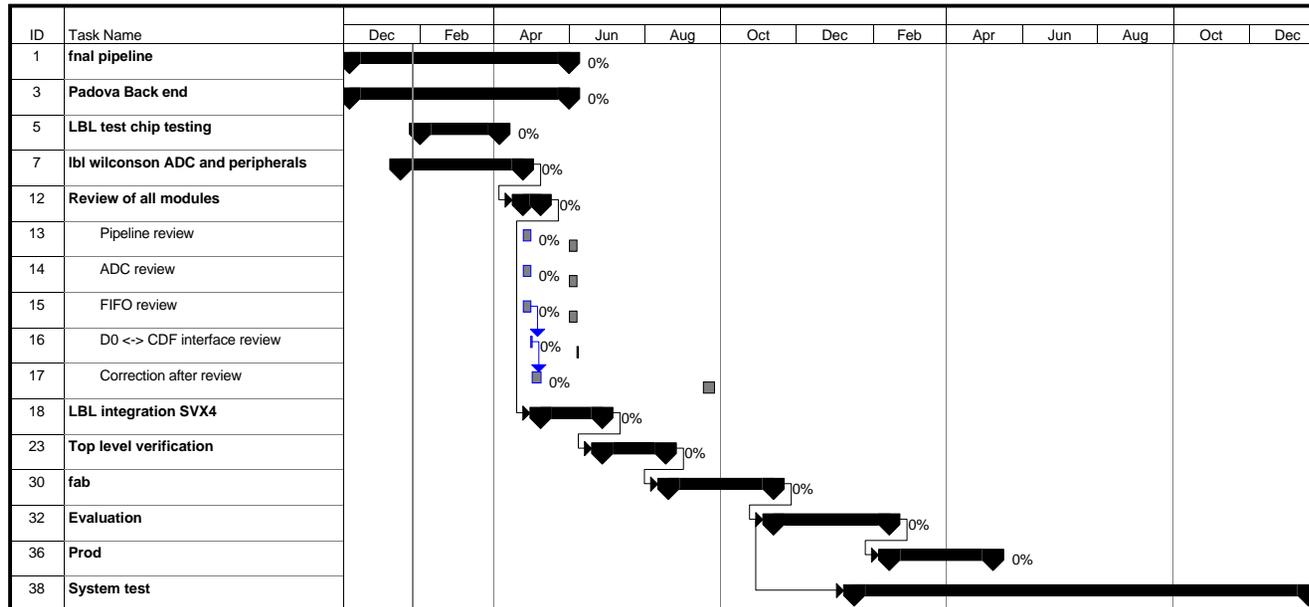
SVX4 Chip



- DØ can use SVX3 architecture
 - Tests successful in operating SVX3D non-dead-timeless
 - DØ SVX4 a different size
- SVX4 in 0.25 μm CMOS
 - Intrinsic rad-hard (to 30MRads)
 - Confidence in simulation models
 - Commercial foundries: cheap, with short lead times, high yield.
- MOSIS test chip with the new preamp just received.
 - Tests in progress at LBNL to:
 - Validate simulation results.
 - Increase experience with TSMC
 - Produce a device that can be radiation-tested.



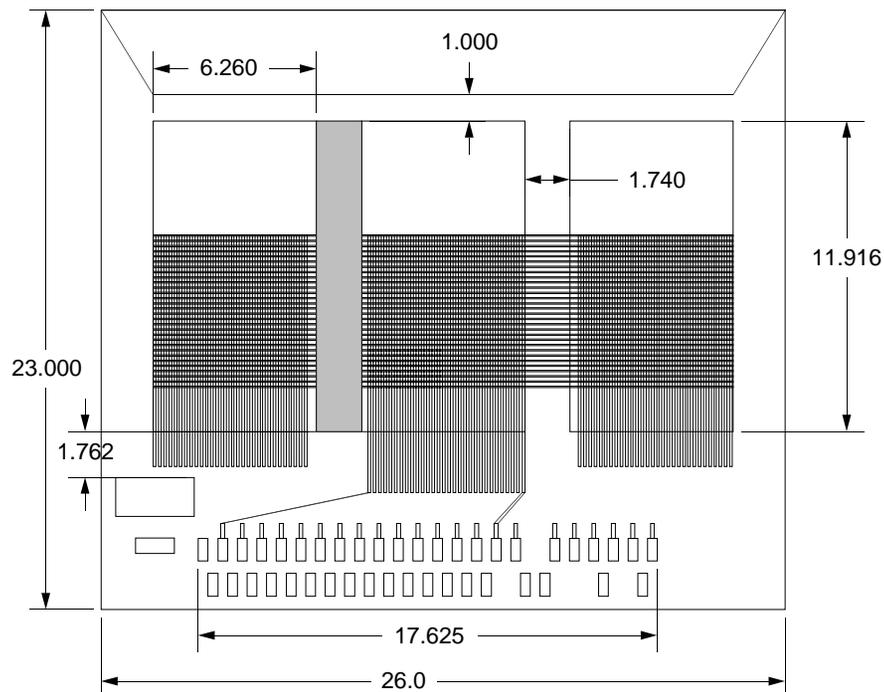
SVX4 Schedule



- Work started LBL Spring '00
- New pre-amp and bias cct. Summer '00
 - By Milgrome/LBL and Neviani/Padova
 - Simulations show lower noise & power and higher bandwidth
- MOSIS test chip received '01
- Design work in progress
 - FNAL: pipeline (1 FTE)
 - Padova: FIFO & Counter (2 FTE)
 - LBL: preamp & integration (1 FTE)
- Technical review April '01
- First full chip submission July '01
- Production Chip by Spring '02



Hybrids



3 chip hybrid concept
CDF-Run2b SVX-IIB
6/12/2000 C.Haber

- Layer 00 technology
 - Combine screening with etching to achieve high density
 - Smaller more compact hybrids
- Recently established a footprint for outer layer hybrids
 - 53.2 mm wide
 - 4 chips
 - Al_2O_3 or BeO substrate 0.015-0.025 inches thick
- Inner layer prototypes
 - we can use L00 hybrids
- Prototype plans
 - Will layout this hybrid and make a handful in the next 6 months



DAQ & PS

● DAQ

➤ Current plan:

- Eliminate DOIMs & Merge portcards and junction cards via addition of buffers and transceivers with special attention to terminations.
- Gang hybrids as needed

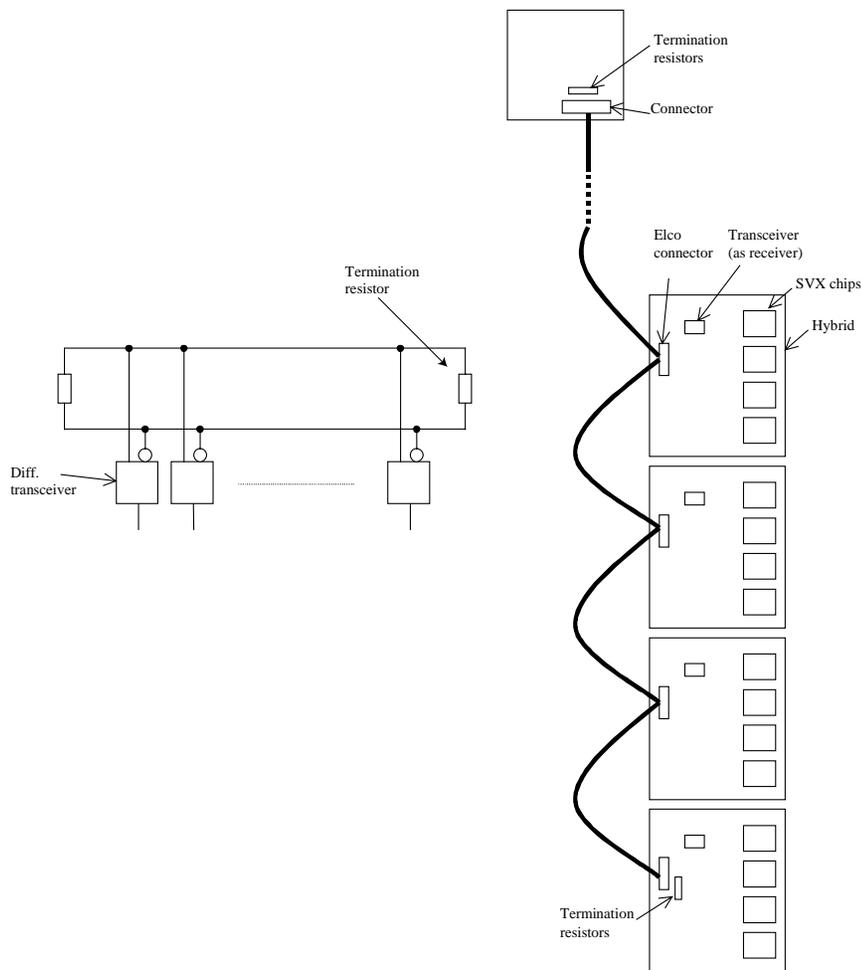
➤ Motivation

- DOIMs entail a lot of excess material and they will die w/radiation
- Merging portcards and junction cards, via additional buffers and transceivers means a significant reduction in complexity and material

● Power Supplies

➤ Maintenance and Spares

- Padova to talk to CAEN about long-term maintenance of existing supplies and options to buy more LOO or ISL type supplies.





Silicon & Cables

● Silicon

- Considering 2 SS mask sets for the outer layers and 3 to 4 SS mask sets for the inner detector layers.
- No strong need to prototype for radiation testing.
 - LHC has done extensive testing
 - Layer 00 will be a useful gauge
- Have quotations from HPK.

● Lightweight Cables

- Japanese Company now making a Layer 00 cable
 - Belle cables were very high quality and lighter than those in L00
 - Delivery March 2nd to Itsuo Nakano (Okayama U.)
 - Cost looks reasonable
 - ▶ 4k\$ for masks and \$700 per sheet (5 cables) ⇒ \$300/cable at 50% yield
 - ▶ If we used cables everywhere, the cost would be \$400k at 50% yield



Organization

- **Goals**

- Get things moving asap
- Keep things simple for cost and schedule containment

- **Run2b Silicon Leadership and Guidance**

- JI will lead group in CY01
- Forming an internal steering committee of top CDF experts
 - Determine the initial specifications *with emphasis on simplicity for cost and schedule containment*
 - Will review any proposed changes to design over time
 - ▶ This is to insure that we do not significantly complicate the design (e.g. for insignificant or small improvements) as the project progresses.
- One group co-leader to be added this year.
- 2nd group co-leader in CY02 will replace JI



R&D/Prototyping

- Plan to build a few ladders
 - Silicon (existing L00 or LHC)
 - Lightweight signal cable (in production)
 - Hybrid with existing chips (in design)
 - Mechanical support (in concept)
- Plug into existing DAQ with approx. Run 2b Configuration
 - Mother cable (in concept) from hybrid to HDI
 - Long HDI (existing ISL)
 - "Port-card" (existing)
- Schedule & Outcome
 - Could have this done by sometime this summer (?)
 - Would resolve almost all of our outstanding issues about our proposed configuration



Studies/Design Finalization

- Performance Studies

- Code is mostly in place for studying the main aspects of pattern recognition and track parameter resolution for b tagging

- Cannot do extremely detailed studies before June
- Expect nevertheless to be able to demonstrate the impact of a full silicon replacement on Higgs sensitivity

- Basic plan

- For various configurations of active and dead material in the tracker we can roughly calculate the expected track parameter covariance matrices and secondary particle production rates.

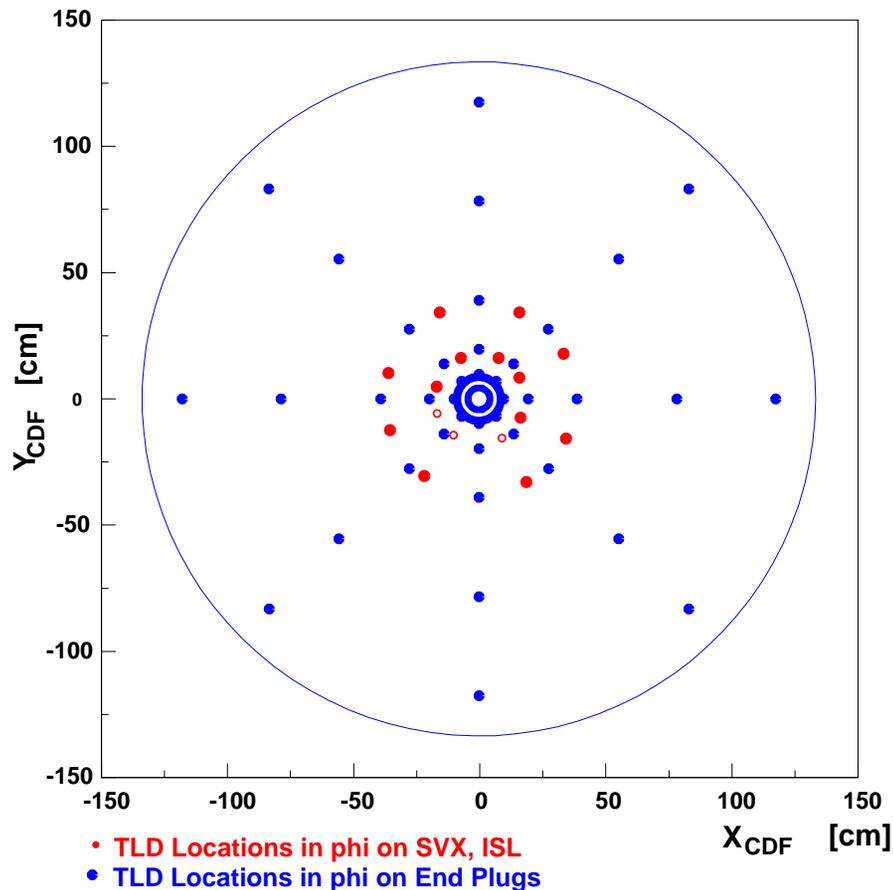
- ▶ Using the covariance matrices: Generate events and handle the tracking parametrically to determine the performance *for perfect pattern recognition*
- ▶ Using the secondary particle estimates: Study the effect of adding tracks to core of high ET b and light quark jets. How is tagging and mistagging affected ?
- ▶ Also plan to study the ghost hit rates for both of the above cases

- Finalizing the design: Single CDF Run 2b proposal for June PAC

- This could be straightforward if the performance studies show clearly that Pixels are or are not necessary to meet our physics goals.



Radiation Monitoring



- Run 2a Dosimetry

- Cross-check other monitors
- Predict damage profiles

- Positioning

- A fairly extensive system of monitors now in place
- Based on toy study with 3 source components: Uniform in space, Cylindrically Symmetric about beam, Spherically symmetric about IP

- Status

- Mylar leaders installed
- Calibrations complete
- Holders loaded
- TLDs to be installed this week



Preliminary Cost Estimates

Item	Estimated Cost [k\$]	Contingency [k\$]	Total Cost [k\$]
SVX4*	150	75	225
Silicon	800	400	1200
Signal Cables	400	200	600
Hybrids & Cables	600	200	800
Power Supplies & Crates	400	200	600
P/J Cards	400	300	700
Beam pipe	150	50	200
Mechanics & Cooling	400	400	800
TOTAL M&S	3,300	1,825	5,125

- **Estimates**
 - Silicon, Hybrids, Signal Cables, SVX4 costs reasonably well understood
 - Other estimates uncertain and will be refined this year
- **Additional Funding sources**
 - Japanese will contribute strongly to Silicon and Signal Cables
 - Hope for Italian help on Power Supplies, SVX4 and Silicon
 - University support in FY01 for R&D

* Assumes half of this cost is accounted by D0



FY01 R&D

Item	Estimated Cost [k\$]	US Cost [k\$]
SVX4*	?	?
Silicon	0	0
Signal Cables	40	0
Hybrids & Cables	40	40
Power Supplies & Crates	0	0
P/J Cards	40	40
Beam pipe	0	0
Mechanics & Cooling	50	50
<i>TOTAL M&S</i>	170	130

- Rough Estimates
- University funds may be available
- Does not include SVX4 development costs



Summary

- Will replace SVXII and L00
- Run 2b system will be simple, robust and powerful
 - Eliminate port-cards
 - Single sided silicon and lightweight signal cables
 - Factor of 2 reduction in material
 - Unambiguous 3D vertexing with excellent resolution in both views
- Focus on simplicity
 - Cost and schedule containment
- Minimal R&D
- Target:
 - Final design by end of FY01
 - Start production in FY02