



CDF in Run 2b

J. Incandela

PAC Meeting, Fermilab

April 14, 2000

- Motivation
- Recent Workshop
- Key Issues
- Emerging View

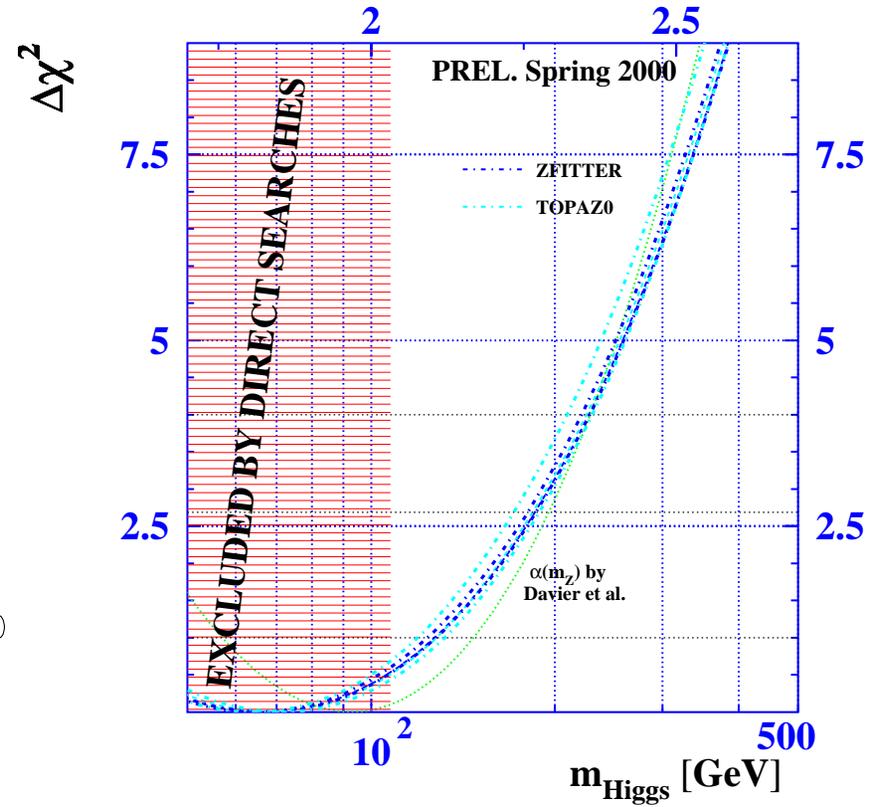
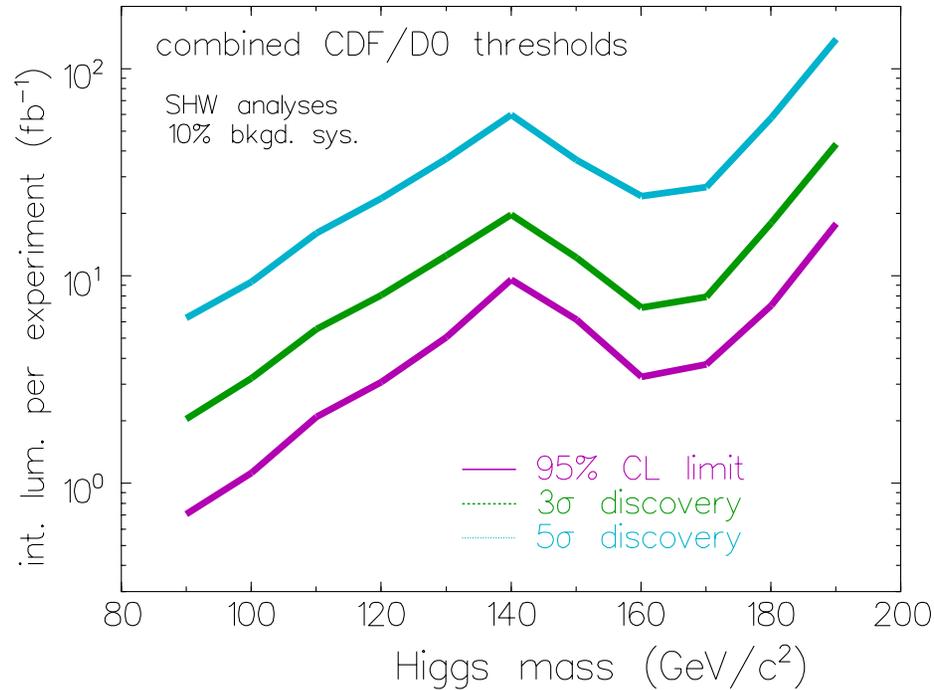


Motivation

- CDF and DØ can make major advances with adequate data.
 - SUSY/Higgs workshop: 30 fb⁻¹ per experiment ⇒
 - SM Higgs observed or excluded up to ~180 GeV
 - Work in progress may yield more sensitivity
 - Significant new sensitivity to SUSY partners
 - Major advances in bottom, top, and W physics
- To maintain the energy frontier
- CDF and DØ silicon detectors were designed for ~3 fb⁻¹
 - In hindsight, this was a mistake.
 - We need to replace the silicon when it is damaged and do so in a way that facilitates our ability to accumulate as much data as possible for as long as possible.



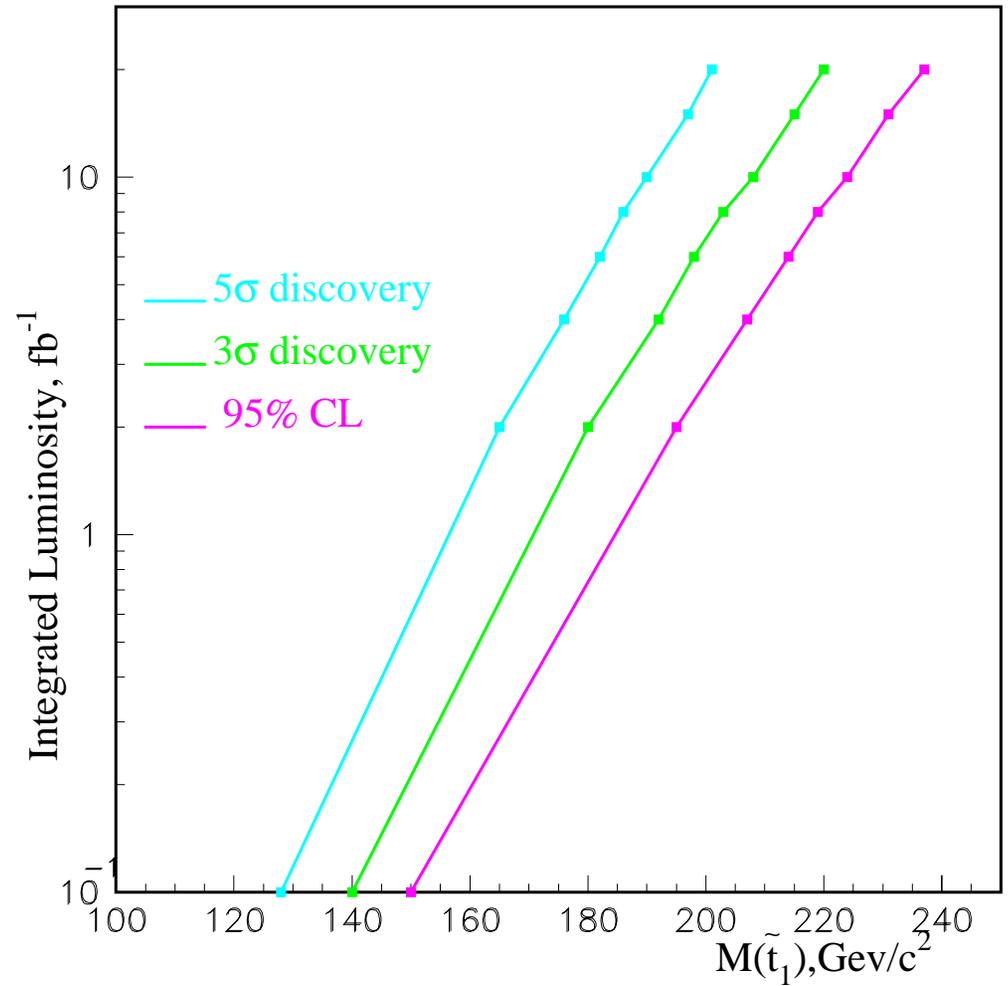
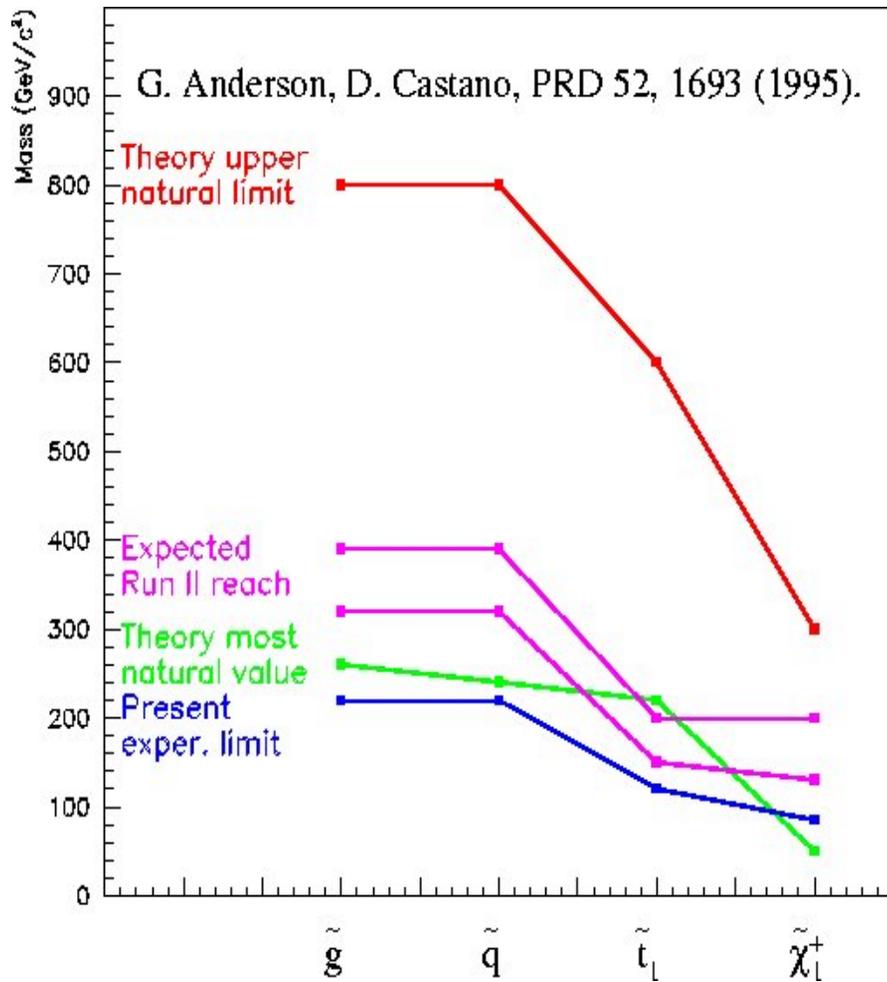
Higgs Search





SUSY

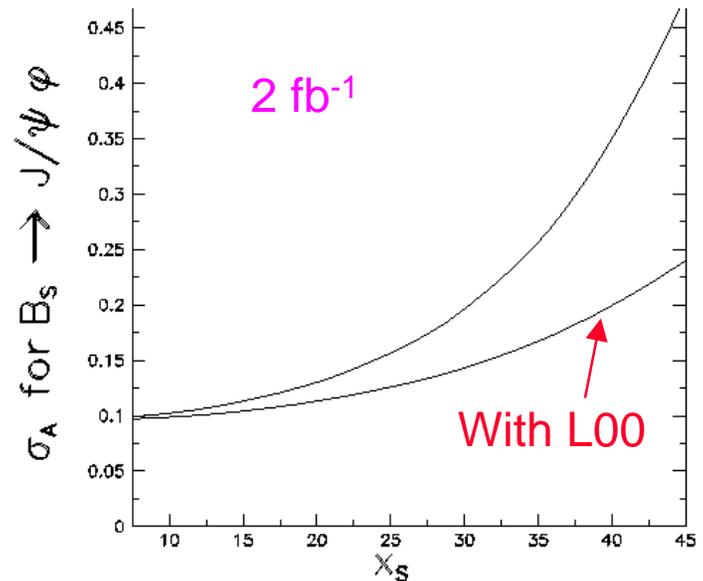
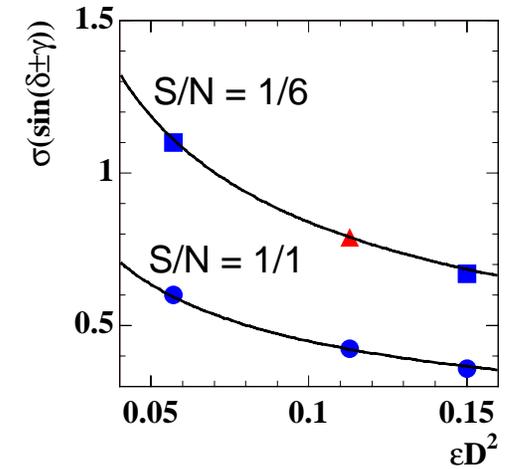
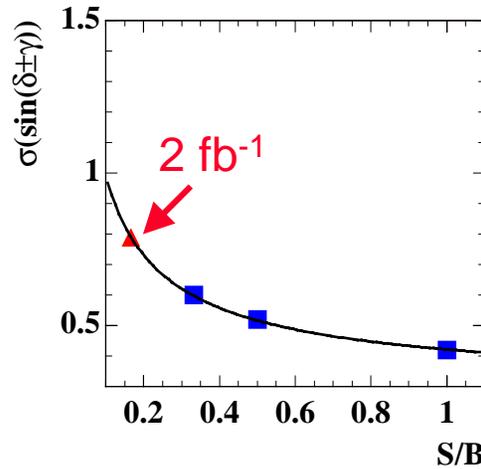
Tevatron Reach for Supersymmetric Top





B Physics

- γ measurement with $B_s \rightarrow D_s K^+$
- CP asymmetries in $B_0 \rightarrow \pi^+ \pi^-, K^+ \bar{K}^-$
(Related to α, γ)
- CP asymmetries in $B_s \rightarrow J/\psi \phi$
- $\Delta\Gamma(B_s)$
- Rare penguins $B_0/B_s \rightarrow \mu^+ \mu^- K^*/\phi$
- Rare radiative decays $B_s \rightarrow K^*/\phi \gamma$
- B_c and b-baryon spectroscopy





CDF Run 2b Si Workshop

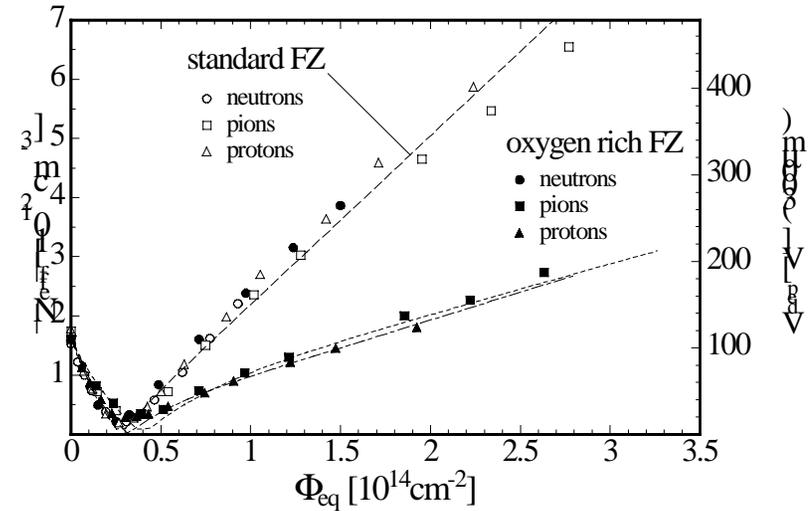
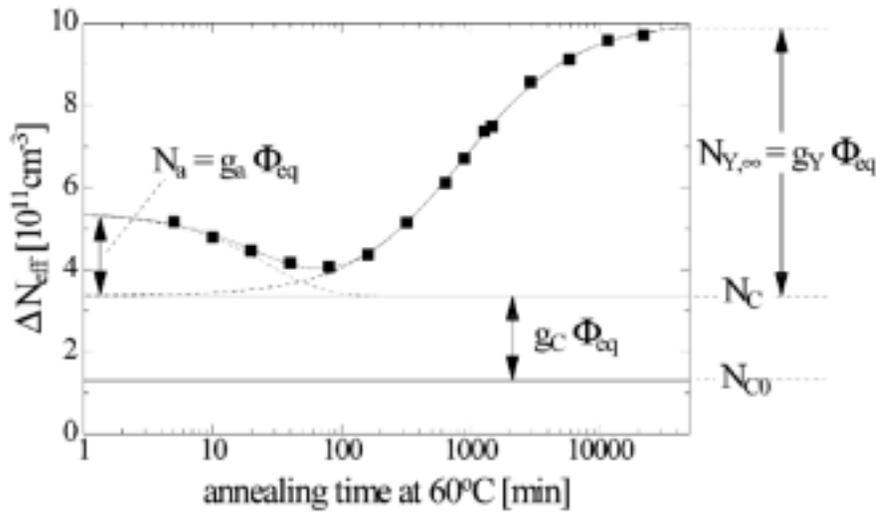
- Workshop held March 15 at FNAL
- Large attendance (~50 persons present and 7 video links)
- Agenda
 - Beam conditions/expectations
 - Run 2a detector review
 - Radiation and lifetime
 - Performance
 - Material
 - Run 2b Issues
 - Rad-hard strips, pixels, diamonds
 - Electronics and DAQ issues
 - Formation of Working Groups
 - sensor technologies (S. Worm)
 - chip development (M. Garcia-Sciveres)
 - overall layout (C.Haber & J.Incandela)

- Key Issues:

- Strips, Pixels, Diamond
- Low-risk, low-cost solution that allows for extended running
- One-for-one replacement or SVX/L00 rebuild
- Readout chips



Strips, Pixels, Diamonds



- N. Bacchetta on Microstrips
 - Reverse annealing strongly temperature dependent. Effectively eliminated near 0°C.
 - Oxygenated detectors (will be installed in L00 for Run 2a)
 - Smaller damage coefficients for charged particle but not for neutrons
- W. Wester on Pixels
 - R&D well-advanced and a pixel system for CDF would be attractive and achievable
- J. Conway on Diamonds
 - ∃ serious non-uniformities. Need extremely low noise readout ⇒ still a long way off.



Delay and Problem Sources in Run 2a Silicon Projects

● Silicon

➤ Double-sided silicon

- difficult to manufacture and handle
- not rad-hard
- saves little material

● Ladder Design and Assembly

➤ Mounting hybrids on silicon increases technical difficulty and cost

- excess material
- risk of damage
- operational complications

➤ Intertwining construction and wirebonding increases technical difficulty and cost

- greater pinhole production

● Electronics

➤ Small rad-hard production facilities carry many risks



Lessons Learned

- Silicon
 - single sided microstrips now an industrial product
- Design and assembly
 - Mount hybrids off silicon and, whenever possible, outside of the tracking region
- Electronics
 - Rad-hard chips can now be manufactured using standard processing in large industrial lines (sub-micron technology: TSMC, IBM)
 - better development tools, higher yields, lower costs
 - better performance
 - FE electronics and hybrids should be simple to manufacture and very robust
 - Electronics should begin to appear in quantity well before real module production starts in order to catch problems and avoid bottlenecks
- Cost & schedule Estimating:
 - Applying these lessons, one can reliably estimate the cost and schedule for even a large silicon system.



Recent Experience

- CDF ISL Module Production

- Simple module design w/Hybrids mounted off silicon
- Construction is not difficult:
 - Assembly less than 1.5 h.
 - Wirebonding ~ 1 h.
 - Repair \leq 1 h per module.

- Single-sided silicon

- An industrial product
- High quality, rad-hard
- Short lead times
 - From final specifications to delivery of all L00 silicon was ~4 months. CMS prototypes had similar experience.
- Commercial capacity:
 - HPK can start 10k wafers/month
 - ST-Catania has similar capacity

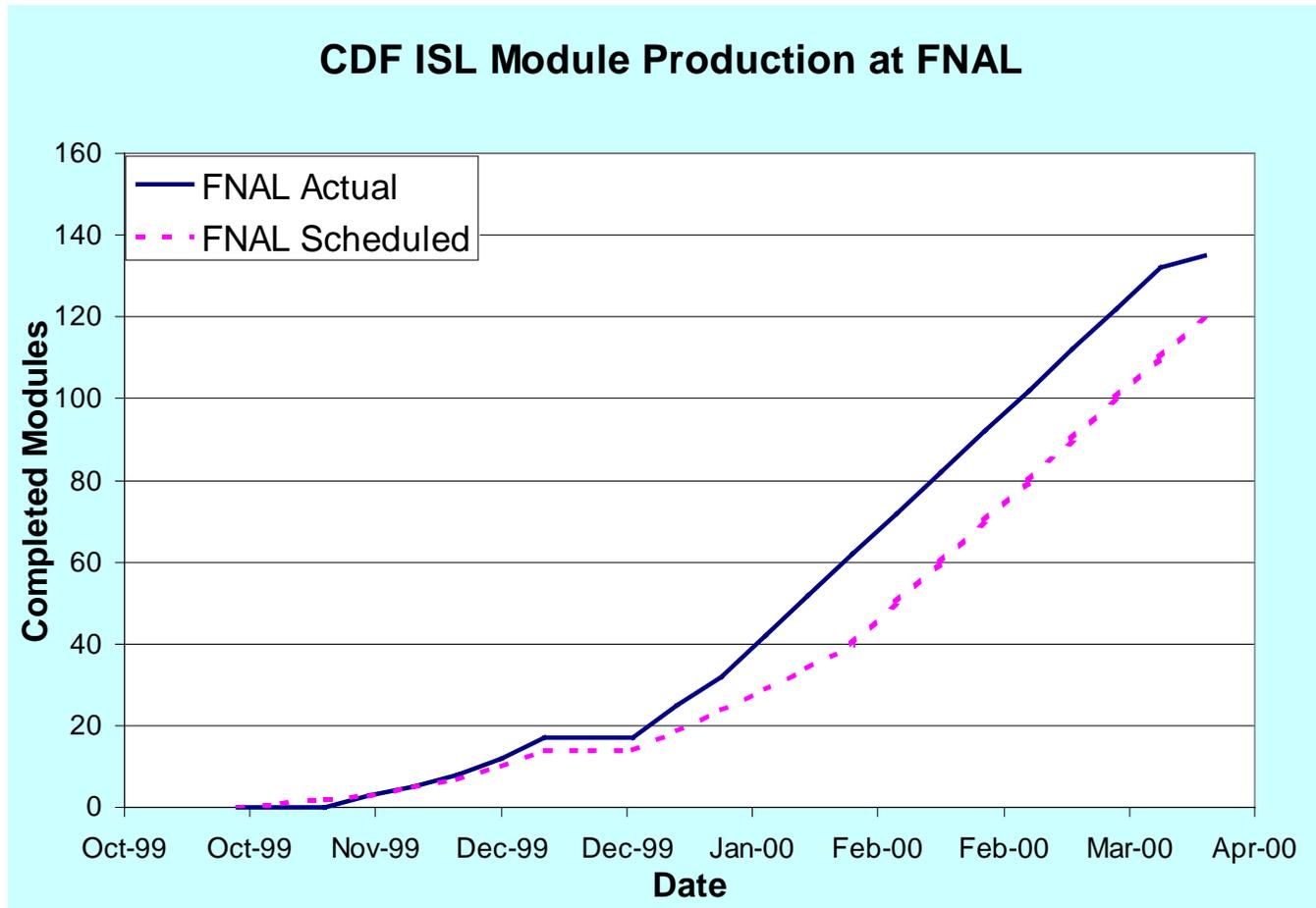
Rad-tolerant Layer 00 Silicon (HPK)

Specifications	wide	narrow
# channels	256	128
active area (cm ²)	9.7	4.8
implant pitch	<u>25μm</u>	
readout pitch	50 μ m	
implant width	8 μ m	
Test Results		
bad strips (@100 V)	0.10 %	0.047 %
depletion voltage	\approx 65 V	\approx 65 V
current @ 500V (nA/strip)	0.5-1.0 typ.	0.5-0.8 typ.

single-sided *p-in-n* silicon



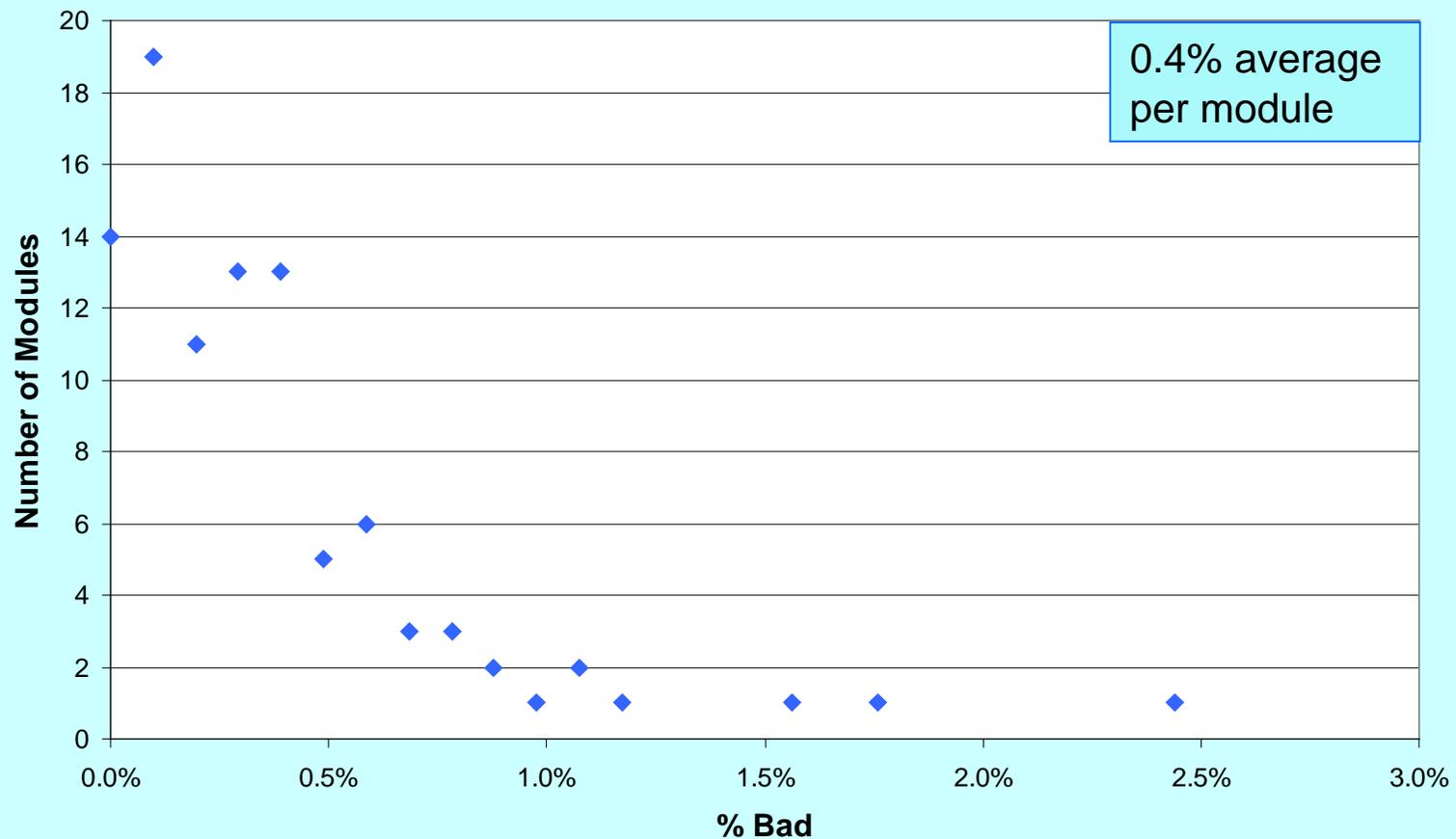
ISL Production at FNAL





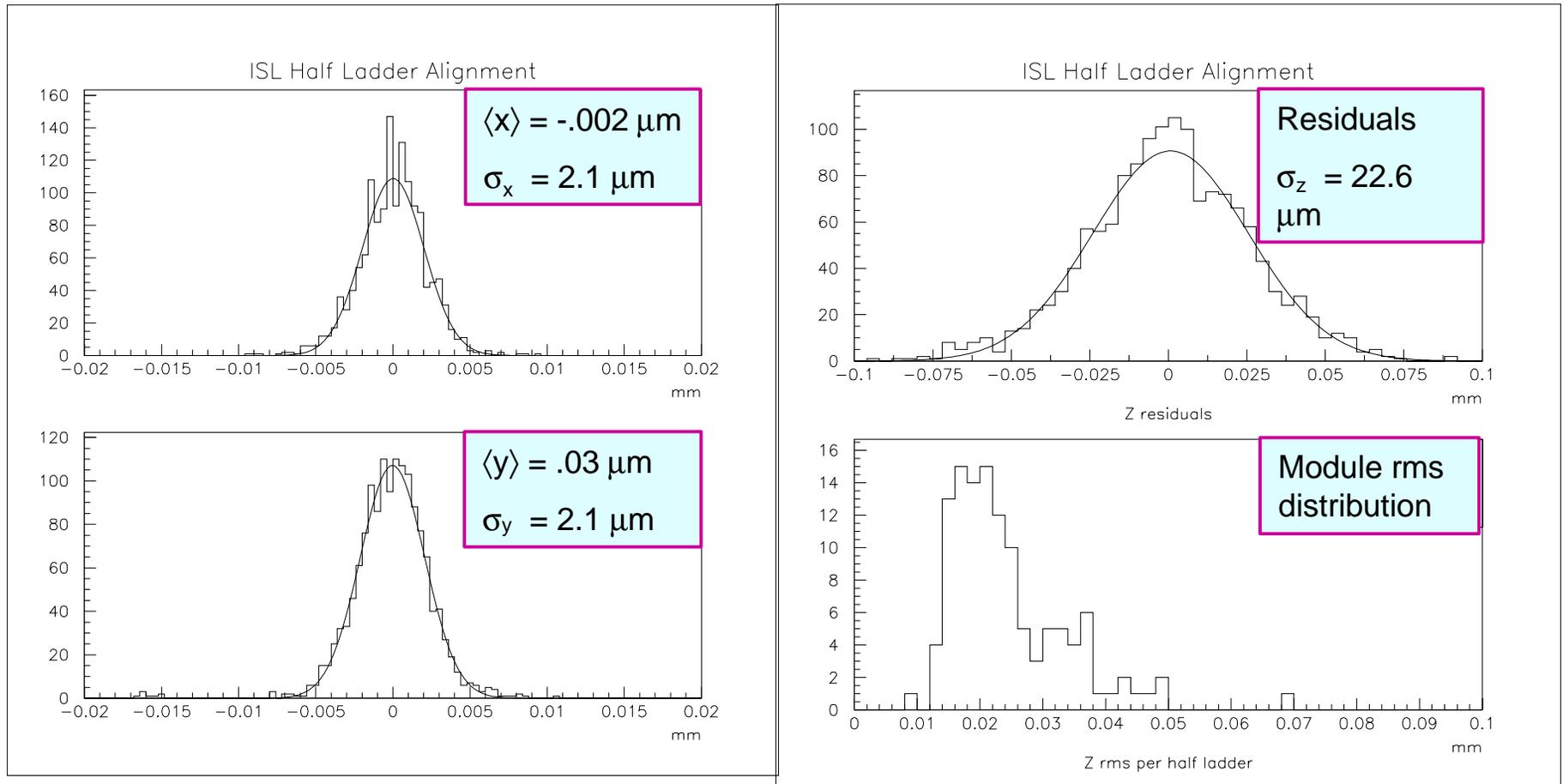
Quality (1)

% Bad Strips Formed During Module Production





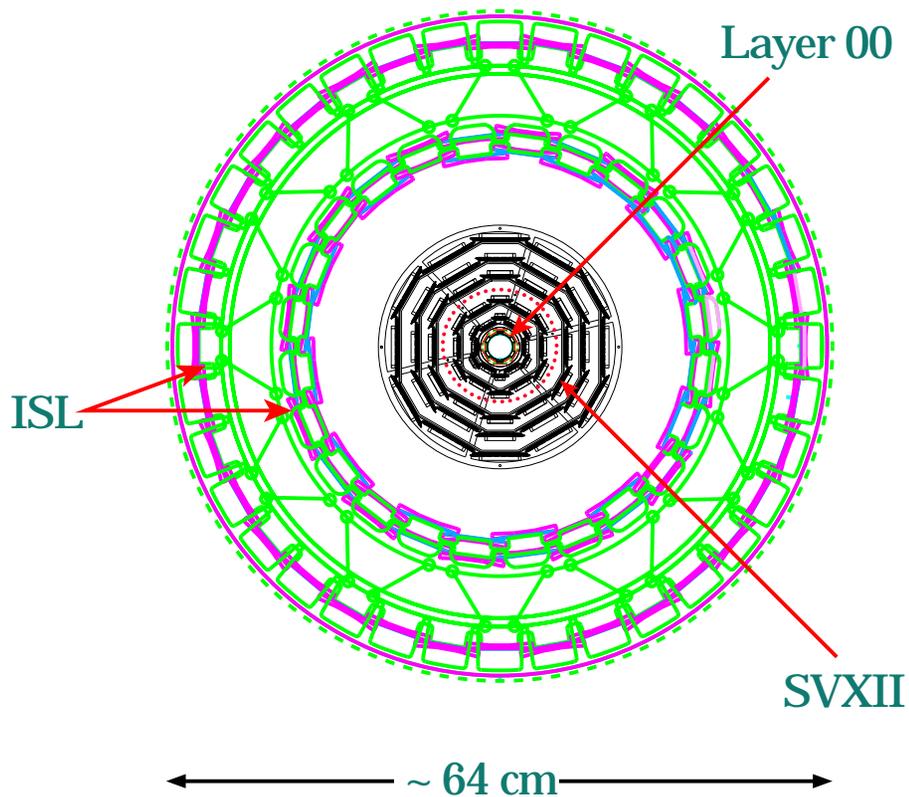
Quality (2)





Current System

- CDF Run 2 tracker qualities
 - Coverage
 - Pattern recognition
 - Resolution





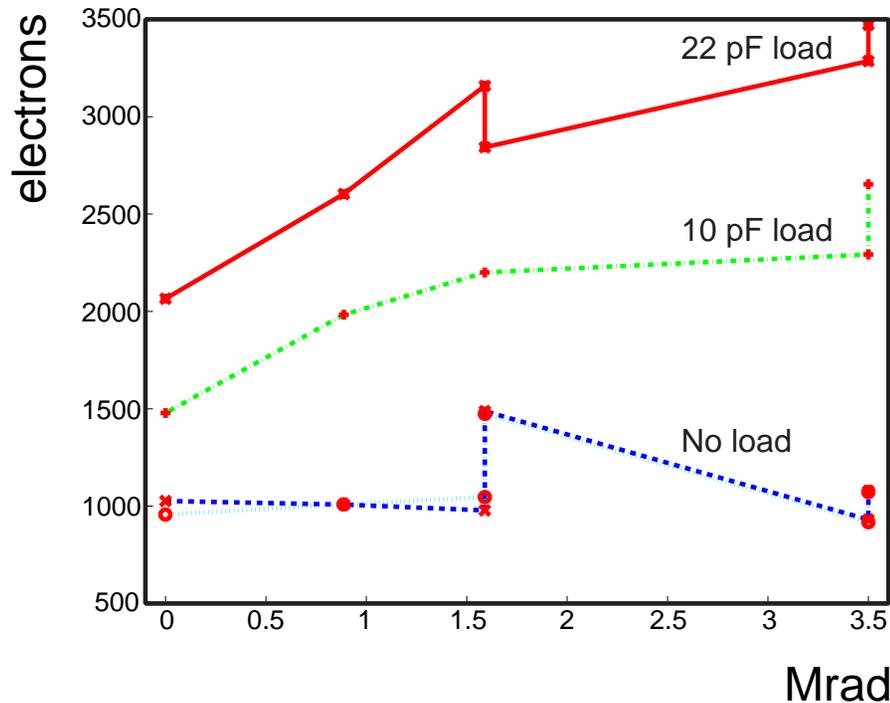
One-for-One

- Replacements of only those layers which are damaged
 - Required shutdown would be long and involve risks
 - Handling, disassembling, and rebuilding SVXII barrels carries real risks and would require significant reconstruction and testing time during the shutdown period.
 - **Extract ISL and transport to SiDet**
 - **Remove SVXII spacetube and split it open**
 - **Remove Beampipe/L00**
 - **Remove all 3 Barrels and transfer to barrel fixtures**
 - **remove all ladders and Re-align bulkheads**
 - **Start assembly sequence all over again...**
 - Any subsequent replacement/repair/upgrade entails equivalent shutdown/risks
 - **Space constraints**
 - Bulkhead structure means we'd have to retain Run 2a geometry and structure
 - **Electronics mounted on silicon - source of heat to silicon**
 - **No direct silicon cooling - lose rad-hardness of strips, pixel option untenable**
 - **Honey-well SVX3 chip will likely not hold up well to radiation**

Lifetime of replacement would be very limited



SVX3 Irradiation



- D. Sjorgren et al. CDF Note #4461
 - 3.5 Mrad dose, 22 pF loaded channel saw noise increase of 75%.
 - Even at 2 Mrad ($\sim 5 \text{ fb}^{-1}$ at $R= 2.8 \text{ cm}$) the noise increase is significant.
 - 1 chip was irradiated to 6 Mrad and no longer functioned.



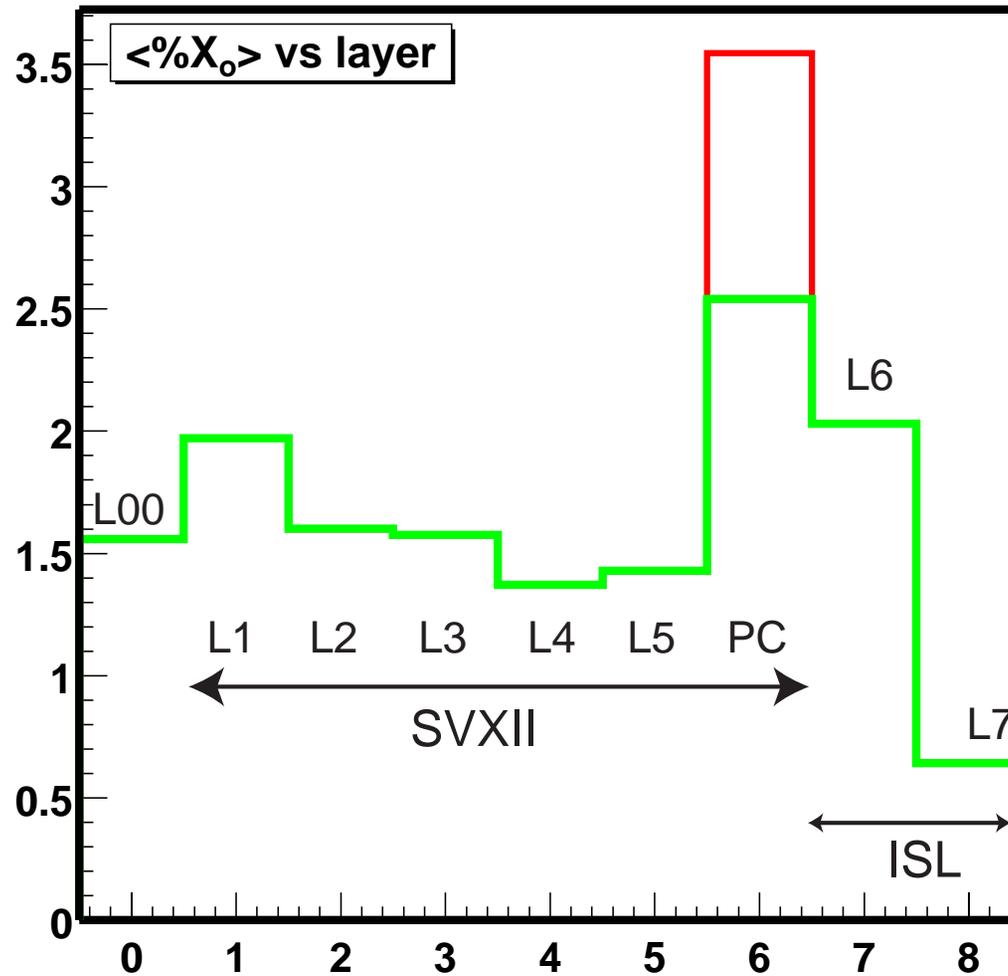
All-for-All

● Full SVXII/L00 replacement

- Ready prior to Tevatron shutdown \Rightarrow no more than 6 months beam-to-beam
 - Use single sided silicon \Rightarrow rad-hard at low cost with fast production & predictability
 - An inner layer could be pixels if ready on time. Build strips in any case.
 - Universal module types \Rightarrow low cost, fast production, predictability
 - Design to include an inner radius section that is easy to swap out so that
 - any future shutdowns can be minimal - as little as 4 months.
 - any future replacements would be small scale
 - we could recover from a major accident or upgrade to pixels for the option of higher luminosity running
- Integrate cooling with silicon (ala CMS or L00)
- Reduce overall material budget from $\sim 13.5\%$ to $\sim 10.5\% X_0$.
 - Some things add material
 - 2 sensors/layer adds $0.3\% X_0$ /layer (currently we have ~ 1.5 - $2.0\% X_0$ /layer in SVXII).
 - Integrated cooling adds some mass (cf. L00)
 - Other things subtract
 - Removing portcards from the tracking region cuts material by $\sim 3.5\% X_0$.
 - Using ISL style double-sided hybrids reduces ave. material by $\sim 0.5\% X_0$ /layer



Material

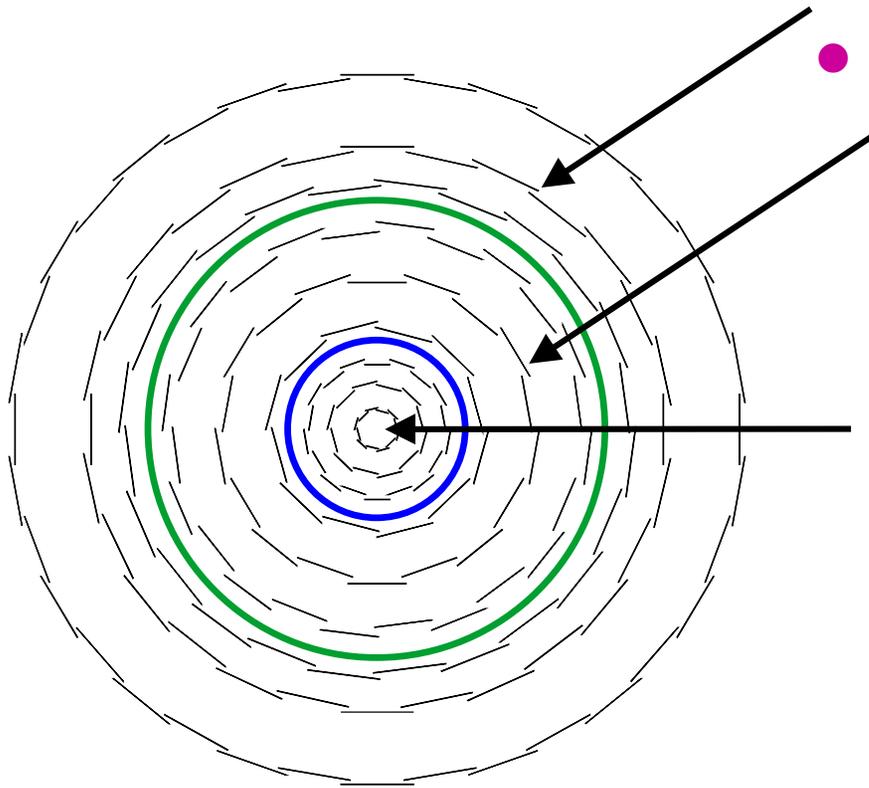


D. Stuart
CDF Note #5268



A Full Replacement Example

- Goal: Keep or improve functionality
- Retain ISL ($\sim 8 \text{ krad/fb}^{-1}$)
- 2 New Radial Groups



➤ Outer (between blue and green circles)

- Design to last a long, long time
- Simple design:
 - two single-sided sensor designs
 - one double-sided hybrid design
 - carbon fiber supports with cooling

➤ Inner (within blue circle)

- Design to last 10-15 fb^{-1}
- Integrated cooling at lower temp.
- Two outer layers w/simple design:
 - 2 single sided sensor designs
 - one double sided hybrid design
- Innermost layer:
 - L00 replacement using existing silicon and hybrid designs
- Pixels
 - an inner layer could be pixels if ready



CMS Support Scheme





Detailed Example

Layer	R [cm]	Nphi	chips	pitch	hybrid pitch	width	total chips	cumulative	phi coverage
L0A-1	1.35	6	1	0.0025	0.005	0.84	36	36	59%
L0A-2	1.65	6	2	0.0025	0.005	1.48	72	108	86%
L1A	3.5	12	2	0.0035	0.007	1.992	144	252	109%
L1S	3.5	12	2	?	0.007	1.992	144	396	109%
L2A	5.25	18	2	0.0035	0.007	1.992	216	612	109%
L2S	5.25	18	2	?	0.007	1.992	216	828	109%
L3A	8	12	4	0.0028	0.0084	4.5008	288	1116	107%
L3S	8	12	3	?	0.0112	4.5008	216	1332	107%
L4A	12	18	4	0.0028	0.0084	4.5008	432	1764	107%
L4S	12	18	3	?	0.0112	4.5008	324	2088	107%
L5A	16	24	4	0.0028	0.0084	4.5008	576	2664	107%
L5S	16	24	3	?	0.0112	4.5008	432	3096	107%

- Total installed chip count of SVXII + L00 = 3168+108 = 3276
 - Need to not exceed this in order to limit impact on DAQ
- Above example has 3096 installed chips.
- Pixels are attractive: improve pattern recognition, would need accompanying new DAQ.



Some Considerations

- **SVX4 deep sub-micron:**

- 1.1 M\$ estimate for all development and production
 - 2-3 engineers (~2 FTE) for ~ 2 years.
 - Need to start.
- Note, the alternative is 2.5 M\$ for Honeywell production of SVX3 chips

- **Silicon**

- Many manufacturers for rad-hard single sided microstrips.
- Oxygenation.
- Have asked HPK for quotations.
 - Production time would be short
 - Cost $\sim 1.20 \pm 0.15$ M\$
 - Quality would be exceptional
 - **99.9% good strips**
 - **$V_d \geq 700V$**

- **Module production**

- Use all single-sided equivalent modules
 - Stacked for doublet views
- Total of ~1000 single sided modules installed.
 - Actual production requirements are modest.

- **Hybrids**

- Off silicon
 - Use adequate real-estate to make robust, simple, easy to manufacture

- **Mechanical supports**

- Model after CMS: nested cylinders
- INFN collaboration possible



Summary

- The physics case for much more luminosity is very strong.
- Replacing only radiation-damaged layers may not be so smart.
 - More detailed studies are in progress
 - Currently however, it appears that it would likely cost more time than it buys
- A full-replacement is Not a repeat of the Run 2a silicon project.
 - It can very likely be achieved at reasonable cost and low technical risk
 - does not require a new DAQ
 - would have better performance and
 - minimize lost running time while
 - providing a simple upgrade path - e.g. to pixels
- We plan to complete our studies \Rightarrow a proposal this summer.
- But we need to start on a sub-micron SVX4 chip
 - This need is independent of the replacement scenario we will choose
 - If we start now, we'll avoid the only remaining risk of a repeat of Run 2a delays.