

Fermilab

Experiment Electronic Systems Group

CHANNEL LINK TEST BOARD V2.0

XFT
FINDER DESIGN

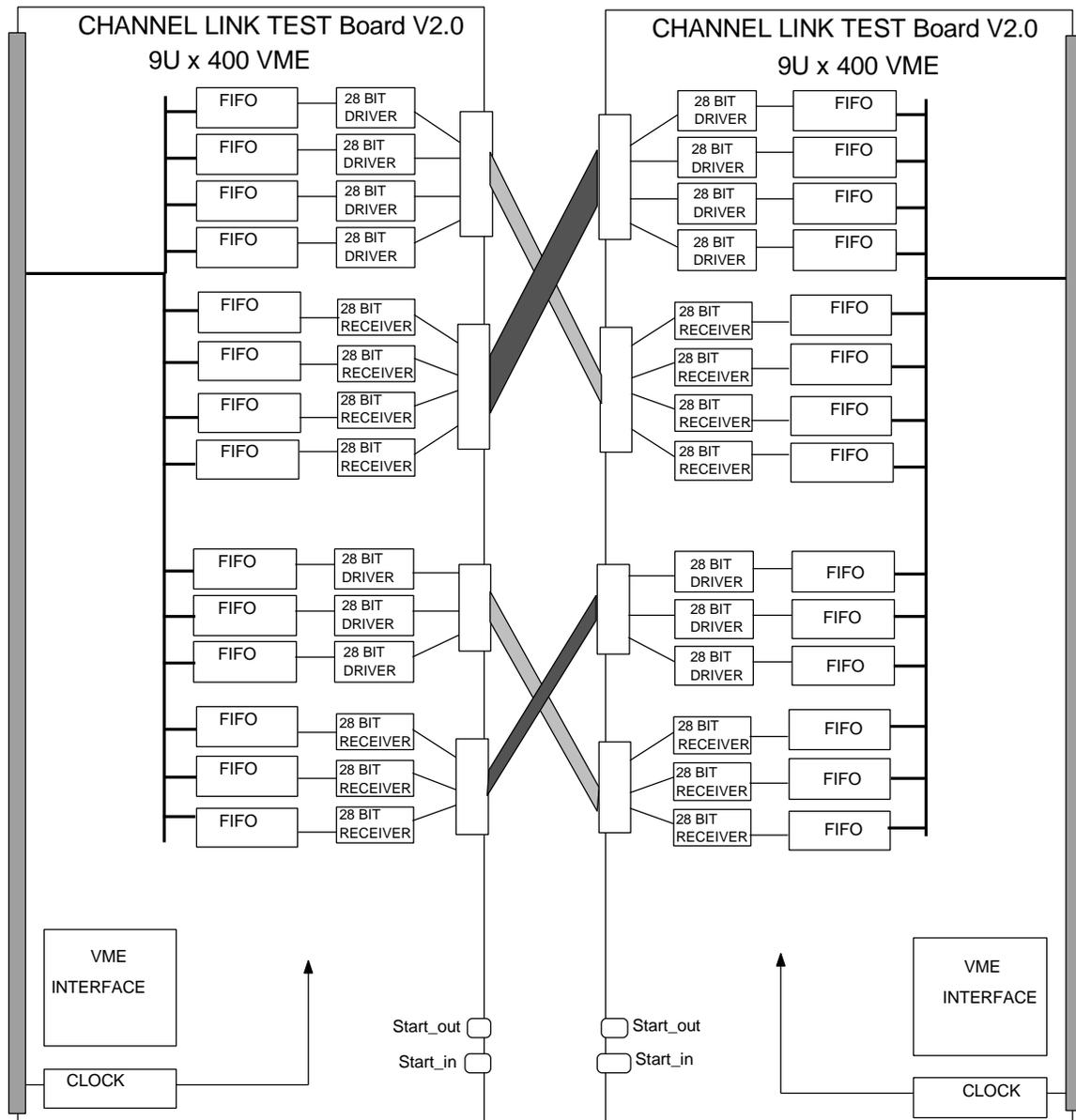
S. Holm

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INTRODUCTION:

This board will give us a method to test the connection between the FINDER board design and the LINKER board design. These boards will simulate a FINDER board when testing a LINKER board and also simulate a LINKER board when testing a FINDER board. These boards will be used to validate the National Semiconductor DS90CR281/282 28-bit Channel Links used on the Finder - Linker boards prior to installation in the system.

The following is a block diagram of the Channel Link test board design. Data is clocked into the channel links at a 33ns rate. Maximum cable length is less than 3 meters.



The blocks perform the following functions:

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FIFOs- The FIFOs will be read/writeable through VME and will be used to test the data path through the channel link. The FIFOs are available in sizes up to 16K. Currently we are using FIFOs that are 1K deep.

CLOCK - Onboard 30M Hz. Oscillator.

VME INTERFACE- The Interface will contain all necessary logic for interfacing with the rest of the system along with controlling functions within the FIFOs.

VME interface design

The VME interface for the test board is adapted from the VME SLAVE INTERFACE design done by T. Shaw.

Memory Map - Channel Link Test Board

YY00 0000 Diagnostic Register (32 bits) (R/W)

YY00 0004 Control (R/W)

<u>Bit</u>	<u>Function</u>
0	Software Reset
1	Dummy - Read Strobe
2	Dummy - Write Strobe
3	Enable - Start out
4	Enable - Start in
5	Enable - Receiver
6	Backplane CDF_Signal Enable

YY00 0010 FIFO Full Flag Register (**Read only**)

These are inverted signals a “high” means the fifo is not full. The full flag is updated on a WCLK signal.

<u>Bit</u>	<u>Function</u>
0	FIFO 1 Full* Flag
1	FIFO 2 Full* Flag
2	FIFO 3 Full* Flag
3	FIFO 4 Full* Flag
4	FIFO 5 Full* Flag
5	FIFO 6 Full* Flag
6	FIFO 7 Full* Flag
7	FIFO 8 Full* Flag
8	FIFO 9 Full* Flag
9	FIFO 10 Full* Flag
10	FIFO 11 Full* Flag
11	FIFO 12 Full* Flag
12	FIFO 13 Full* Flag
13	FIFO 14 Full* Flag
31-14	Undefined

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YY00 0014 FIFO Empty Flag Register (**Read only**) *
 These are inverted signals a “high” means the fifo is not empty. The empty flag is updated on a RCLK signal.

<u>Bit</u>	<u>Function</u>
0	FIFO 1 Empty* Flag
1	FIFO 2 Empty* Flag
2	FIFO 3 Empty* Flag
3	FIFO 4 Empty* Flag
4	FIFO 5 Empty* Flag
5	FIFO 6 Empty* Flag
6	FIFO 7 Empty* Flag
7	FIFO 8 Empty* Flag
8	FIFO 9 Empty* Flag
9	FIFO 10 Empty* Flag
10	FIFO 11 Empty* Flag
11	FIFO 12 Empty* Flag
12	FIFO 13 Empty* Flag
13	FIFO 14 Empty* Flag
31-14	Undefined

YY00 0018 Start Transmission Register (**R/W**)

<u>Bit</u>	<u>Function</u>
0	Start Channel Link Pair 1
1	Start Channel Link Pair 2
2	Start Channel Link Pair 3
3	Start Channel Link Pair 4
4	Start Channel Link Pair 5
5	Start Channel Link Pair 6
6	Start Channel Link Pair 7
3-0	Start Channel Link Set A(1-4)
6-3	Start Channel Link Set B(5-7)
6-0	Start Channel Link Sets A & B
31-10	Undefined

YY10 0000 - YY10 007F ID PROM (upper 8 bits)

YY2X XXXX	FIFO 1 Data (26:0) (R/W)
YY3X XXXX	FIFO 2 Data (26:0) (R/W)
YY4X XXXX	FIFO 3 Data (26:0) (R/W)
YY5X XXXX	FIFO 4 Data (26:0) (R/W)
YY6X XXXX	FIFO 5 Data (26:0) (R/W)
YY7X XXXX	FIFO 6 Data (26:0) (R/W)
YY8X XXXX	FIFO 7 Data (26:0) (R/W)
YY9X XXXX	FIFO 8 Data (26:0) (R/W)
YYAX XXXX	FIFO 9 Data (26:0) (R/W)
YYBX XXXX	FIFO 10 Data (26:0) (R/W)
YYCX XXXX	FIFO 11 Data (26:0) (R/W)
YYDX XXXX	FIFO 12 Data (26:0) (R/W)
YYEX XXXX	FIFO 13 Data (26:0) (R/W)
YYFX XXXX	FIFO 14 Data (26:0) (R/W)
	31 - 27 Undefined

BOARD OPERATION

During test mode the FIFOs can be tested by writing/reading them through VME. During RUN mode the driver FIFOs are written to through VME. A VME_WRITE to the “Start Transmission Register” will begin the test. A ‘start’ command will allow the data in the driver FIFOs: to be transmitted out of the driver FIFOs through the channel link drivers, across the cable, through the channel link receivers and into the receiver FIFOs. The data in the receiver FIFOs can then be read through VME and compared to the data transmitted.

TEST(R/W) operation

To write data to a FIFO:

Address the Control Register and reset the module by toggling bit 0 of the control register(bit 0 of CR).

Perform a VME_WRITE to the appropriate FIFO. The write will set the /WE of that FIFO low and then each VME data strobe will load the FIFO by strobing it’s write clock . The Full flag register can be checked for full condition. The flags both empty and full are active low signals.

To read data from a FIFO:

Address the Control Register and toggle bit “1”to perform a dummy read. This will set the FIFO’s empty flag to the correct state. A fifo can not be read if the empty flag is set. The empty flag is updated with the FIFO’s read clock.

Perform a VME_READ to the appropriate FIFO. The read will set the /RE of that fifo low and then each VME data strobe will read data from the FIFO. The Empty flag register can be checked for data.

TRANSMIT/RECEIVE(T/R) operation

To start a T/R operation the Driver’s FIFOs should be loaded and have full flags. The receivers should be empty and have empty flags. A dummy read (Address the Control Register and toggle bit “1”) will be issued to all FIFOs.

The Channel Link clocks are always operating. This means that data is always being transmitted and received by the channel links.

RECEIVER SETUP: A RECEIVE/ signal will enable the tri-state buffers at the output of the Channel Link receivers and also enable the FIFOs for loading when any of the START bits are set in the Start Transmission Register. When receiving data from the same board ‘OR’d combination of all the bits in the start register will enable the /Receive signal. When receiving data from another Channel Link board or a FINDER board the /Receive bit in the control register must be enabled(CS bit 5).

DRIVER SETUP: The START signal will enable a dff to register a logic high signal “d27” which is transmitted to the receiver board on the next rising edge of the channel link’s clock. The signal “d27” is also used to enable the data to be clocked out of the FIFOs with the next rising edge of the same clock. This allows the “d27” signal to be used to alert the receiver section that the next set of data coming is valid data. When the ‘d27’ signal arrives at the receiver it will be registered as a DATA VALID signal which will along with the RECEIVE/ signal enable the tri-state buffers at the output of the channel link’s receiver. This will allow the valid data to be loaded into the receiver FIFOs. When the driver FIFOs are empty the empty flag will reset the “d27” signal which will reset the DATA VALID signal. The receiver’s full flag will also be able to reset the DATA VALID signal. There will be one ‘d27’ signal input to each channel link driver. Each channel link receiver will operate its own “DATA VALID” signal. The FIFO

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pair associated with a channel link pair will receive its write clock signal from the PLL in the channel link receiver which obtains its clock reference from the driver with the data.

The `START_IN` and `START_OUT` signals are used to incorporate more than one Channel Link Test board into a test (testing of the Linker board). The `START_OUT` bit in the control register will have to be set on the board that is issued the start command and the `START_IN` bit in the control register will have to be set on the board that is not issued the start command. The `START_OUT` port will inform the `START_IN` port on the second board to send data to the receiver board (Linker) at the same time as the first driver board.

We have modified the board to include the capability to use a `CDF_halt` and `CDF_B0` signal to start transmission of data through the Channel Link devices. To use this function bit 6 of the CS must be on. A write to the Start register will enable the appropriate Channel Links for transmission which will occur the next `CDF_B0` after a `CDF_Halt` signal. These signals are obtained from the crate backplane and registered on the board with the `CDF_Clock` signal that is also obtained from the backplane.