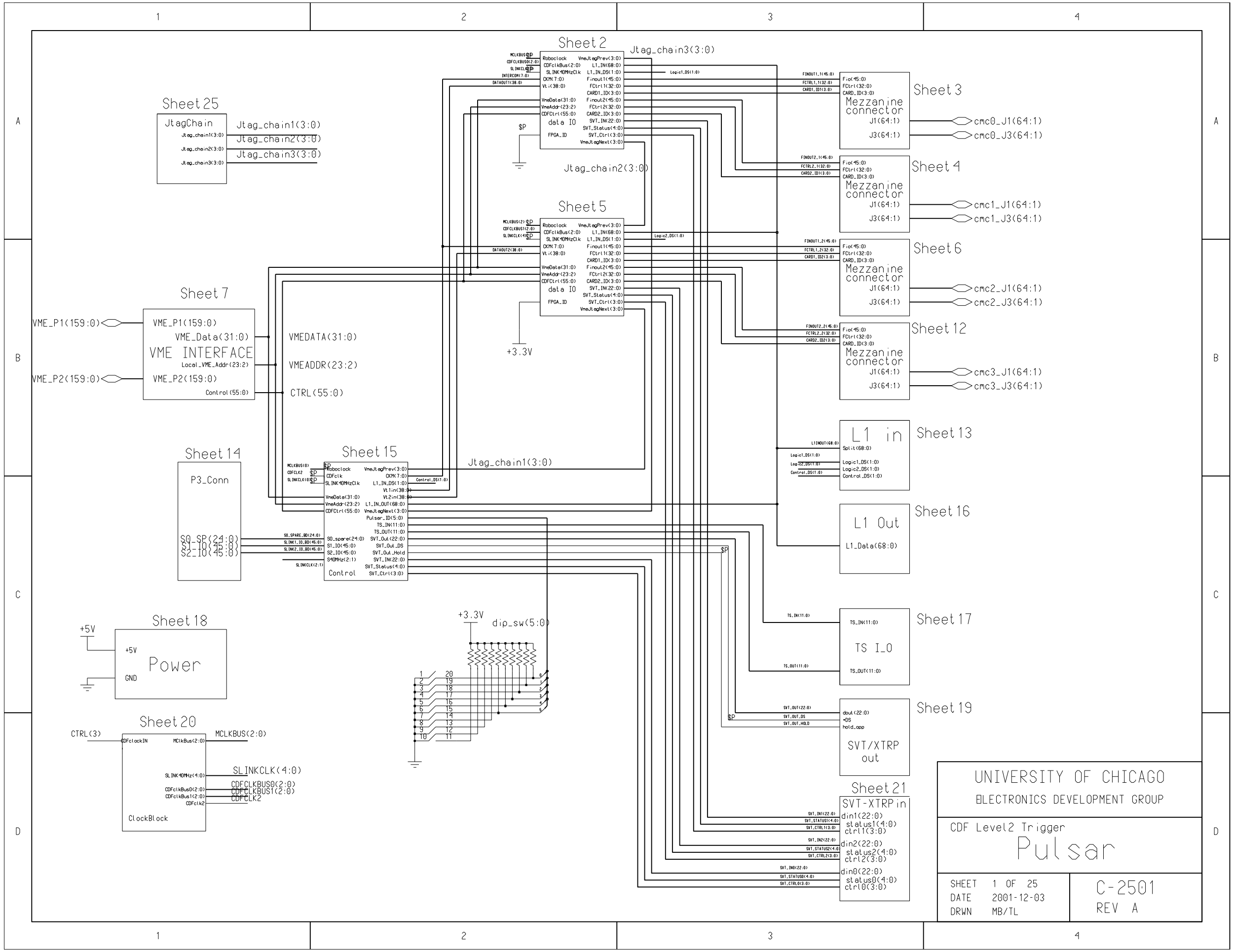
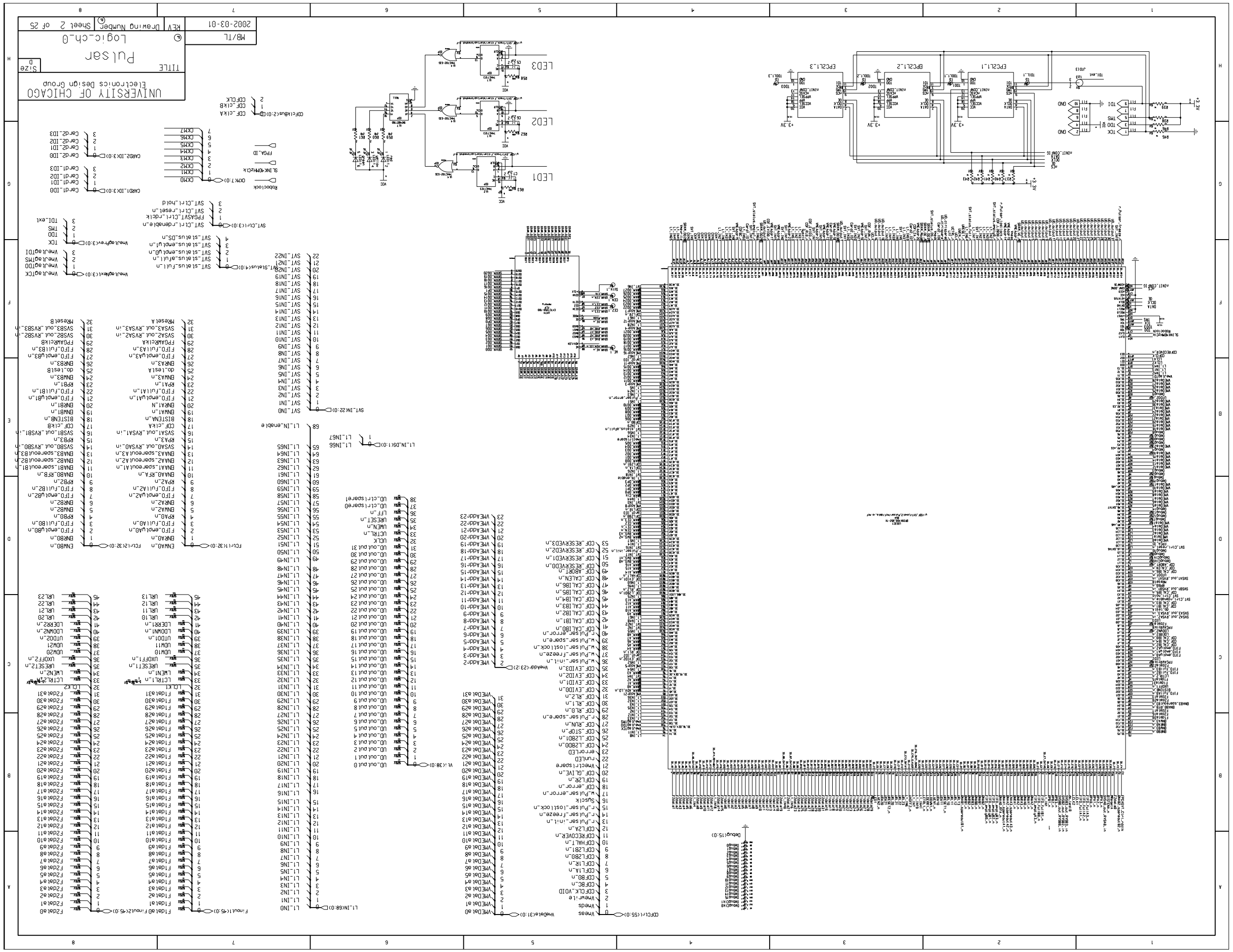
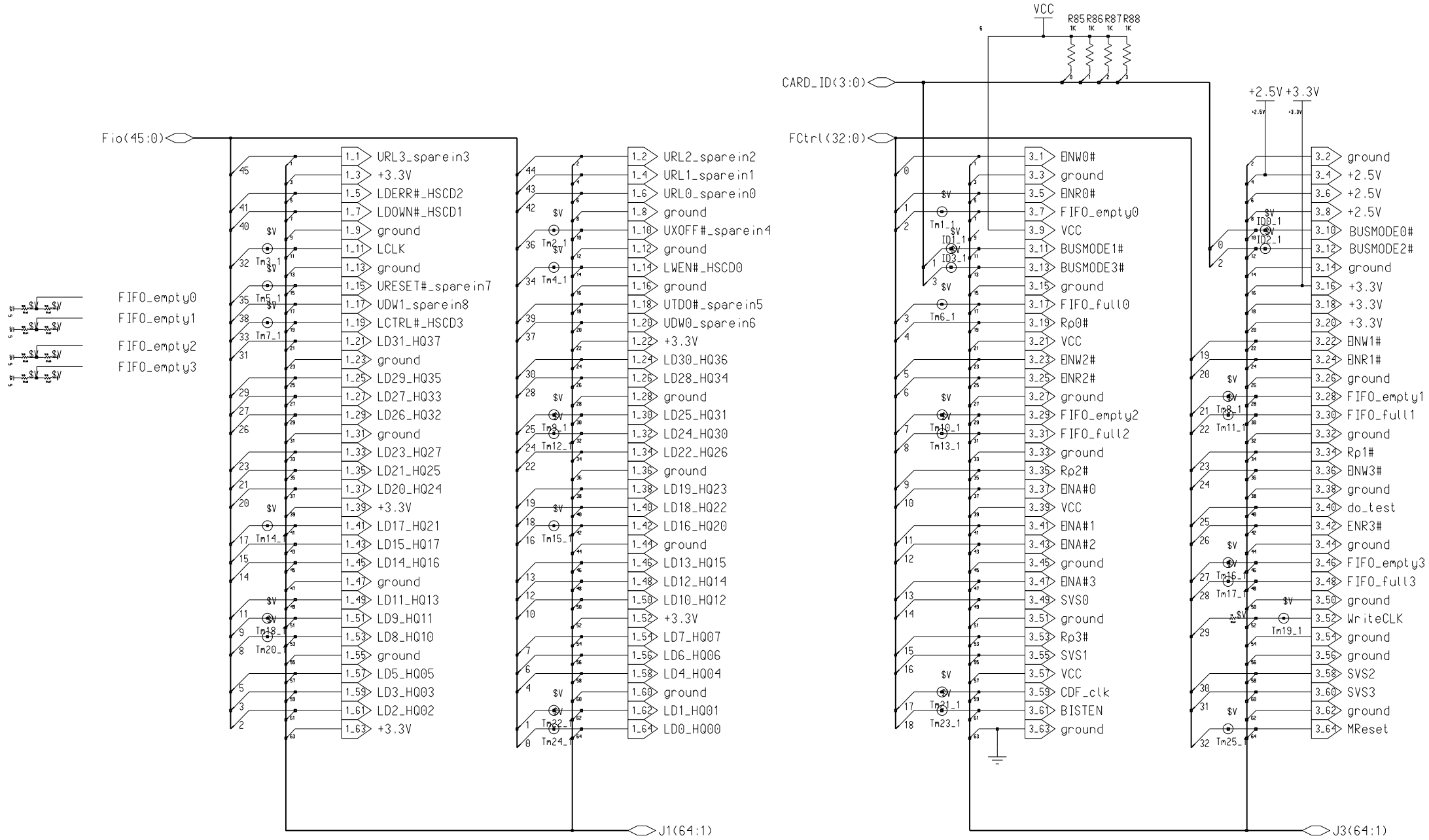

Sheet 2
Roboclock
CDFclkBus(2:0)
SLINK40MHzClk
CKM(7:0)
Vt(38:0)
VmeData(31:0)
VmeAddr(23:2)
CDFCtrl(55:0)
data IO
FPGA_ID
VmeJtagPrev(3:0)
L1_IN(68:0)
L1_IN_DS(1:0)
Finout1(45:0)
FCtrl1(32:0)
CARD1_ID(3:0)
Finout2(45:0)
FCtrl2(32:0)
CARD2_ID(3:0)
SVT_IN(22:0)
SVT_Status(4:0)
SVT_Ctrl(3:0)
VmeJtagNext(3:0)
Jtag_chain3(3:0)
Jtag_chain2(3:0)
Sheet 25
JtagChain
Jtag_chain1(3:0)
Jtag_chain2(3:0)
Jtag_chain3(3:0)
Sheet 3
Sheet 4
Sheet 6
Sheet 12
Mezzanine connector
J1(64:1)
J3(64:1)
cmc0_J1(64:1)
cmc0_J3(64:1)
cmc1_J1(64:1)
cmc1_J3(64:1)
cmc2_J1(64:1)
cmc2_J3(64:1)
cmc3_J1(64:1)
cmc3_J3(64:1)
Sheet 5
Sheet 7
VME_P1(159:0)
VME_P2(159:0)
VME INTERFACE
VME_Data(31:0)
Local_VME_Addr(23:2)
Control(55:0)
VMEDATA(31:0)
VMEADDR(23:2)
CTRL(55:0)
+3.3V
Sheet 13
L1 in
Split(68:0)
Logic1_DS(1:0)
Logic2_DS(1:0)
Control_DS(1:0)
Sheet 14
P3_Conn
S0_SP(24:0)
S1_IO(45:0)
S2_IO(45:0)
Sheet 15
Roboclock
CDFclk
SLINK40MHzClk
VmeData(31:0)
VmeAddr(23:2)
CDFCtrl(55:0)
VmeJtagPrev(3:0)
CKM(7:0)
L1_IN_DS(1:0)
Vt1in(38:0)
Vt2in(38:0)
L1_IN_OUT(68:0)
VmeJtagNext(3:0)
Pulser_ID(5:0)
TS_IN(11:0)
TS_OUT(11:0)
S0_spare(24:0)
SVT_Out(22:0)
S1_IO(45:0)
SVT_Out_DS
S2_IO(45:0)
SVT_Out_Hold
S40MHz(2:1)
SVT_IN(22:0)
SVT_Status(4:0)
SVT_Ctrl(3:0)
Control
Jtag_chain1(3:0)
Sheet 16
L1 Out
L1_Data(68:0)
Sheet 17
TS I_O
Sheet 18
+5V
Power
GND
+3.3V
dip_sw(5:0)
Sheet 19
dout(22:0)
+DS
hold_opp
SVT/XTRP out
Sheet 20
CTRL(3)
CDFclockIN
MClkBus(2:0)
MCLKBUS(2:0)
SLINK40MHz(4:0)
SLINKCLK(4:0)
CDFclkBus0(2:0)
CDFclkBus1(2:0)
CDFclk2
CDFCLKBUS0(2:0)
CDFCLKBUS1(2:0)
CDFCLK2
ClockBlock
Sheet 21
SVT-XTRP in
din1(22:0)
status1(4:0)
ctrl1(3:0)
din2(22:0)
status2(4:0)
ctrl2(3:0)
din0(22:0)
status0(4:0)
ctrl0(3:0)
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP
CDF Level2 Trigger
Pulsar
SHEET 1 OF 25
DATE 2001-12-03
DRWN MB/TL
C-2501
REV A


UNIVERSITY OF CHICAGO
Electronics Design Group
TITLE
Pulsar
Size
D
Logic_ch_0
MB/TL
2002-03-01
REV
Drawing Number
Sheet 2 of 25

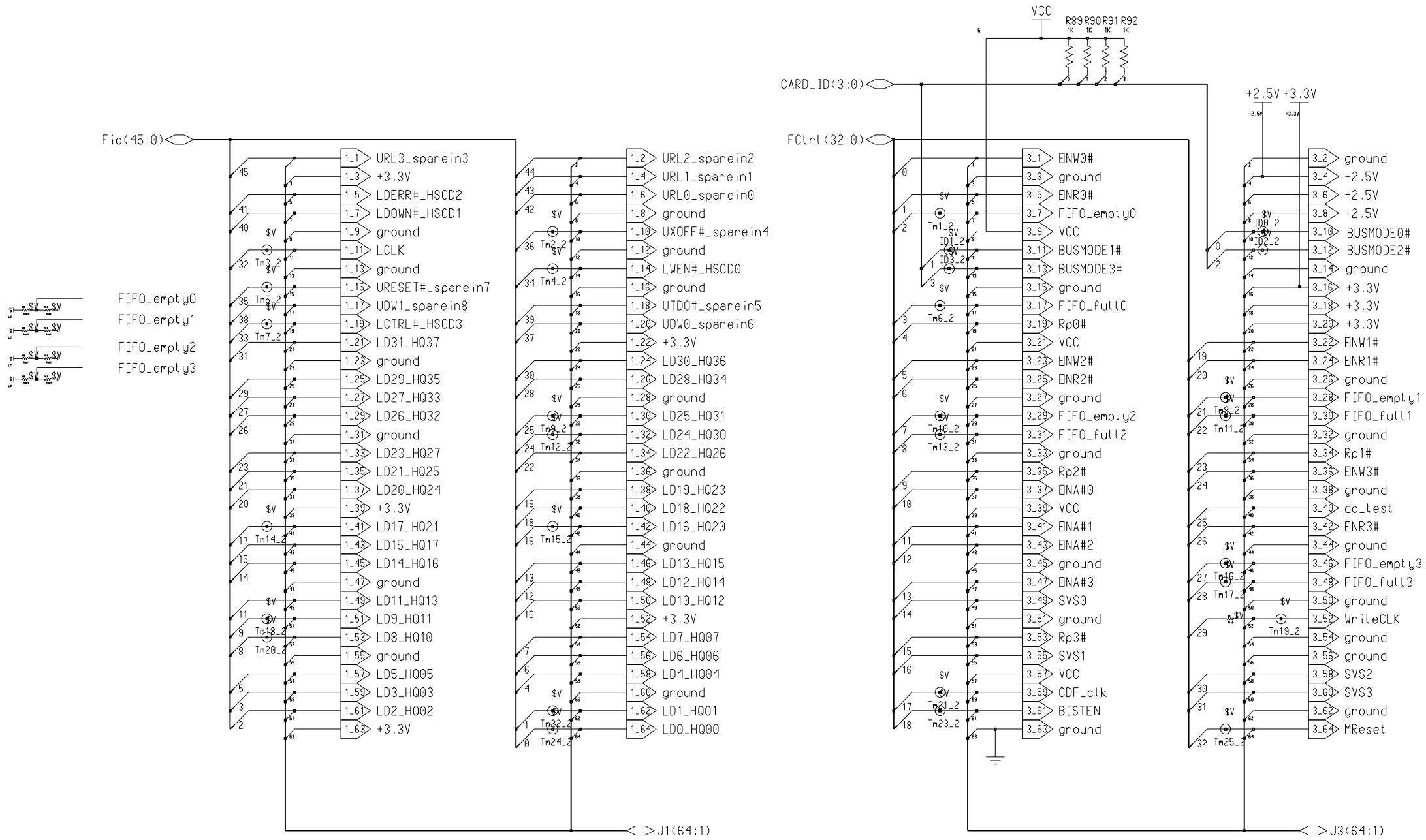


Note: the mezzanine card connector is a receptacle 64-pin surface-mount CMC connector.

Note: FCtrl(32:0) is for optical IO mezzanine card control signals, not for SLINK Fio(45:0) is for SLINK LDC, but also for optical IO mezzanine card signals

Engineer MB/TL	COMPANY NAME Address City	
Drawn by MB/TL		
R&D CHK	TITLE Mezanine_Card_1 Pulsar	Size C
DOC CTRL CHK		
MFG ENGR CHK		
QA CHK		

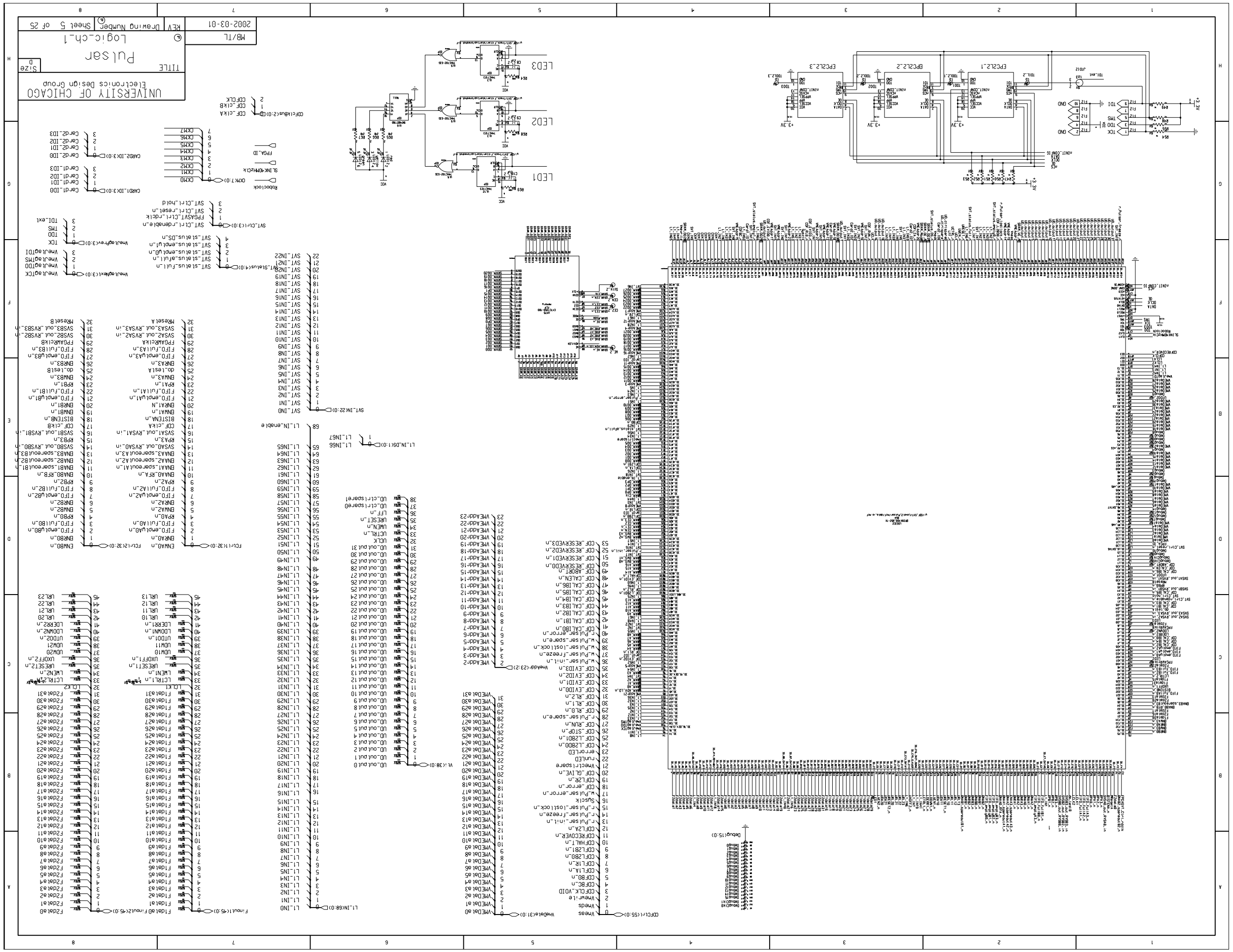
Changed by	Date Changed	Time Changed	REV	Drawing Number	Sheet
MB/TL	March 18, 2002	9:51:06 am	B	2501	3 of 25

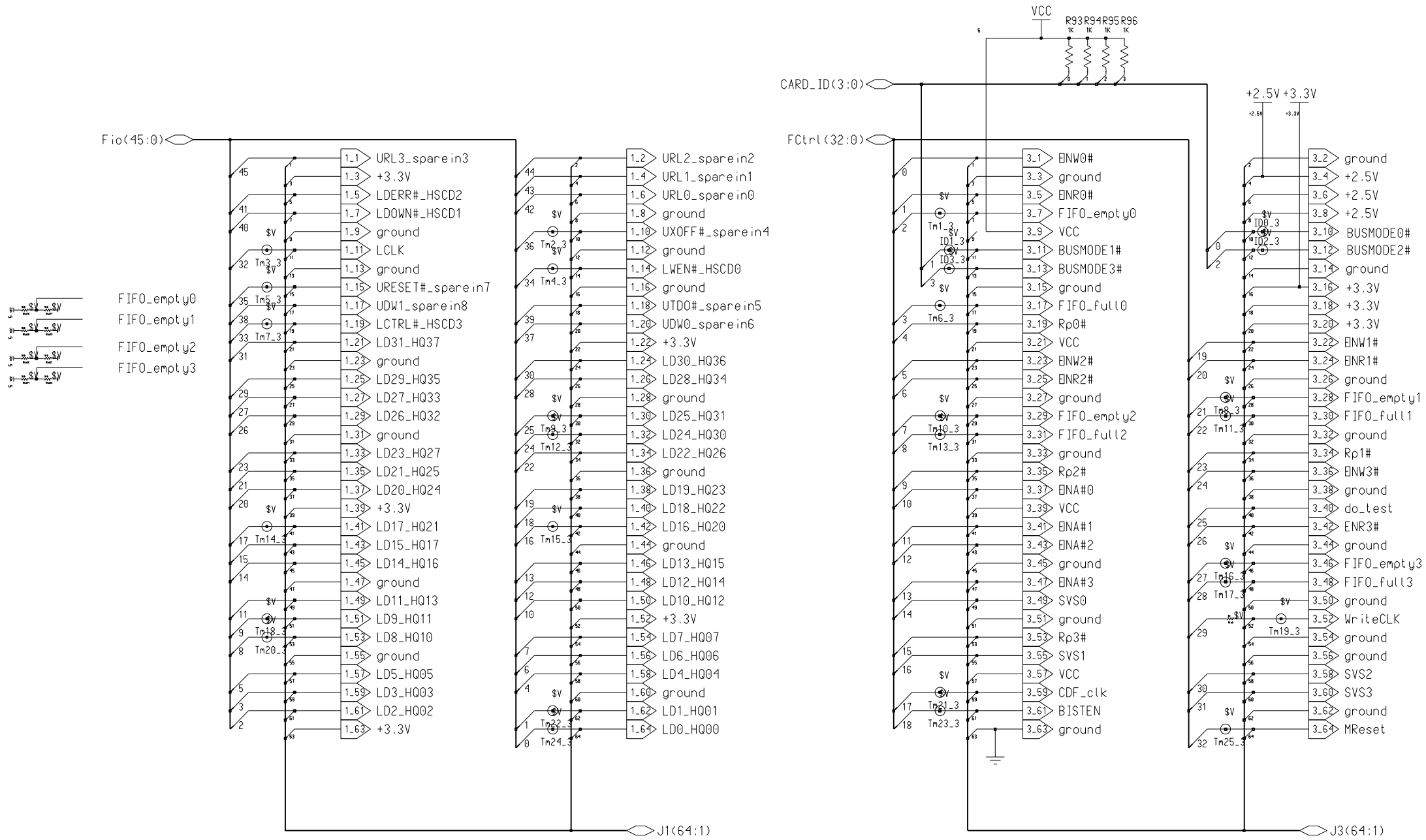


Note: the mezzanine card connector is a receptacle 64-pin surface-mount CMC connector.

Note: FCtrl(32:0) is for optical IO mezzanine card control signals, not for SLINK Fio(45:0) is for SLINK LDC, but also for optical IO mezzanine card signals

Engineer MB/TL	COMPANY NAME Address City		
Drawn by MB/TL			
R&D CHK	TITLE Mezanine_Card_2 Pulsar	Size C	
DOC CTRL CHK			
MFG ENGR CHK			
Changed by MB/TL	Date Changed March 18, 2002	Time Changed 9:51:06 am	QA CHK
REV B	Drawing Number 2501	Sheet 4 of 25	

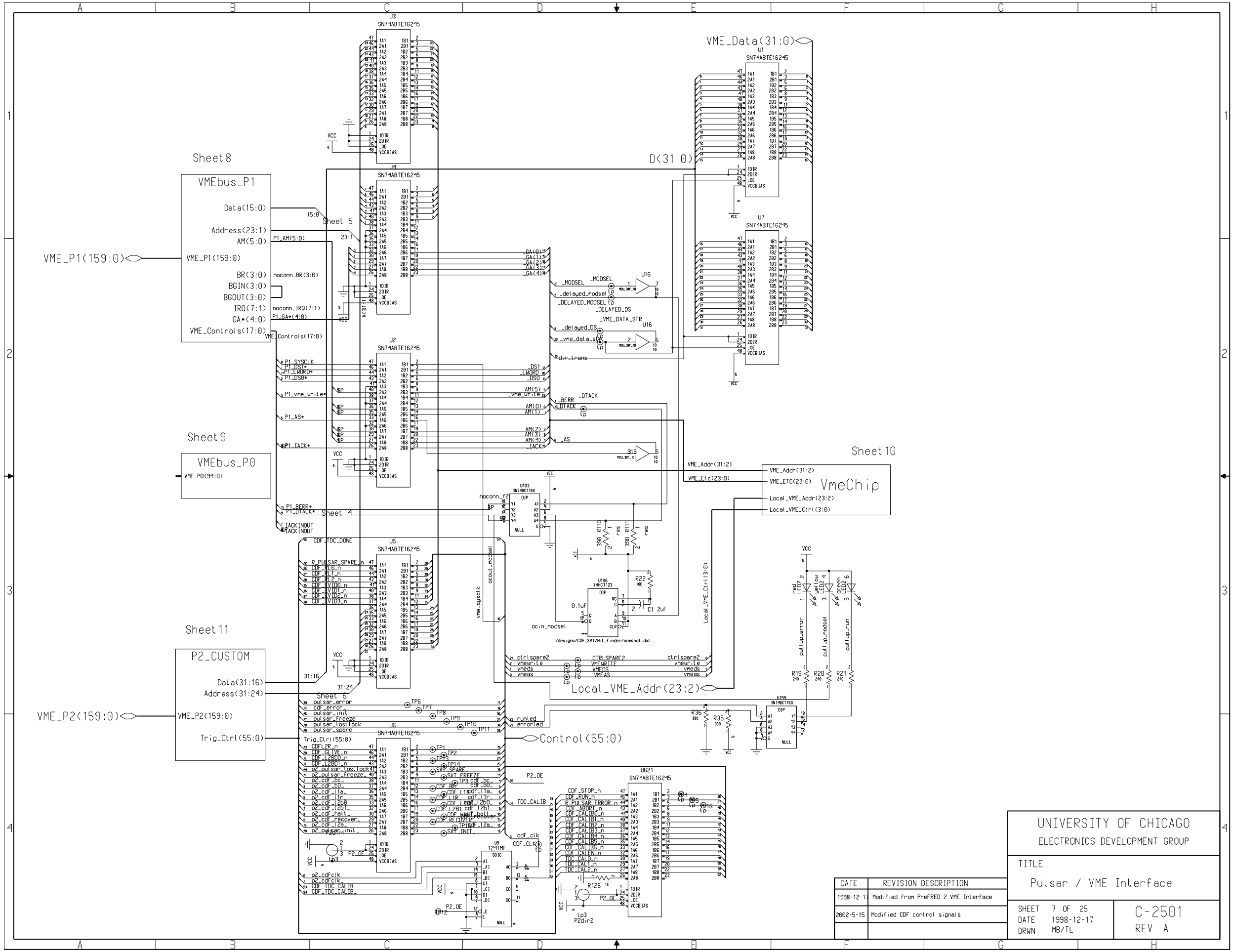

UNIVERSITY OF CHICAGO
Electronics Design Group
TITLE
Pulsar
Size
D
Logic_ch_1
MB/TL
2002-03-01
REV
Drawing Number
Sheet 5 of 25



Note: the mezzanine card connector is a receptacle 64-pin surface-mount CMC connector.

Note: FCtrl(32:0) is for optical IO mezzanine card control signals, not for SLINK
Fio(45:0) is for SLINK LDC, but also for optical IO mezzanine card signals

Engineer MB/TL	COMPANY NAME Address City		
Drawn by MB/TL			
R&D CHK	TITLE Mezanine_Card_3 Pulsar	Size C	
DOC CTRL CHK			
MFG ENGR CHK			
Changed by MB/TL	Date Changed March 18, 2002	Time Changed 9:51:06 am	QA CHK
REV B	Drawing Number 2501	Sheet 6 of 25	



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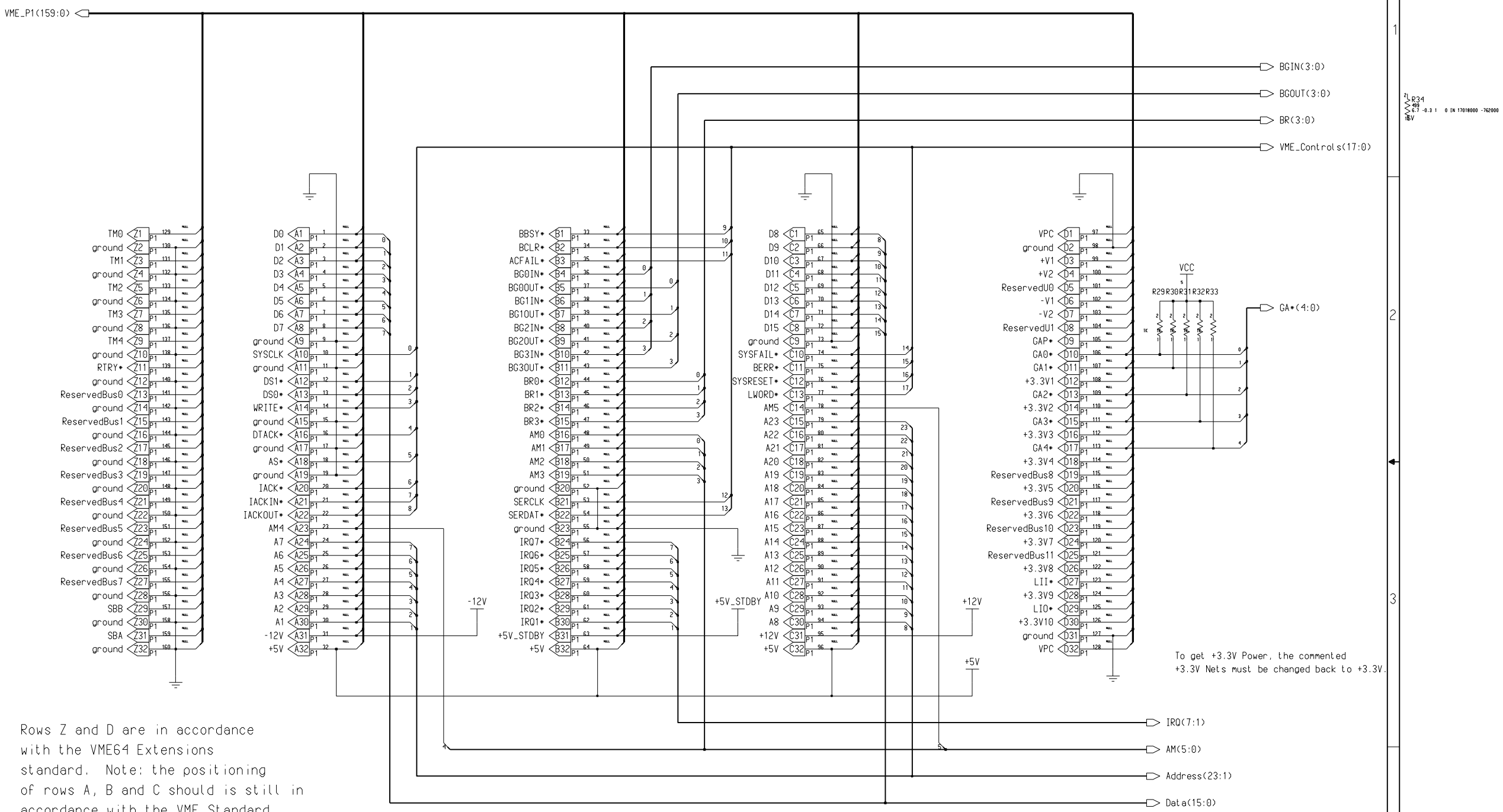
TITLE
Pulsar / VME Interface

DATE	REVISION DESCRIPTION
1998-12-17	Modified from PreFRED 2 VME Interface
2002-5-15	Modified CDF control signals

SHEET 7 OF 25
DATE 1998-12-17
DRWN MB/TL

C-2501
REV A

P1



To get +3.3V Power, the commented +3.3V Nets must be changed back to +3.3V.

Rows Z and D are in accordance with the VME64 Extensions standard. Note: the positioning of rows A, B and C should is still in accordance with the VME Standard.

DATE	REVISION DESCRIPTION
1998-12-11	Copied from PreFRED2 P1 -- MAB/WJA
2002-03-26	modified for Pulsar (MB/TL)

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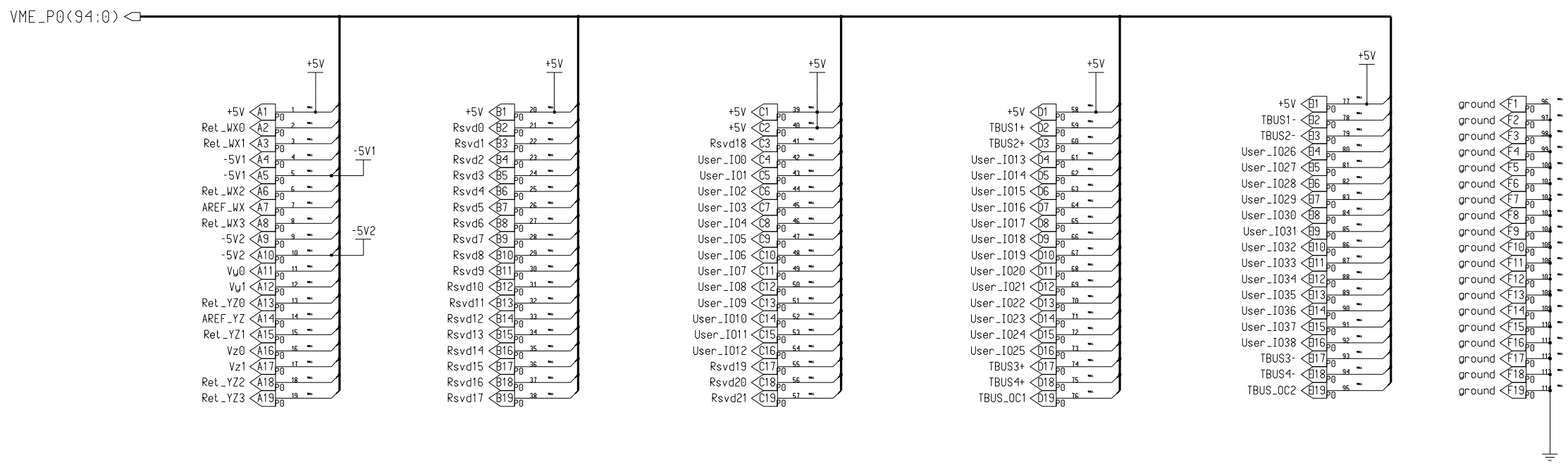
ELECTRONICS DEVELOPMENT GROUP

TITLE
Pulsar VMEbus_P1

SHEET 8 OF 25
DATE 18 Nov 1996
DRWN JW

C-2501
REV A

P0



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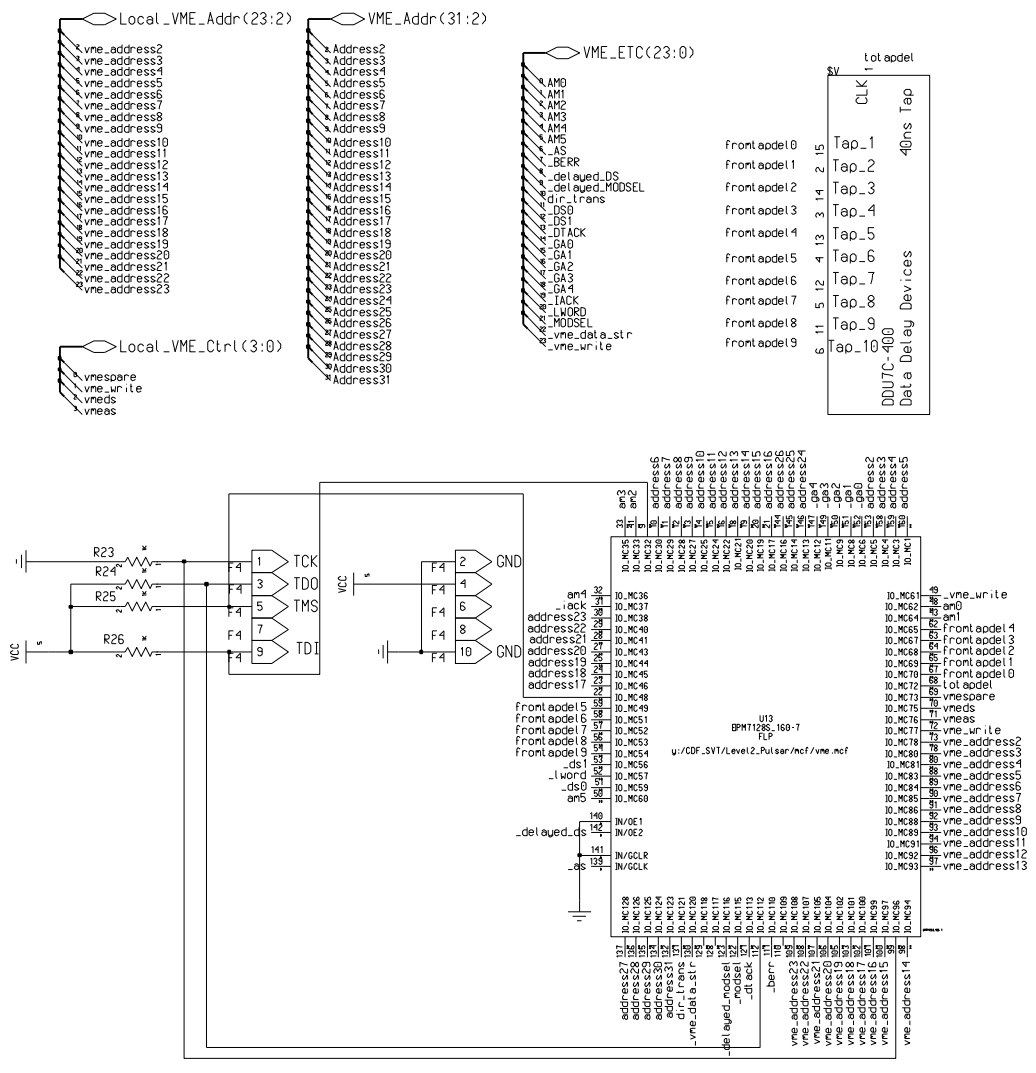
ELECTRONICS DEVELOPMENT GROUP

TITLE
Pulsar VMEbus_P0

DATE	REVISION DESCRIPTION
1998-12-11	Copied from PreFRED2 P0 Rev C -- MAB/WJA

SHEET 9 OF 25
DATE 18 Nov 1996
DRWN JW

C-2501
REV A



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ELECTRONICS DEVELOPMENT GROUP

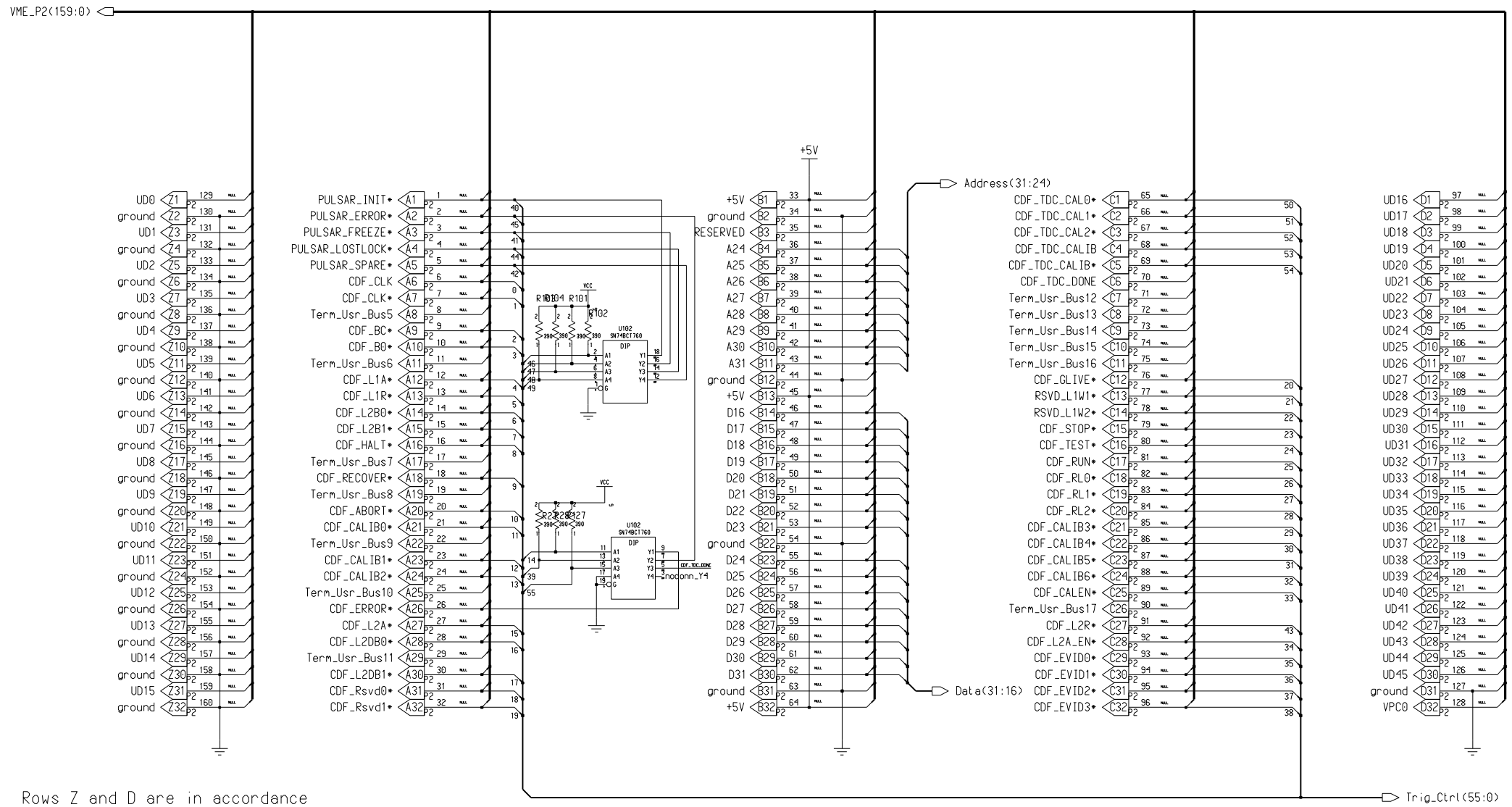
TITLE
Pulsar VME chip

DATE	REVISION DESCRIPTION

SHEET 10 OF 25
DATE 18 Nov 1996
DRWN MB/BA

C-2501
REV A

P2



Rows Z and D are in accordance with the VME64 Extensions standard. Note: the positioning of rows A, B and C should is still in accordance with the VME Standard.

All user-defined signals on P2 are totem-pole TTL excluding:

a. Geographical Addresses are pulled-up/grounded wires

b. 132ns Clock is differential PECL: CLK - CLK*

c. ERROR* is open collector TTL

DATE	REVISION DESCRIPTION
	Started from PreFRED2 P2 Rev C -- MAB/WJA
1998-12-17	Added SVT-specific A1-A5 signals -- WJA
2002-03-28	modifed for Pulsar (MB/TL)

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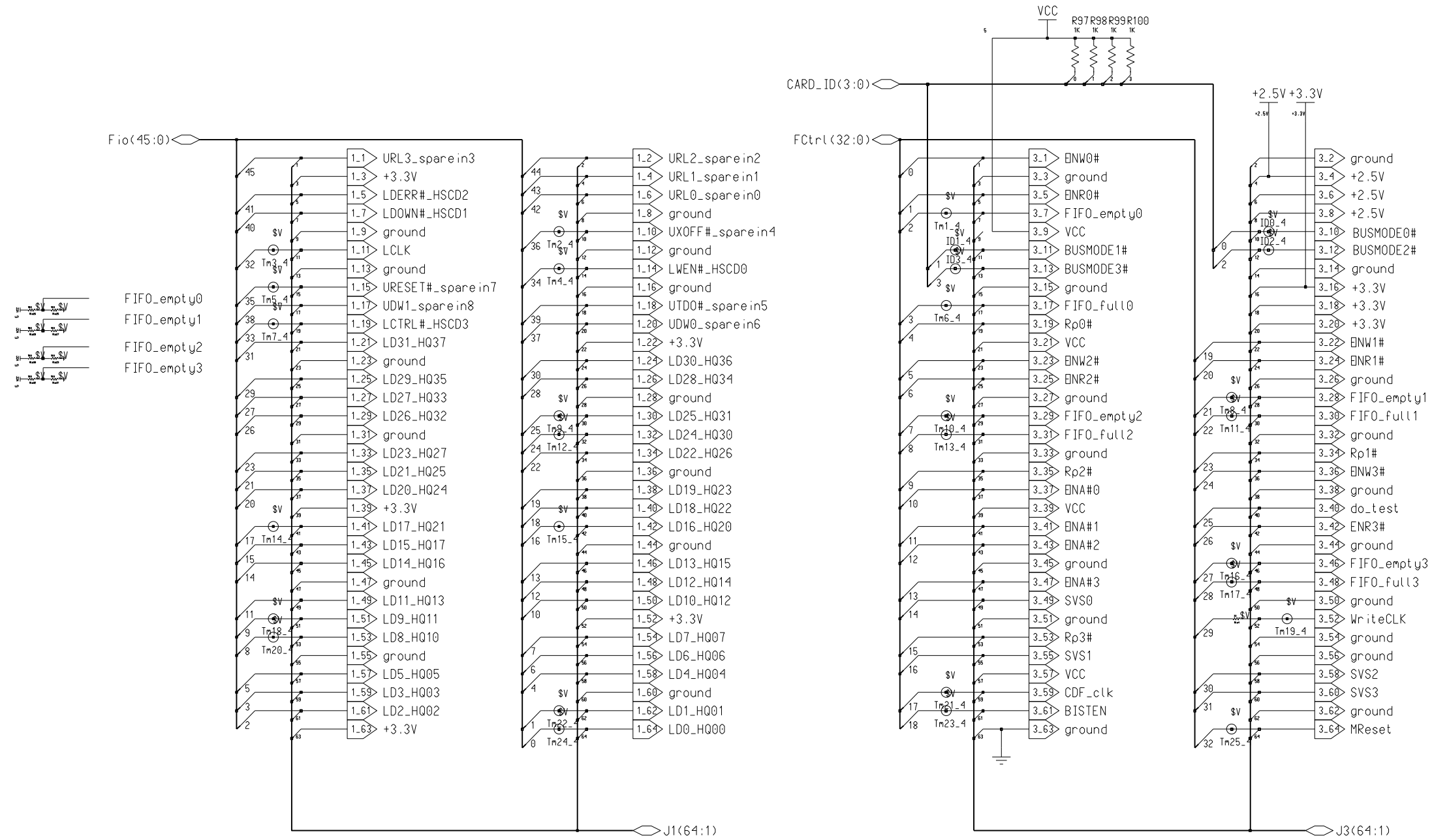
TITLE
Pulsar / VMEbus_P2

SHEET 11 OF 25
DATE 18 Nov 1996
DRWN JW

C- 2501
REV A



Note: the mezzanine card connector is a receptacle 64-pin surface-mount CMC connector.

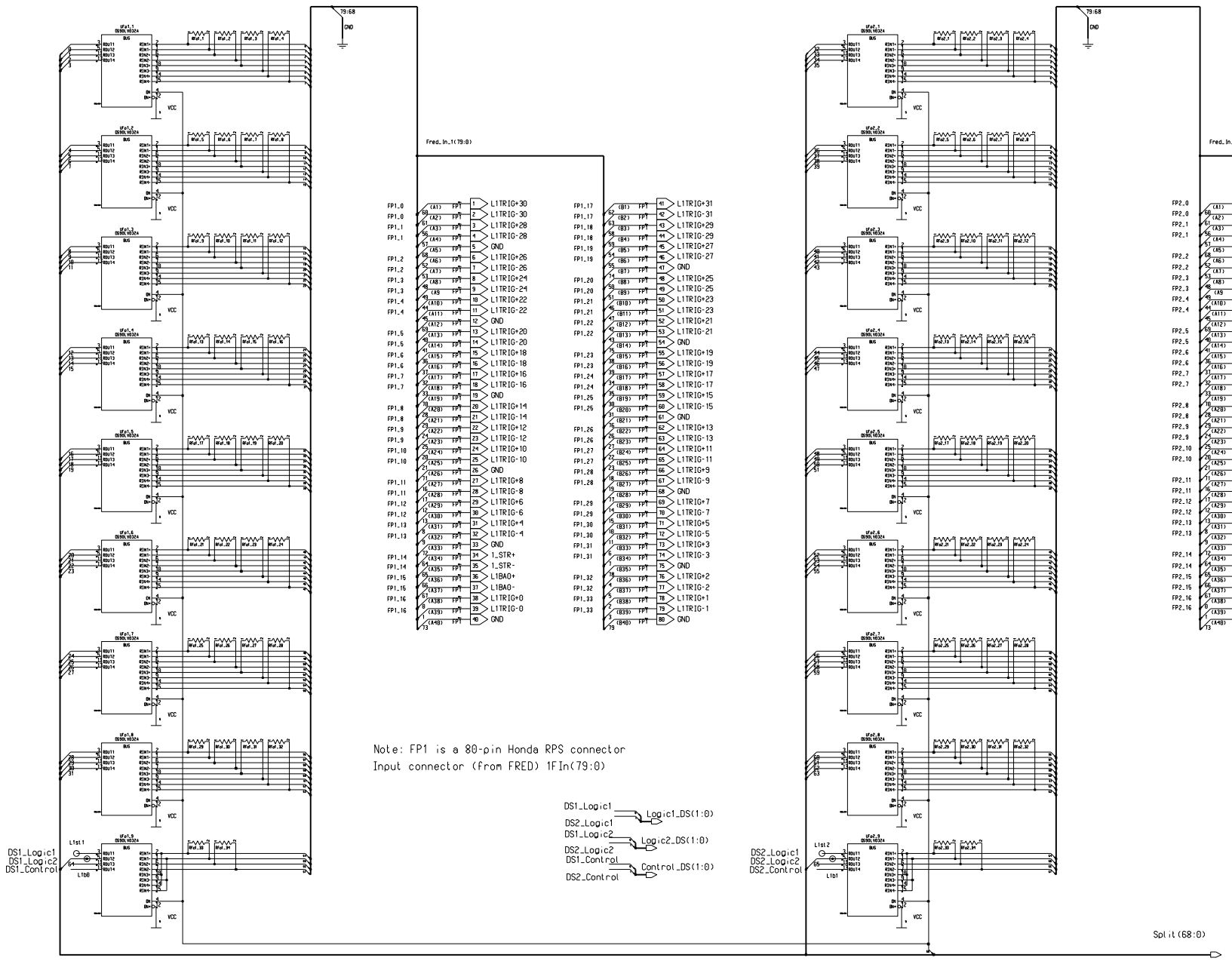
Note: FCtrl(32:0) is for optical IO mezzanine card control signals, not for SLINK Fio(45:0) is for SLINK LDC, but also for optical IO mezzanine card signals

Engineer MB/TL	COMPANY NAME Address City	
Drawn by MB/TL		
R&D CHK	TITLE Mezanine_Card_4 Pulsar	Size C
DOC CTRL CHK		
MFG ENGR CHK		
QA CHK	REV B	Drawing Number 2501

Changed by MB/TL	Date Changed March 18, 2002	Time Changed 9:51:06 am	Sheet 12 of 25

The L1 input signal map is based on Fred inputs on the interface board side. Note that the L1 output connector pin map is based on Fred signals on the Fred side. Need to remap the signals in Firmware for PreFred signals.

the 64 L1 trigger bits are sent into FPGA as L1_IN(63:0), while L1Buffer bits (1:0) are L1_IN(65:64), and strobe 2 and 1 are L1_IN(67:66), and L1_IN(68) is the enable bit.



DATE	REVISION DESCRIPTION
2002-08-16	changed the signal mapping (MB/TL)
2002-07-11	added extra strobes.

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ELECTRONICS DEVELOPMENT GROUP

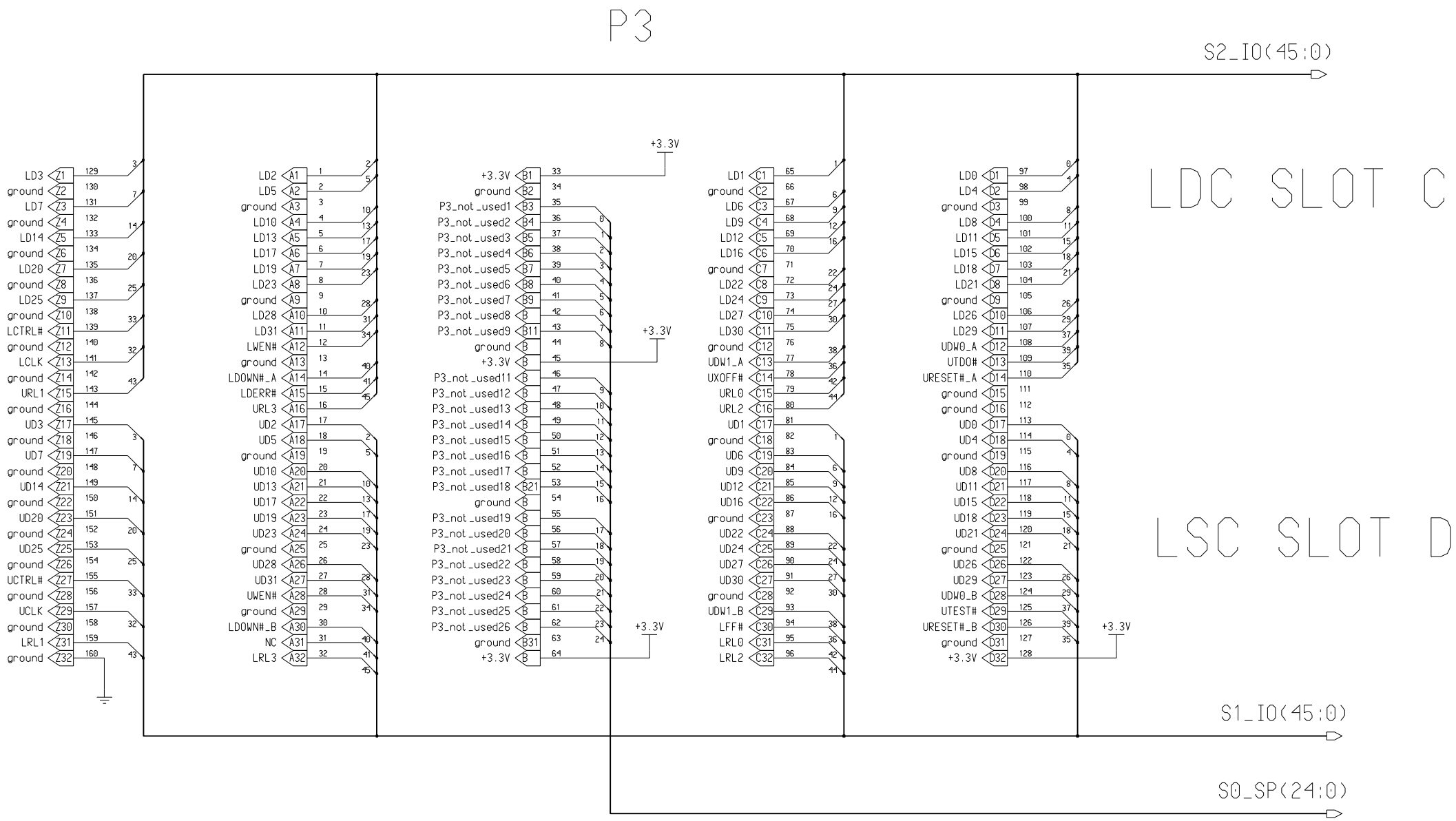
TITLE Pulsar
Level1 Inputs

SHEET 13 OF 25
DATE 2002-03-01
DRWN MB/TL

C- 2501
REV A

5-row P3 connector map to one SLINK LDC and one LSC (use P2-type backplane).
the signals into control FPGA are mapped in such a way to be consistent with the mezzanine card connector, to make life easier in firmware

The 32 data bits are mapped to S_IO(31:0), other signals are mapped to higher bits. the mapping is similar for both LDC and LSC signals.



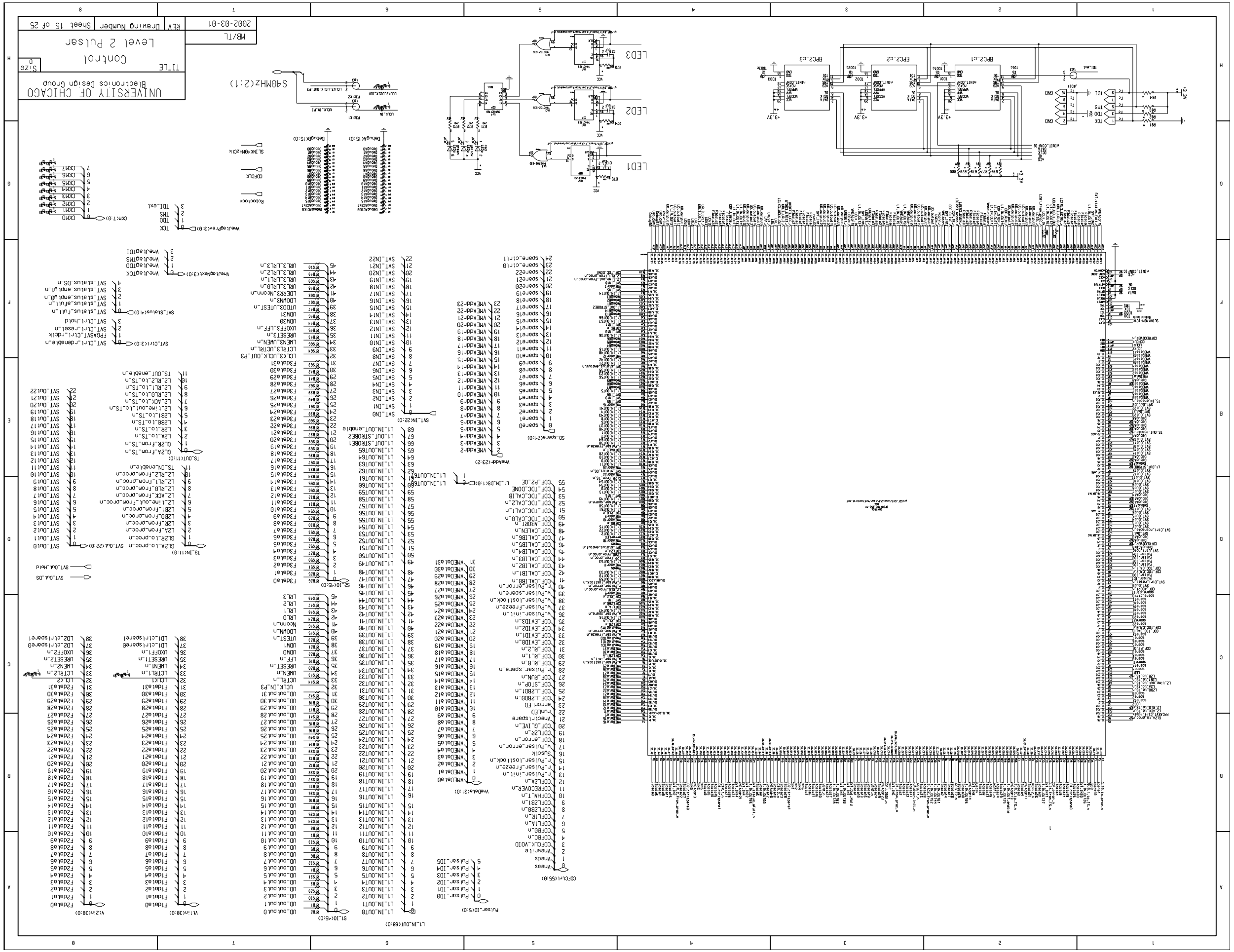
DATE	REVISION DESCRIPTION

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

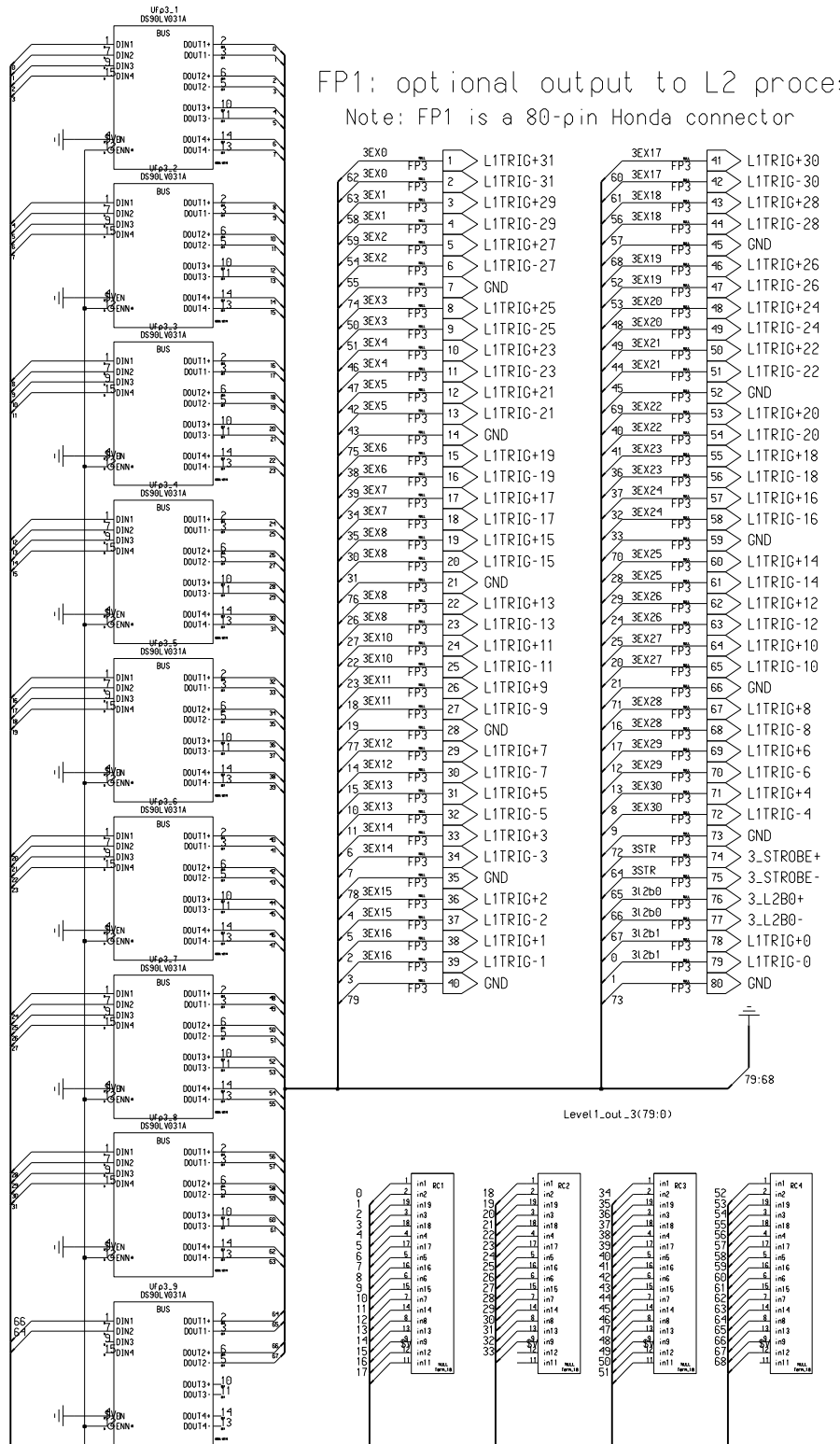
TITLE
Level2 Pulsar / P3

SHEET 14 OF 25
DATE 5/15/2002
DRWN MB/TL

C-2501
REV A


UNIVERSITY OF CHICAGO
Electronics Design Group
TITLE
Control
Level 2 Pulsar
Size
D
MB/TL
2002-03-01
REV
Drawing Number
Sheet 15 of 25
S40MHz(2:1)
LED1
LED2
LED3
BPC2_C1
EPC2_C2
BPC2_C3
Debug0(15:0)
Debug4(15:0)
Robotclock
CPCLK
S_INC40MHzCLK
Vmeladr(23:2)
Vmeldata(31:0)
Pulser_ID(5:0)
L1_IN_OUT(68:0)
S1_IO(45:0)
S2_IO(45:0)
W1_in(38:0)
W2_in(38:0)
TS_IN(11:0)
TS_OUT(11:0)
SVT_DA_DS
SVT_DA_hold
SVT_DA(22:0)
SVT_Cr(3:0)
SVT_Status(4:0)
Vmeldatext(3:0)
Vmeladrex(3:0)
OCR(55:0)
OCR(7:0)
TDI_ext
TDI_Cr(55:0)
TDI_Cr(5:0)
SVT_IN(0)
SVT_IN(22:0)
SVT_OUT(22:0)
SVT_OUT(0)
SVT_OUT(1)
SVT_OUT(2)
SVT_OUT(3)
SVT_OUT(4)
SVT_OUT(5)
SVT_OUT(6)
SVT_OUT(7)
SVT_OUT(8)
SVT_OUT(9)
SVT_OUT(10)
SVT_OUT(11)
SVT_OUT(12)
SVT_OUT(13)
SVT_OUT(14)
SVT_OUT(15)
SVT_OUT(16)
SVT_OUT(17)
SVT_OUT(18)
SVT_OUT(19)
SVT_OUT(20)
SVT_OUT(21)
SVT_OUT(22)
TS_IN_enable_n
TS_OUT_enable_n
L1_IN_OUT_enable
L1_IN_DS(1:0)
L1_IN_DUT(15:0)
L1_IN_OUT(15:0)
L1_OUT_STROBE1
L1_OUT_STROBE2
L1_IN_OUT(15:0)
L1_IN_OUT(15:0)
L1_IN_OUT(15:0)

The L1 input signal map is based on Fred inputs on the interface board side. Note that the L1 output connector pin map is based on Fred signals on the Fred side.
Need to remap the signals in firmware for PreFred signals.
the 64 L1 trigger bits are sent into FPGA as L1_IN(63:0), while L1Buffer bits (1:0) are L1_IN(65:64), and strobe 2 and 1 are L1_IN(67:66), and L1_IN(68) is the enable bit.

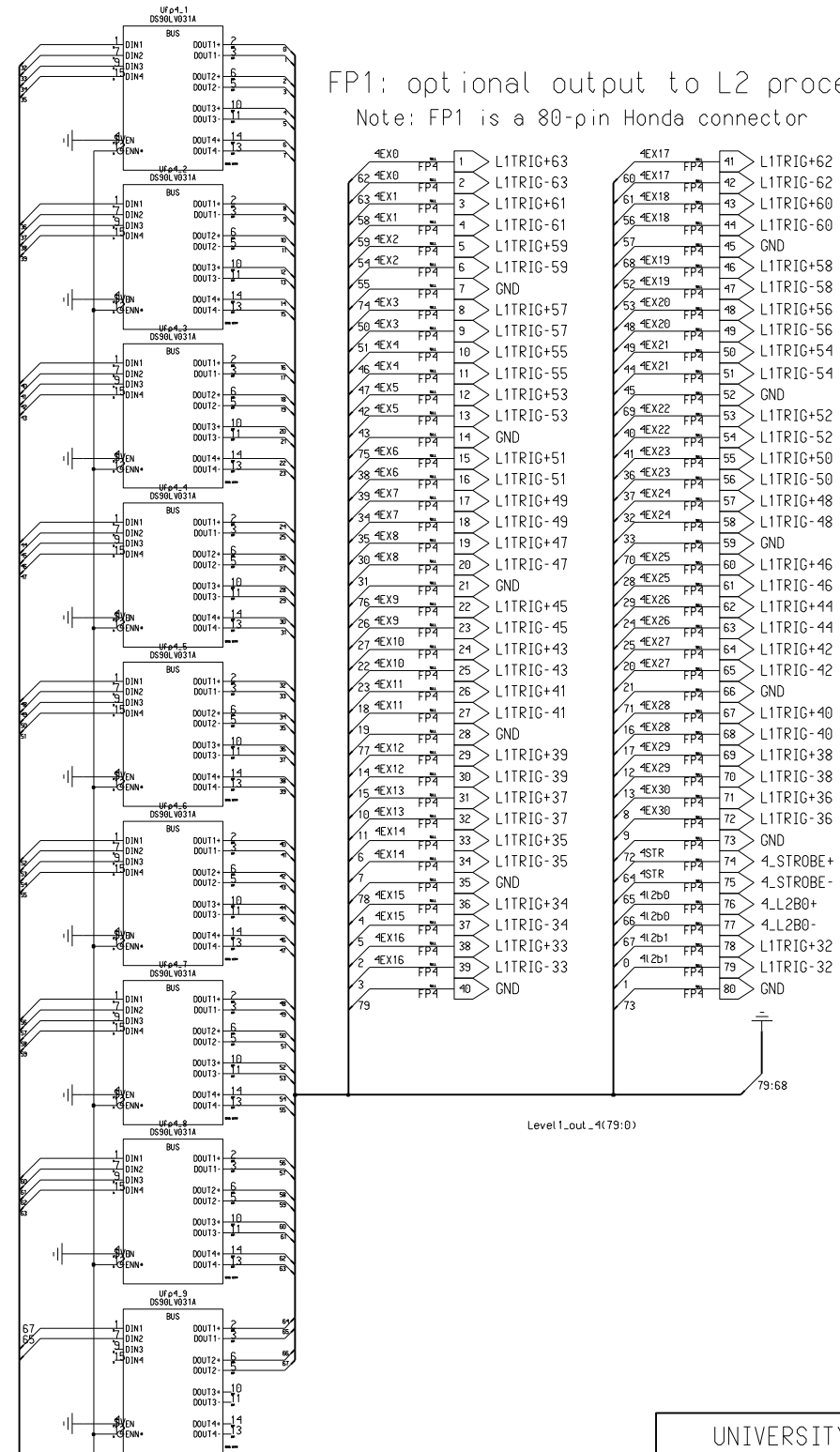


FP1: optional output to L2 processors

Note: FP1 is a 80-pin Honda connector

Pin	Signal	Pin	Signal
1	L1TRIG+31	41	L1TRIG+30
2	L1TRIG-31	42	L1TRIG-30
3	L1TRIG+29	43	L1TRIG+28
4	L1TRIG-29	44	L1TRIG-28
5	L1TRIG+27	45	GND
6	L1TRIG-27	46	L1TRIG+26
7	GND	47	L1TRIG-26
8	L1TRIG+25	48	L1TRIG+24
9	L1TRIG-25	49	L1TRIG-24
10	L1TRIG+23	50	L1TRIG+22
11	L1TRIG-23	51	L1TRIG-22
12	L1TRIG+21	52	GND
13	L1TRIG-21	53	L1TRIG+20
14	GND	54	L1TRIG-20
15	L1TRIG+19	55	L1TRIG+18
16	L1TRIG-19	56	L1TRIG-18
17	L1TRIG+17	57	L1TRIG+16
18	L1TRIG-17	58	L1TRIG-16
19	L1TRIG+15	59	GND
20	L1TRIG-15	60	L1TRIG+14
21	GND	61	L1TRIG-14
22	L1TRIG+13	62	L1TRIG+12
23	L1TRIG-13	63	L1TRIG-12
24	L1TRIG+11	64	L1TRIG+10
25	L1TRIG-11	65	L1TRIG-10
26	L1TRIG+9	66	GND
27	L1TRIG-9	67	L1TRIG+8
28	GND	68	L1TRIG-8
29	L1TRIG+7	69	L1TRIG+6
30	L1TRIG-7	70	L1TRIG-6
31	L1TRIG+5	71	L1TRIG+4
32	L1TRIG-5	72	L1TRIG-4
33	L1TRIG+3	73	GND
34	L1TRIG-3	74	3_STROBE+
35	GND	75	3_STROBE-
36	L1TRIG+2	76	3_L2B0+
37	L1TRIG-2	77	3_L2B0-
38	L1TRIG+1	78	L1TRIG+0
39	L1TRIG-1	79	L1TRIG-0
40	GND	80	GND

Level1_out_3(79:0)



FP1: optional output to L2 processors

Note: FP1 is a 80-pin Honda connector

Pin	Signal	Pin	Signal
1	L1TRIG+63	41	L1TRIG+62
2	L1TRIG-63	42	L1TRIG-62
3	L1TRIG+61	43	L1TRIG+60
4	L1TRIG-61	44	L1TRIG-60
5	L1TRIG+59	45	GND
6	L1TRIG-59	46	L1TRIG+58
7	GND	47	L1TRIG-58
8	L1TRIG+57	48	L1TRIG+56
9	L1TRIG-57	49	L1TRIG-56
10	L1TRIG+55	50	L1TRIG+54
11	L1TRIG-55	51	L1TRIG-54
12	L1TRIG+53	52	GND
13	L1TRIG-53	53	L1TRIG+52
14	GND	54	L1TRIG-52
15	L1TRIG+51	55	L1TRIG+50
16	L1TRIG-51	56	L1TRIG-50
17	L1TRIG+49	57	L1TRIG+48
18	L1TRIG-49	58	L1TRIG-48
19	L1TRIG+47	59	GND
20	L1TRIG-47	60	L1TRIG+46
21	GND	61	L1TRIG-46
22	L1TRIG+45	62	L1TRIG+44
23	L1TRIG-45	63	L1TRIG-44
24	L1TRIG+43	64	L1TRIG+42
25	L1TRIG-43	65	L1TRIG-42
26	L1TRIG+41	66	GND
27	L1TRIG-41	67	L1TRIG+40
28	GND	68	L1TRIG-40
29	L1TRIG+39	69	L1TRIG+38
30	L1TRIG-39	70	L1TRIG-38
31	L1TRIG+37	71	L1TRIG+36
32	L1TRIG-37	72	L1TRIG-36
33	L1TRIG+35	73	GND
34	L1TRIG-35	74	4_STROBE+
35	GND	75	4_STROBE-
36	L1TRIG+34	76	4_L2B0+
37	L1TRIG-34	77	4_L2B0-
38	L1TRIG+33	78	L1TRIG+32
39	L1TRIG-33	79	L1TRIG-32
40	GND	80	GND

Level1_out_4(79:0)

DATE	REVISION DESCRIPTION
2001-04-23	GhostBuster customization from PreFRED
07/11/02	Changed Pin Mapping to FRED(MB/TL)

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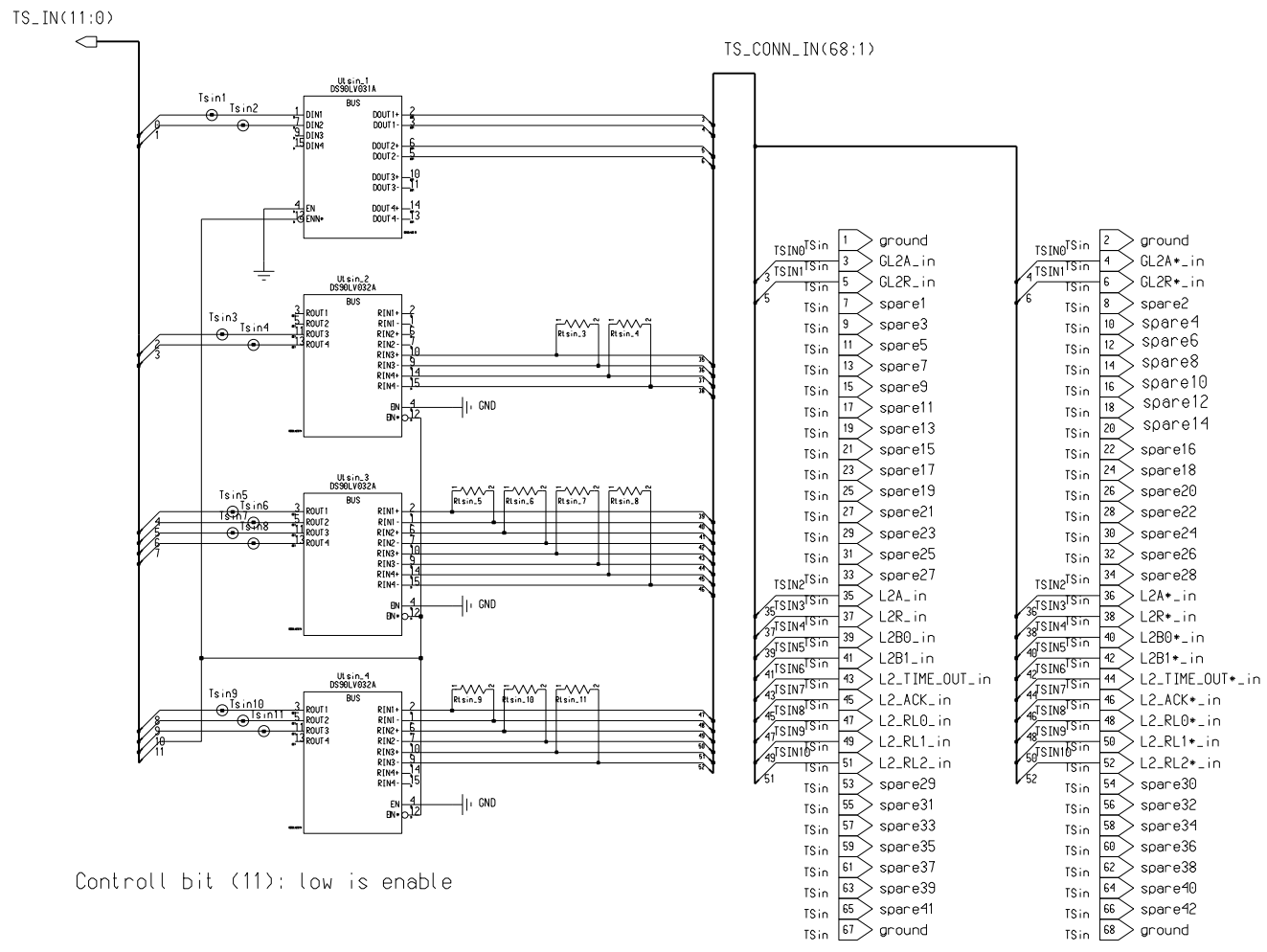
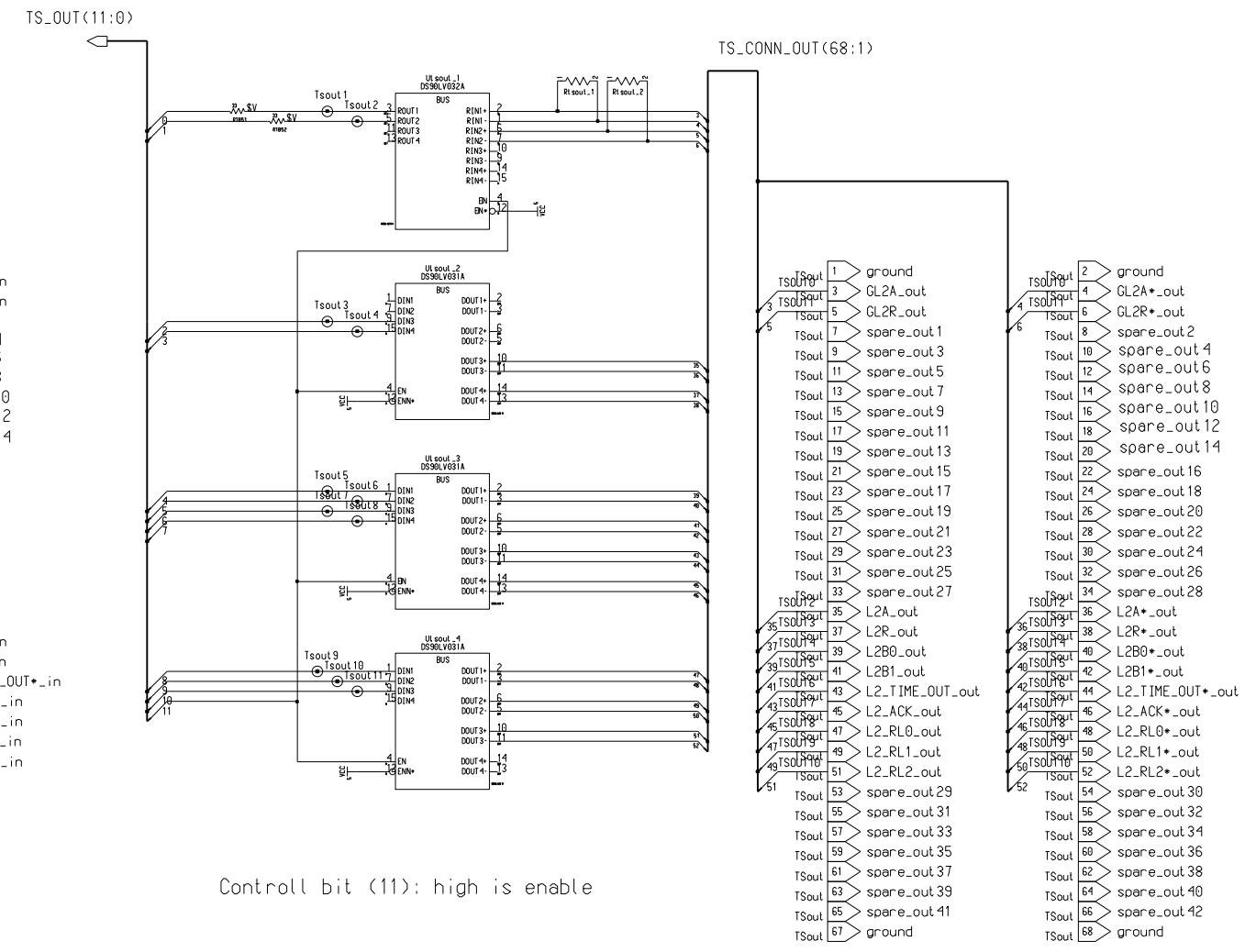
ELECTRONICS DEVELOPMENT GROUP

TITLE Pulsar
Level1 Out

SHEET 16 OF 25
DATE 2001-04-23
DRWN WJA/MAB

C- 2501
REV A





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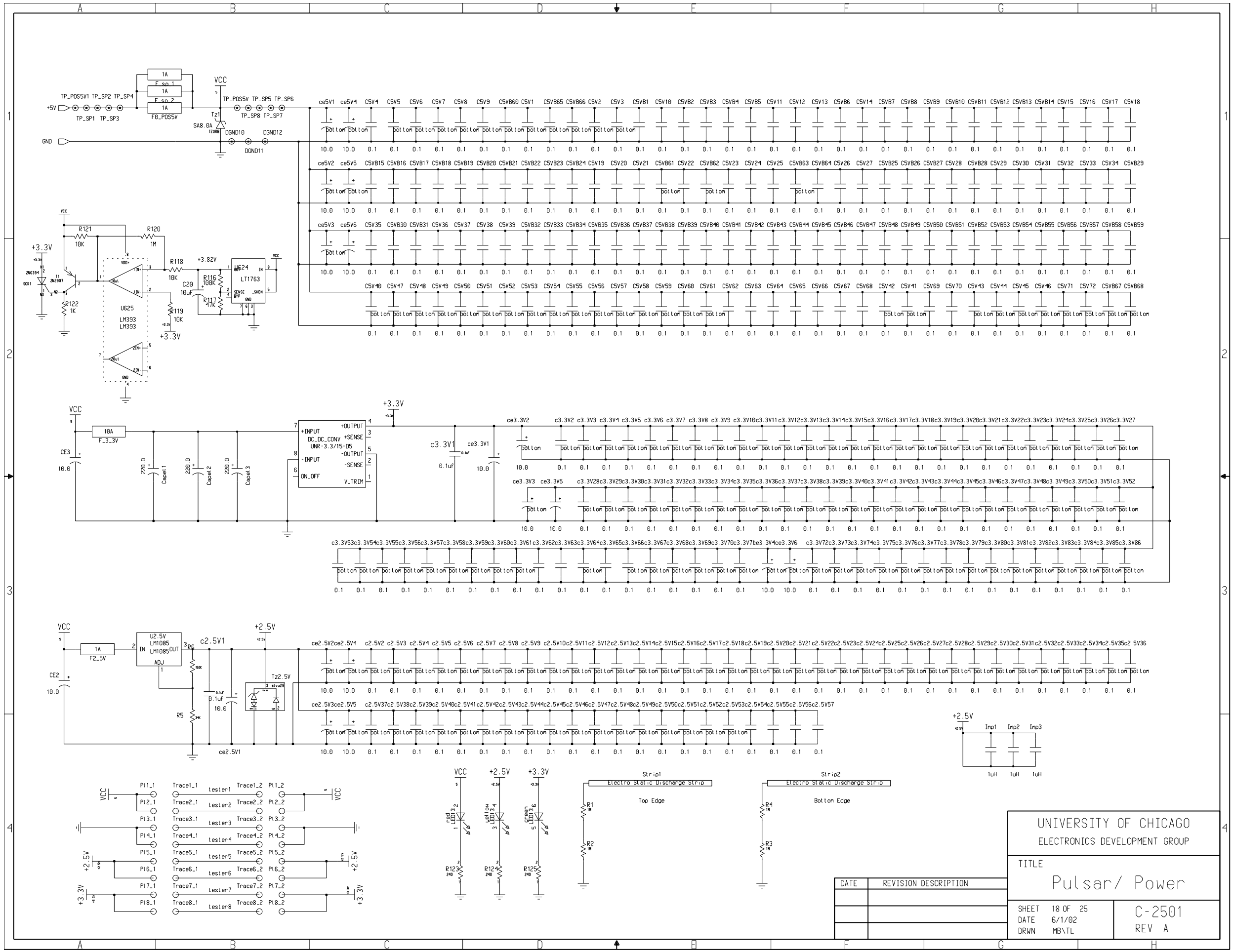

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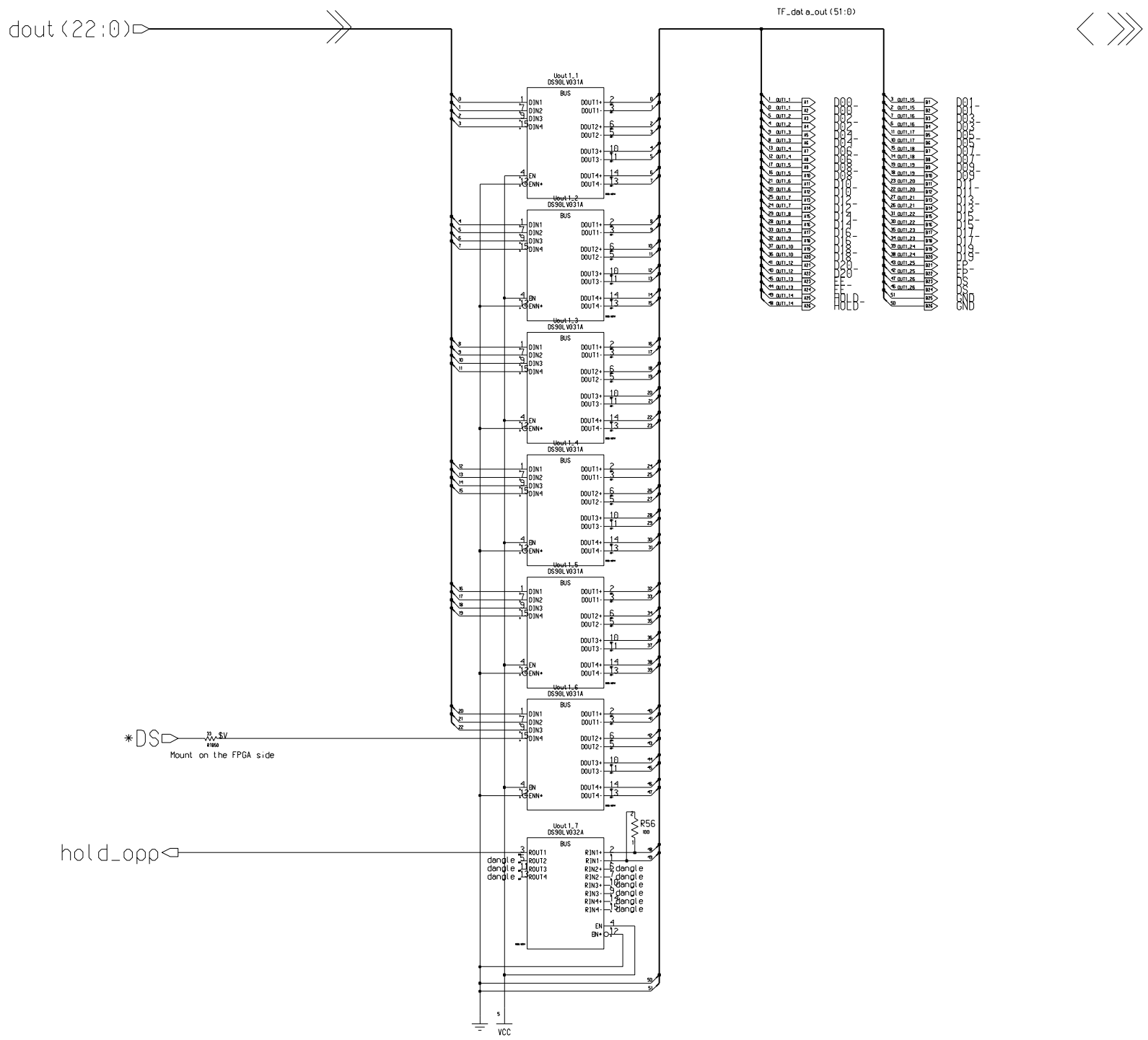
ELECTRONICS DEVELOPMENT GROUP

TITLE
Pulsar/ Power

DATE	REVISION DESCRIPTION

SHEET 18 OF 25
DATE 6/1/02
DRWN MB\TL

C-2501
REV A



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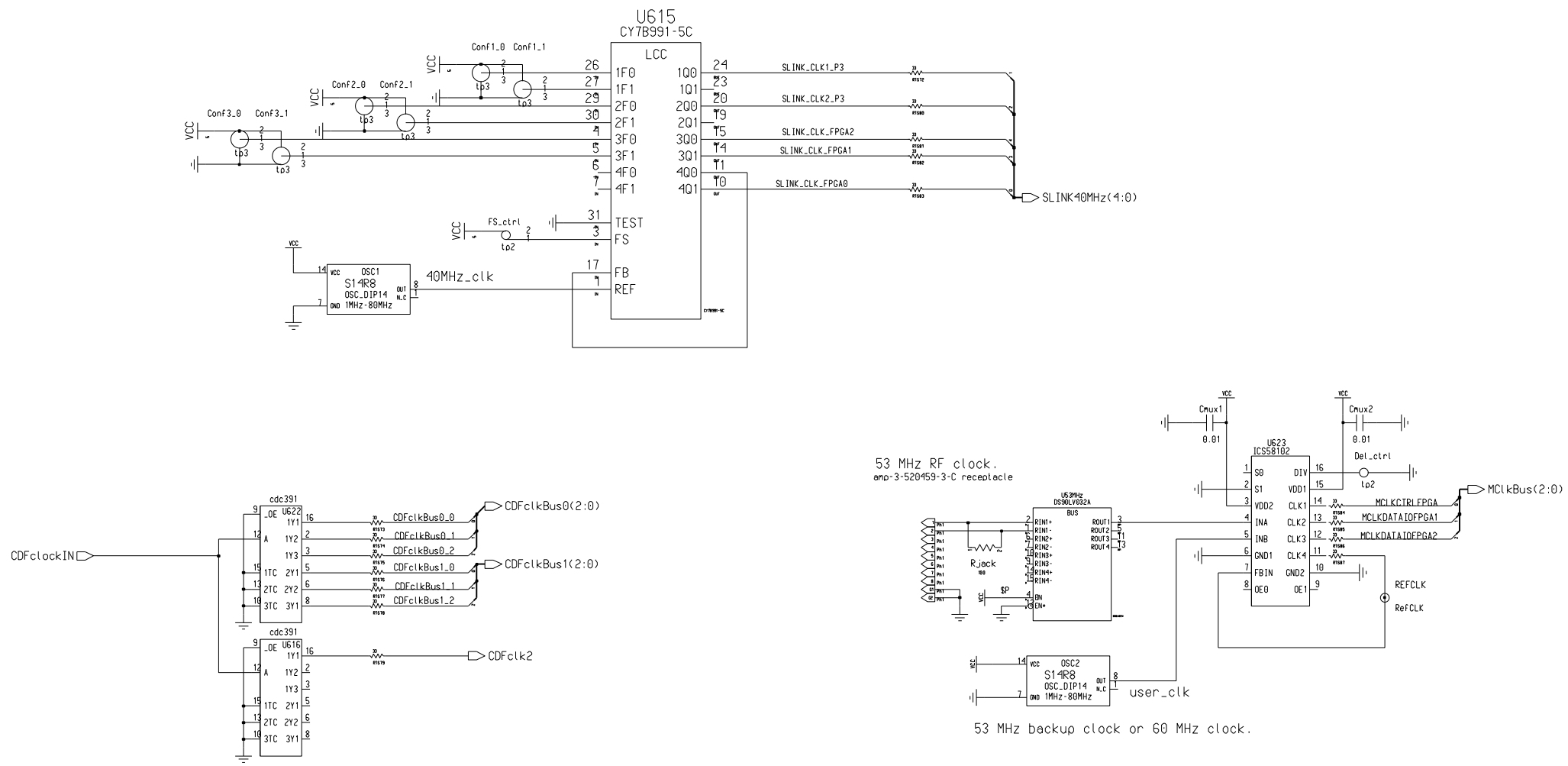
ELECTRONICS DEVELOPMENT GROUP

Pulsar
Front_Panel/DATAOUT

DATE	REVISION DESCRIPTION

SHEET 19 OF 25
DATE 01 Feb 1999
DRWN T. Nakaya

C-2501
REV A



Engineer MB/TL	COMPANY NAME Address City		
Drawn by MB/TL			
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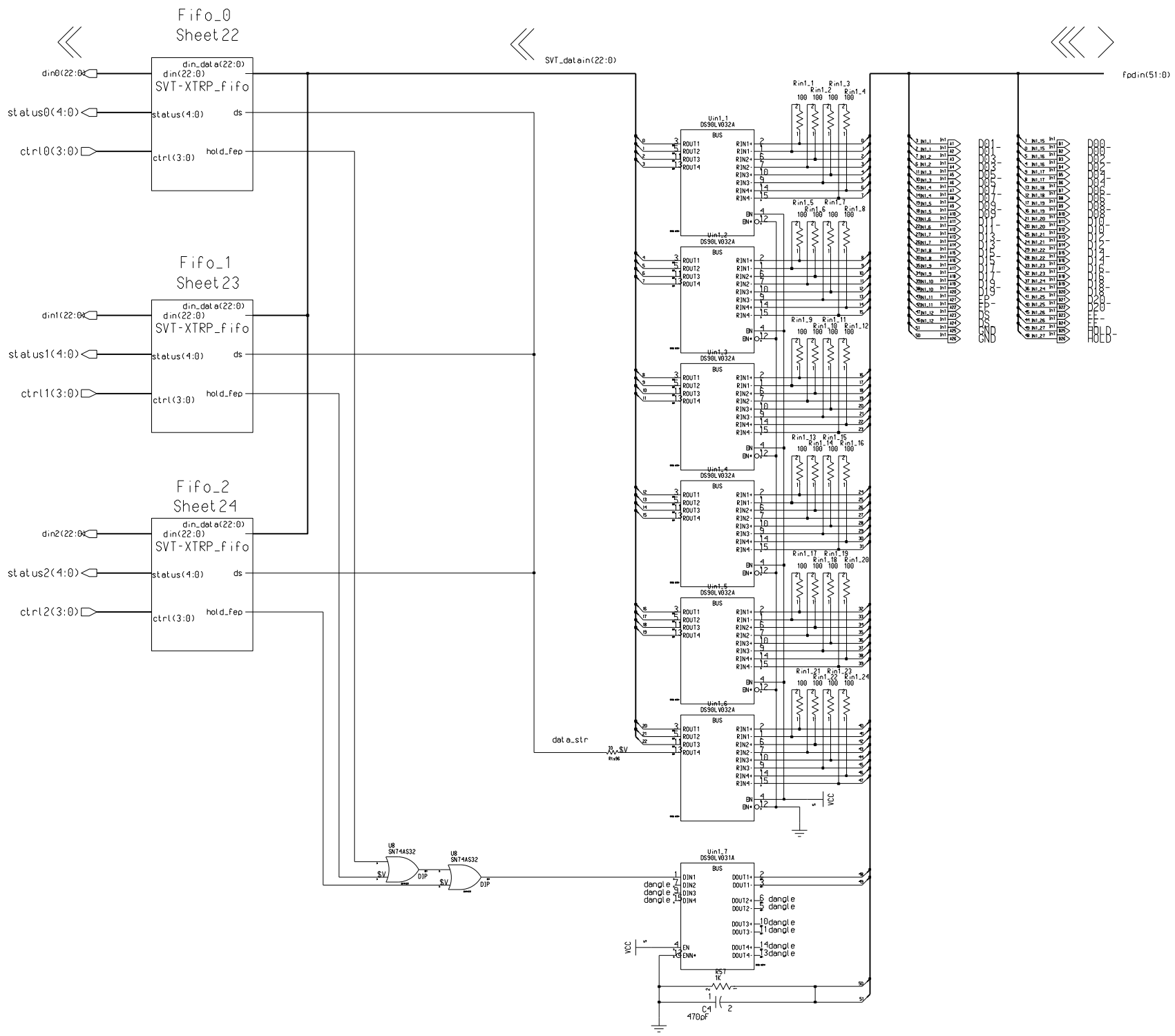
QA CHK	REV	Drawing Number	Sheet 20 of 25

Changed by	Date Changed	Time
bogdan	Wednesday, February 27, 2002	1:23:36 pm



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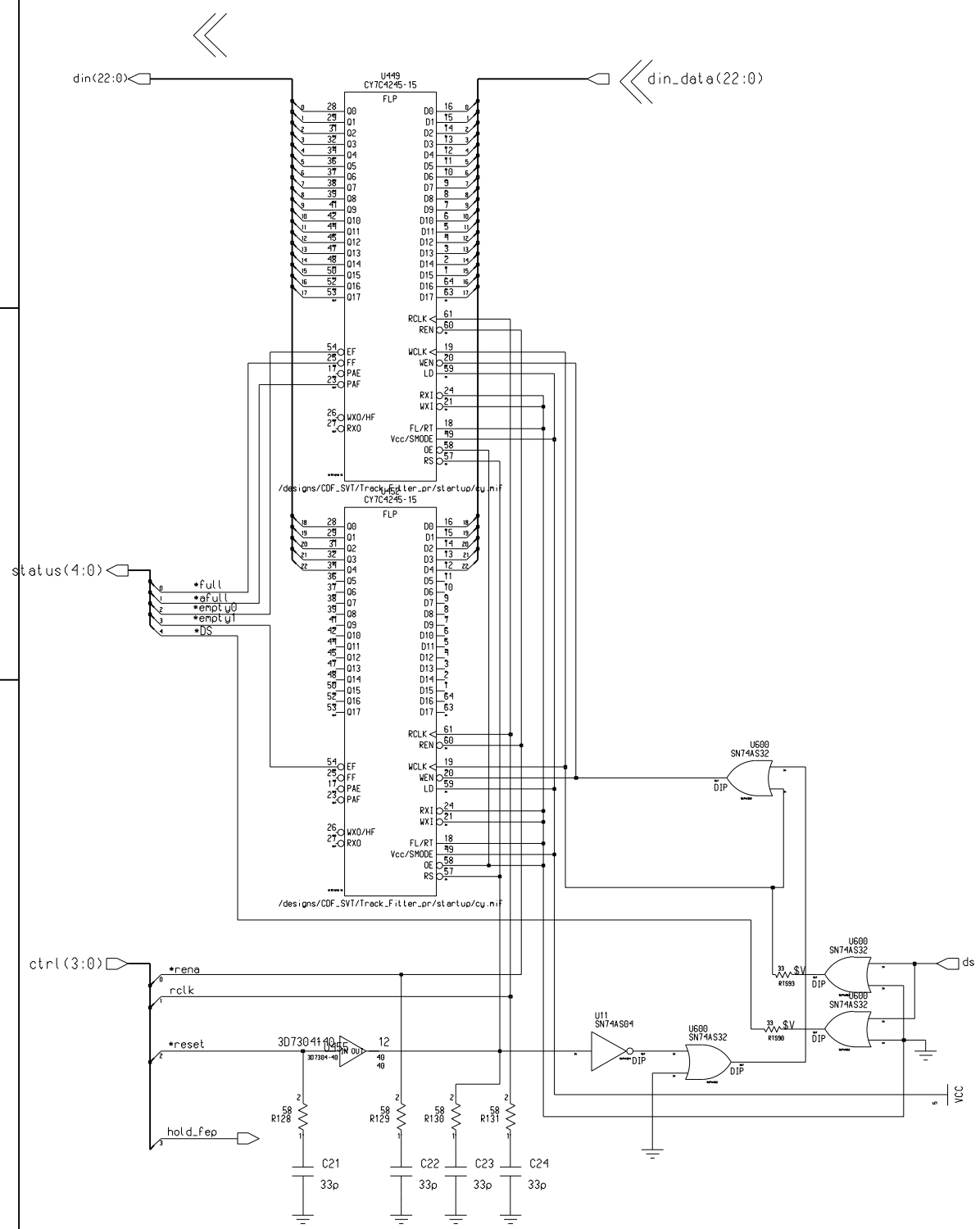
ELECTRONICS DEVELOPMENT GROUP

Pulsar
Front_Panel/DATAIN

DATE	REVISION DESCRIPTION

Sheet 21 of 25
DATE 2002-03-01
DRWN MB/TL

C-2501
REV A



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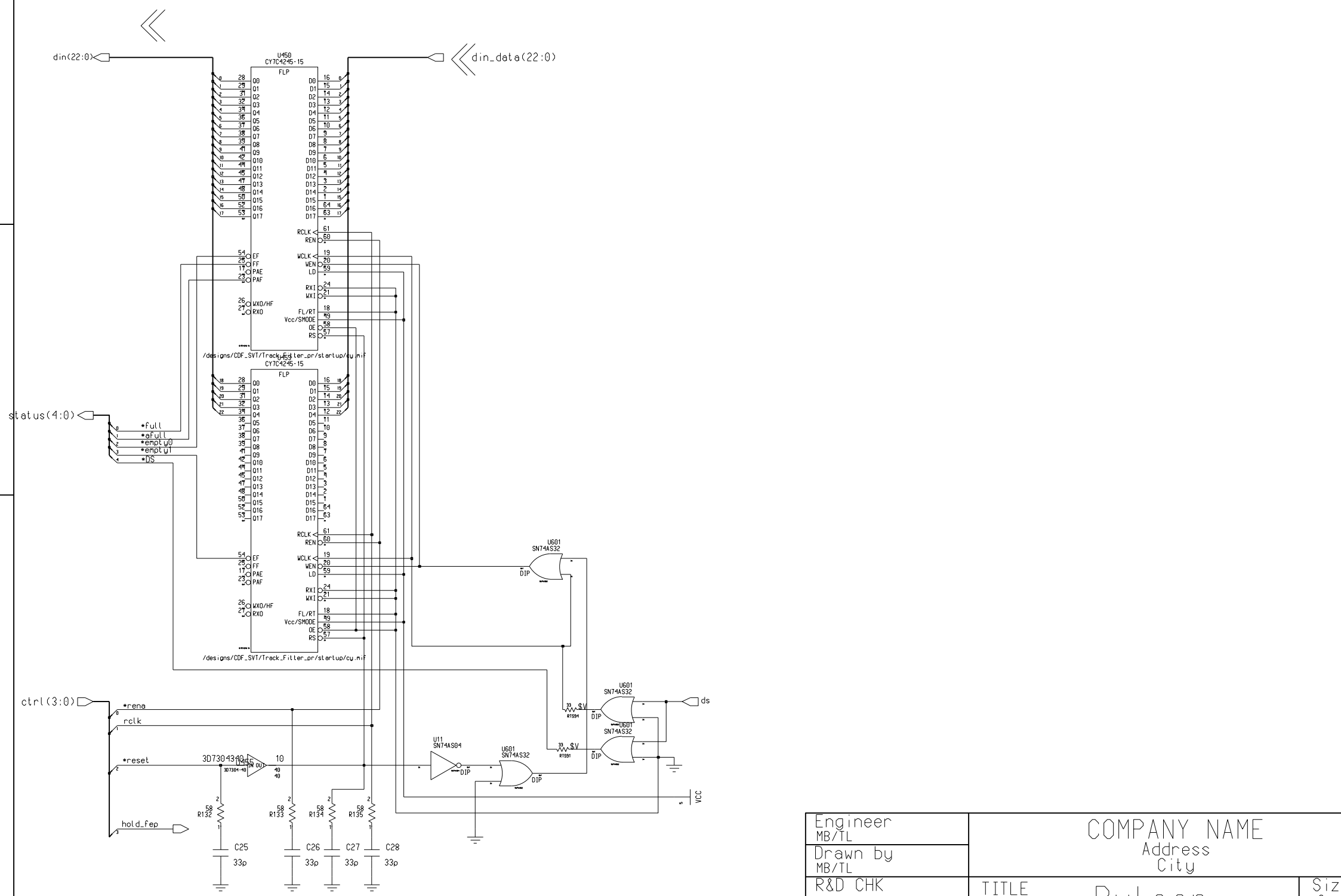
Changed by bogdan	Date Changed March 14, 2001	Time Changed 9:51:06 am	QA CHK
REV B	Drawing Number C-2501	Sheet 22 of 25	



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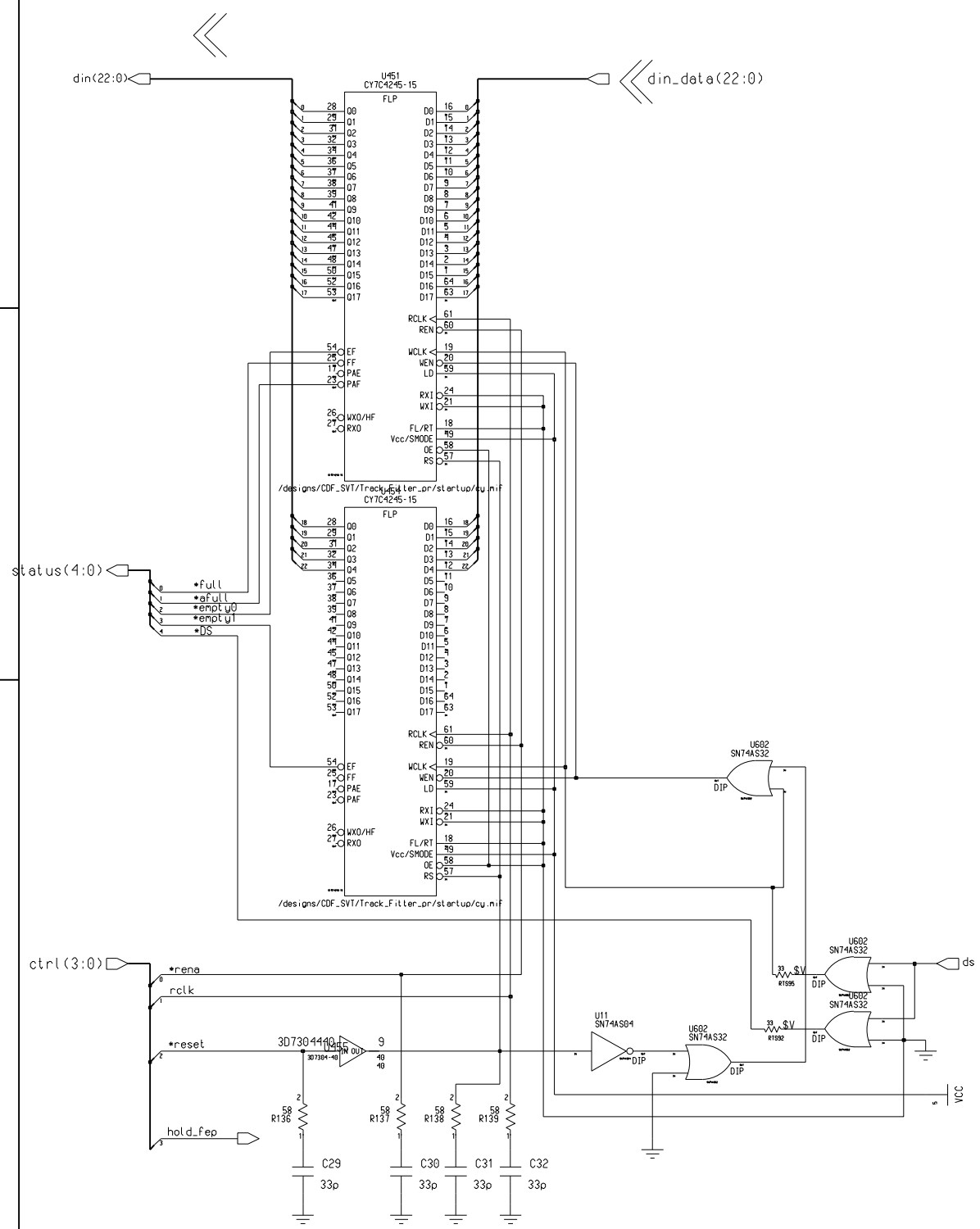
REV B	Drawing Number C-2501	Sheet 23 of 25	



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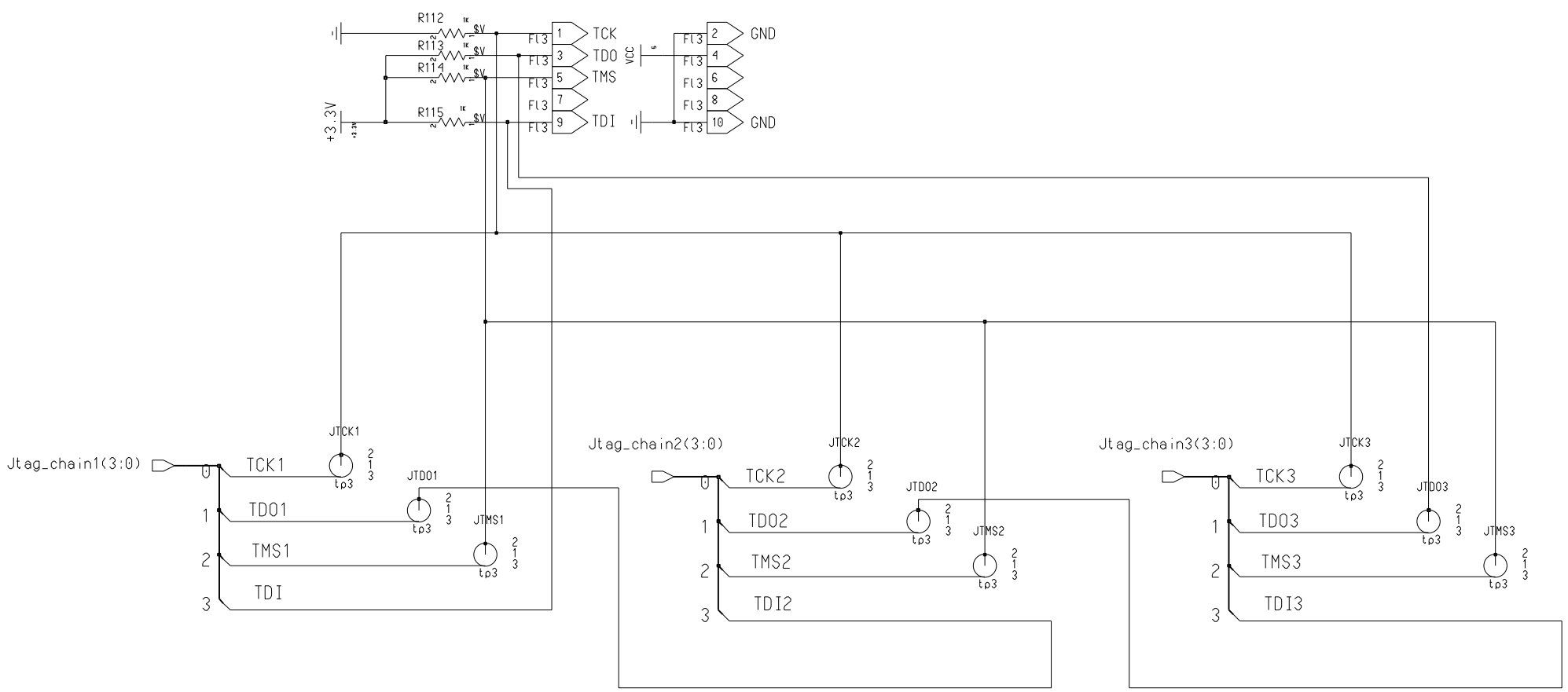
REV B	Drawing Number C-2501	Sheet 24 of 25	



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ELECTRONICS DEVELOPMENT GROUP

TITLE Pulsar Jtag_Chain

DATE	REVISION DESCRIPTION

SHEET 25 OF 25
DATE 6/14/2002
DRWN MB/TL

C-2501
REV A