

# **EVENT BUILDER DEVELOPMENTS AND PLANS**

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for the  
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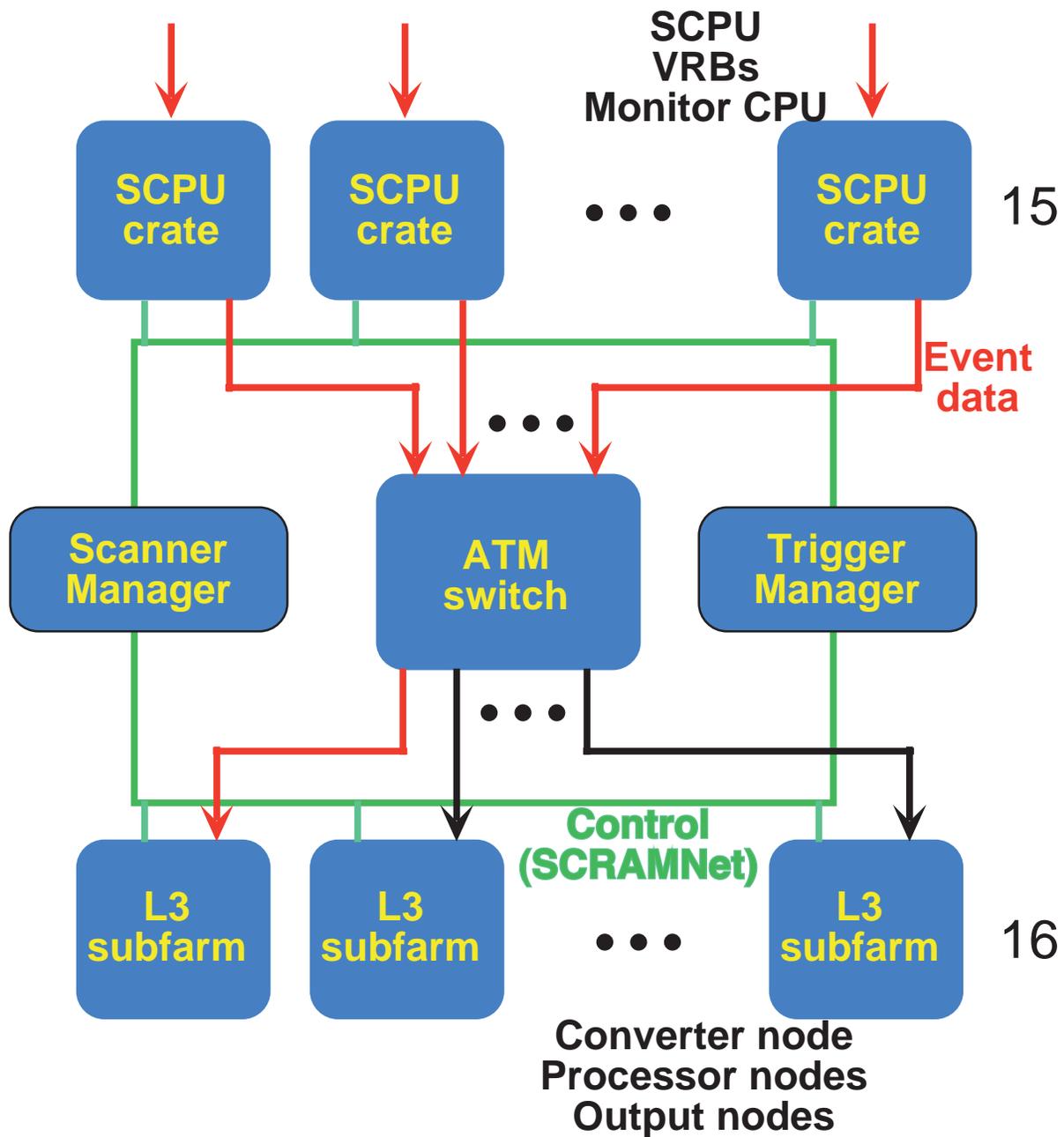
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## Summary

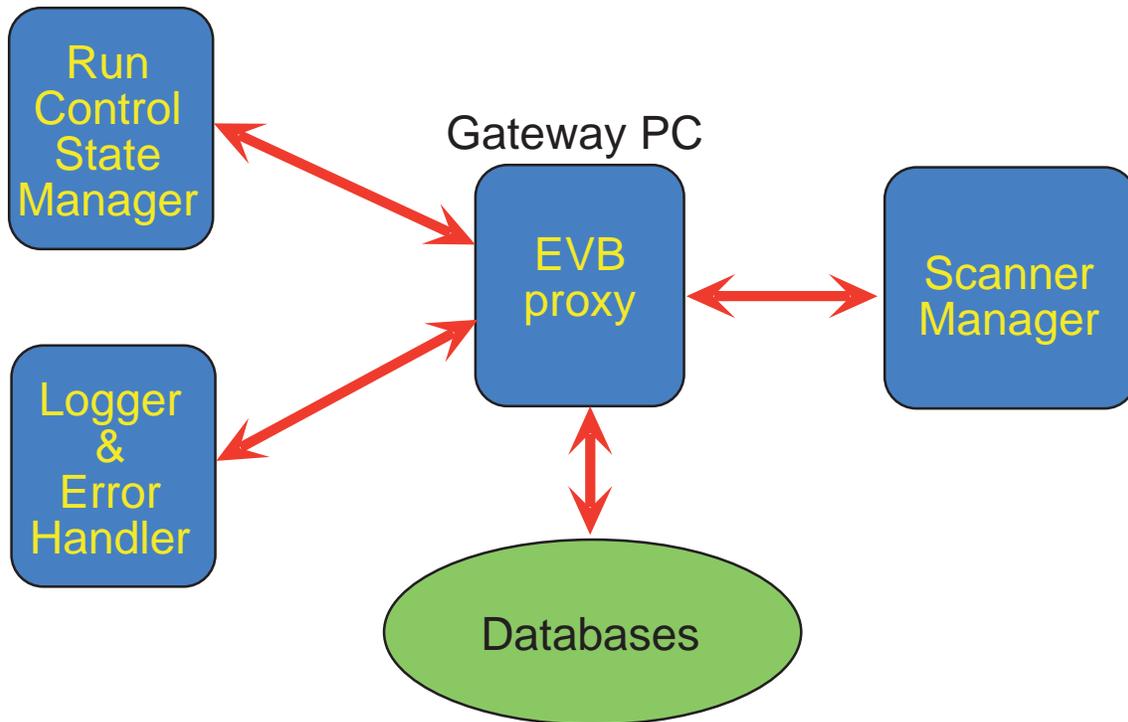
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# Intro

# Event builder architecture



# The EVB Proxy



- Why the intermediate step?
  - Event builder CPUs will remain on a private network, so they need a gateway anyhow.
  - Keep DB and SmartSockets code off VME CPUs
  - Greater freedom of implementation, e.g., one can use Java.

## Commissioning Run

# Features implemented

- Use all 16 subfarms and 30 processor nodes reliably.
- Use all SCPUs which have detector data.
- Operate well with Run Control.
- Configure using hardware database.
- Send messages readable by Error Logger.
- Publish event rate at regular intervals.
- Do some event format checking in SCPUs.
  - Helped to debug VRB readout
- Provide reasonable control GUI for Aces.
- Provide reasonable operating docs for Aces.

# Features deferred

## Events larger than 59 KB per SCPU

- Max size of single ATM packet.
- Calibrations used software event builder.

## Multi-partition operation

- Never worked in Run 1.
- Still have trouble with ending runs.

## Sharing of SVX VRBs during data-taking

- Unsynchronized use of VRBs by more than one CPU causes corruption of data read from the fast FIFO.
- Syncing method was not yet worked out.
- Needed to monitor G-link errors, SVX occupancy, etc.

**March 1 2001 and after**

# To be ready by March 1

## 5 MB per SCPU per event

- Requires multiple ATM packets per event per SCPU.
- Stand-alone tests of SCPU side OK.
- Stand-alone tests of converter node reception OK.
- Ready to test in real data-taking.

## Multipartition operation

- General bug fixes during commissioning run made it "almost" work.
- Will start work on it again by end of Jan.

# To be ready by March 1

## Allow SVX monitor CPU access to VRBs

- Software written to allow SCPU and monitor CPU to time-share VME bus.
- Time-sharing a VME memory worked.
- Works on both 260x and 230x CPUs.
- Tentatively approved by SVX group, just need to package it conveniently for them.
- Not yet tested for data-taking.

## Miscellaneous

- Produce the new end-of-run messages.
- Try to fix observed bugs
  - Occasional SCPU mem. corruption.
  - Make repeated HRR cycles more robust.
- Expand monitoring info.

# The longer term

## Once the DAQ system settles down

- See how rate can be increased.
  - Current ceiling seems to be 500 Hz with fragment size 10–16 KB.
- Have more than three reception buffers per converter node.
  - Requires different ATM addressing

## Summary

# Conclusions

**Got a decent event builder ready for the commissioning run.**

- Speed acceptable.
- Reliability acceptable.
- Operating docs acceptable.

**Work is going well on additions for March 1.**

- Larger SCPU fragments
- Multi-partition operation.
- Monitoring of SVX VRBs.