



# *Pulsar Status Report*

**PULSAR: PULSer And Recorder**

- Pulsar design **overview**:
  - from L2 teststand tool to a **general purpose** tool
- Current **status**:
  - schematics/layout, firmware, **board level simulation** etc.
- Possible **applications** for Pulsar
- Board level simulation and prototype testing plan

**Note: This talk ended up with ~ 40 slides, will only show ~20 at the meeting.**

**Ted Liu**

Friday Trigger Meeting, May 10th. 02

**Upcoming talks: Hotlink mezzanine cards design and prototype (Natalia Kuznetsova)  
Pulsar firmware in pulser mode: design and status (Peter Wittich)**

## From last meeting (Feb. 22rd)

Now the Level 2 system is working, things are much less hectic, we can do what we should have done much earlier, which is to get together to talk about the test stand plans.

**this meeting should focus on the functionality requirements**

**(or specifications) for the Level 2 test stand**, once we agree on what we should build, then things can move very fast...



We will have more meetings on test stand issues as needed.

**Last meeting we focused on functional requirements.**

**At this meeting, I will present Pulsar overall design and current status. A web page is being setup which will contain all the design (hardware and firmware) details for Pulsar, and will be available to everyone soon.**

**Since now we have the actual design, we will have brief status report at every Friday meeting from now on. We will have a Design Review later to discuss all the details.**

## What has been done since Feb.?

### Pulsar design is “optimized and almost finalized”:

- schematics finished early April
- core firmware in place
- **intensive** board level simulation in progress
- detailed firmware design and VHDL coding in progress
- initial layout work started
- Pulsar web page is almost ready with all design details

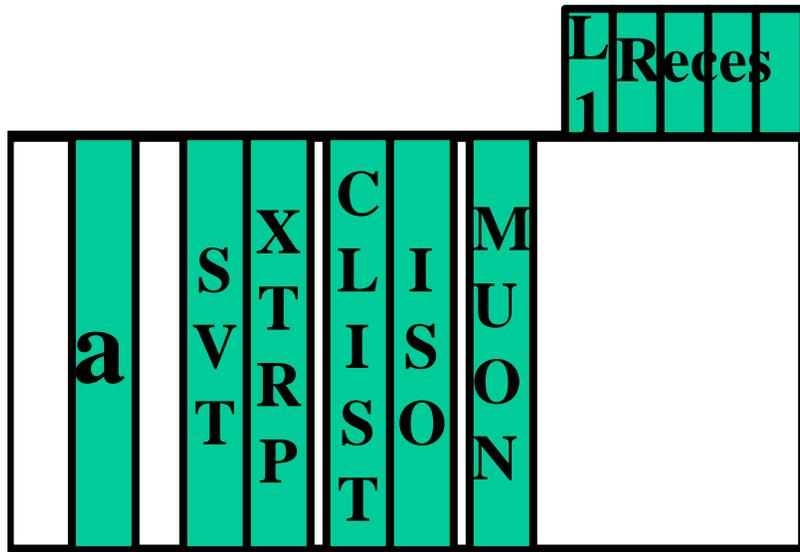
### Hotlink mezzanine cards (Tx and Rx)

- schematics finished in March
- board level simulation finished in April (with both Tx and Rx)
- prototype boards (Tx and Rx) fully loaded end of April
- prototype debugging/testing in progress

All firmware (VHDL code), compile setting files, simulation waveform, FPGA pin maps are in CVS

## Basic hardware requirement: have all hardware interfaces

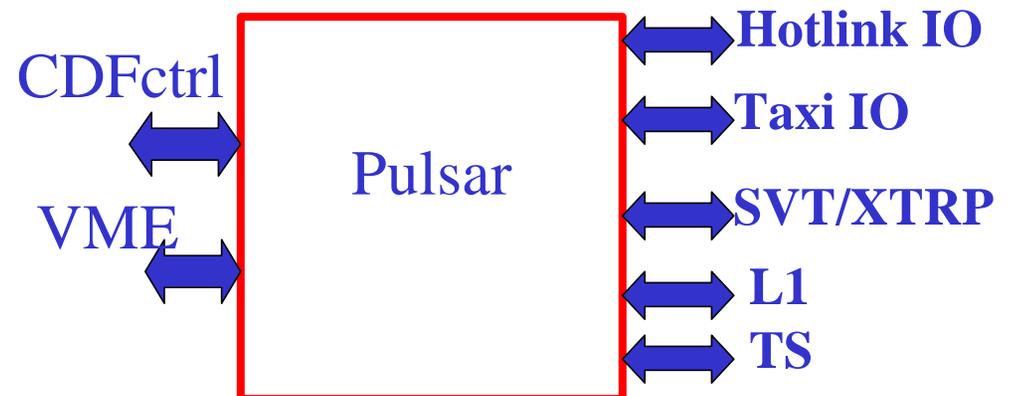
Pulsar is designed to have all the data interfaces that Level 2 decision crate has. It is a **data source** for all trigger inputs to Level 2 decision crate, it can be used to record data from upstream as well.



**L2 decision crate**

PulsAR: Pulser And Recorder

Main difficulty for Pulsar design:  
Each subsystem data path was implemented differently, to design an universal tester board is not all that easy...  
The only way is to use mezzanine cards...

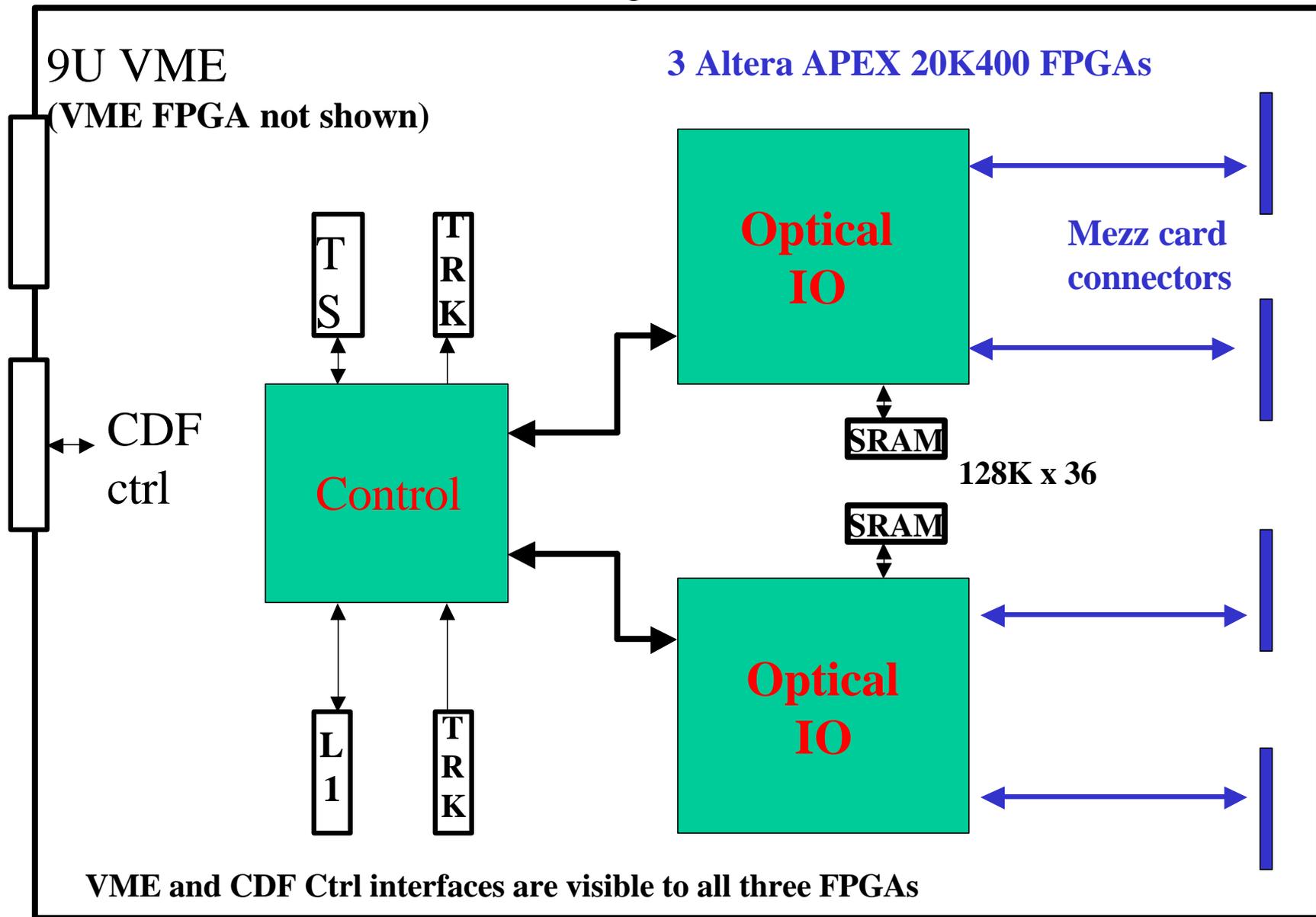


## Level 2 trigger input data paths were implemented differently

	SVT	XTRP	L1	CLIST	ISO	Muon	Reces
<b>Incoming data Clock rate</b>	30Mhz	7.6Mhz	7.6Mhz	20Mhz	12Mhz	30Mhz cdfclk x 4	7.6 Mhz cdfclk
<b>Interface hardware</b>	SVT cable	SVT cable	L1 cable	Hotlink+fiber	Taxi+fiber	Hotlink+fiber	Taxi+fiber
<b>data size range</b>	150bits/trk	21 bits/trk	96 bits/evt	46bits/clu	145bits/clu	11Kbits/evt	1.5Kb/evt
<b>Latency range*</b>	~10-100us	~1us - 10us	~132 ns	~1-20us	~few us	~1-5 us	~ 6 us
<b>Fixed or variable data length?</b>	variable	variable	fixed	variable	variable	fixed	fixed
<b>Data with Buffer#?</b>	yes	yes	yes	yes	yes	no	yes
<b>EOE with data? (or from separate path?)</b>	yes	yes	-	no	no	yes	-
<b>B0 marker?</b>	BC#	BC#	no	no	no	yes	no
<b>Data gap within one event?</b>	yes	yes	no	no	yes	no	no
<b>Flow control ?</b>	Not used	not used	no	no	no	no	no

\* Latency range also depends on L1A history ...

# Level2\_Pulsar design as test stand tool



Pulsar: Pulsar and Recorder (as Level 2 test stand tool)

## Pulsar interface to/from P1 and P2 backplane

### VME interface to all three FPGAs:

- based on UC VMEchip used on other UC boards
- the interface from UC VMEchip to three main FPGAs:  
VMEdata(31:0), VMEaddr(23:2), vmeAS, vmeDS and vmeWrite

### CDF control (P2) signals to all three FPGAs:

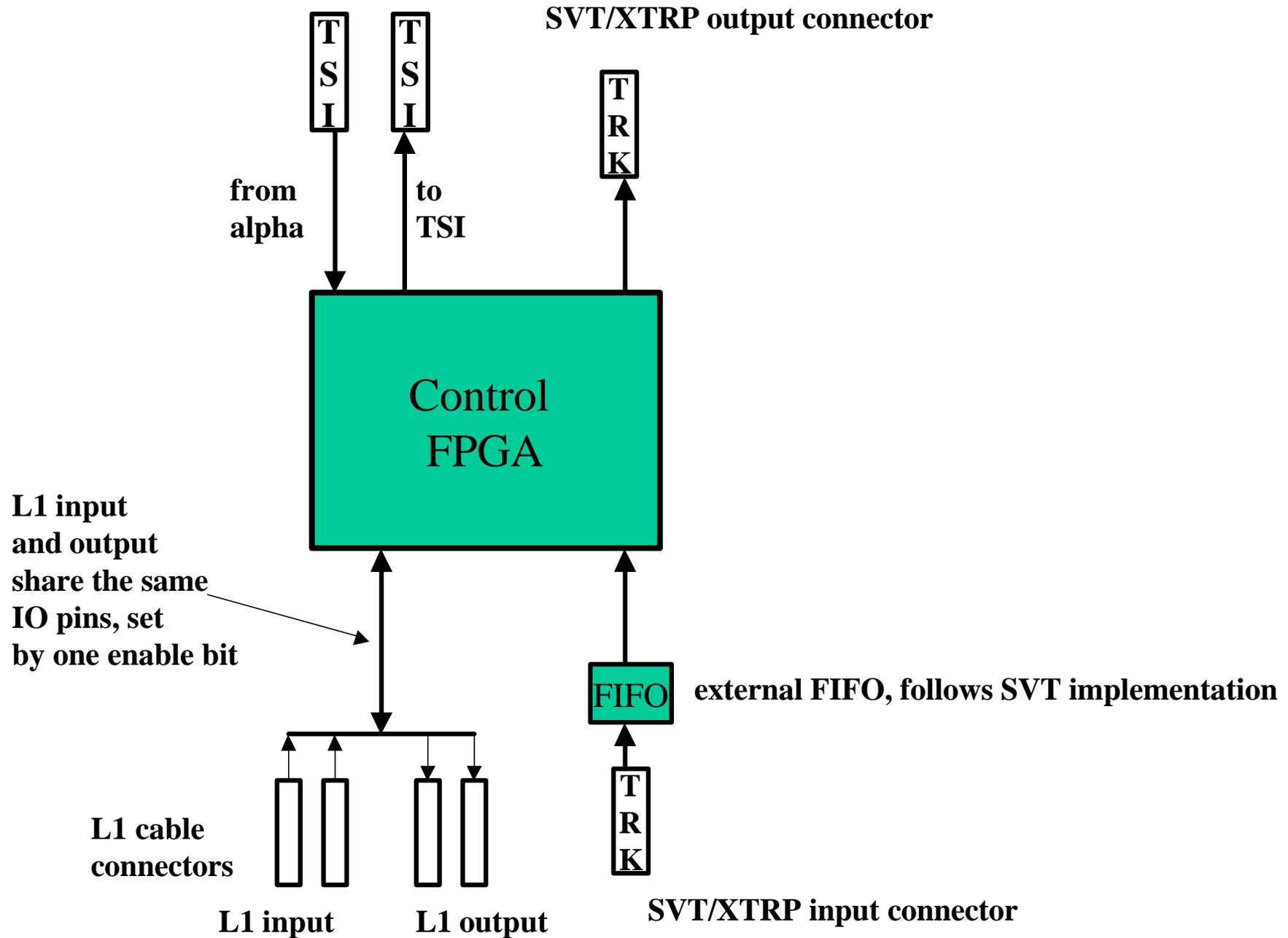
- CDFCLK, BC, B0, L1A/R, L2B0/B1, Halt, Recover, Run, L2A/R, L2BD0/BD1, CDF\_error, GLIVE, STOP, RL(2:0) ... -- this is the current map, can add more.

### Pulsar inter-communication control lines (P2 user defined pins):

- follows SVT implementation (can communicate with any SVT board)
- A1: Pulsar\_init
- A2: Pulsar\_error
- A3: Pulsar\_freeze
- A4: Pulsar\_lostlock
- A5: Pulsar\_spare

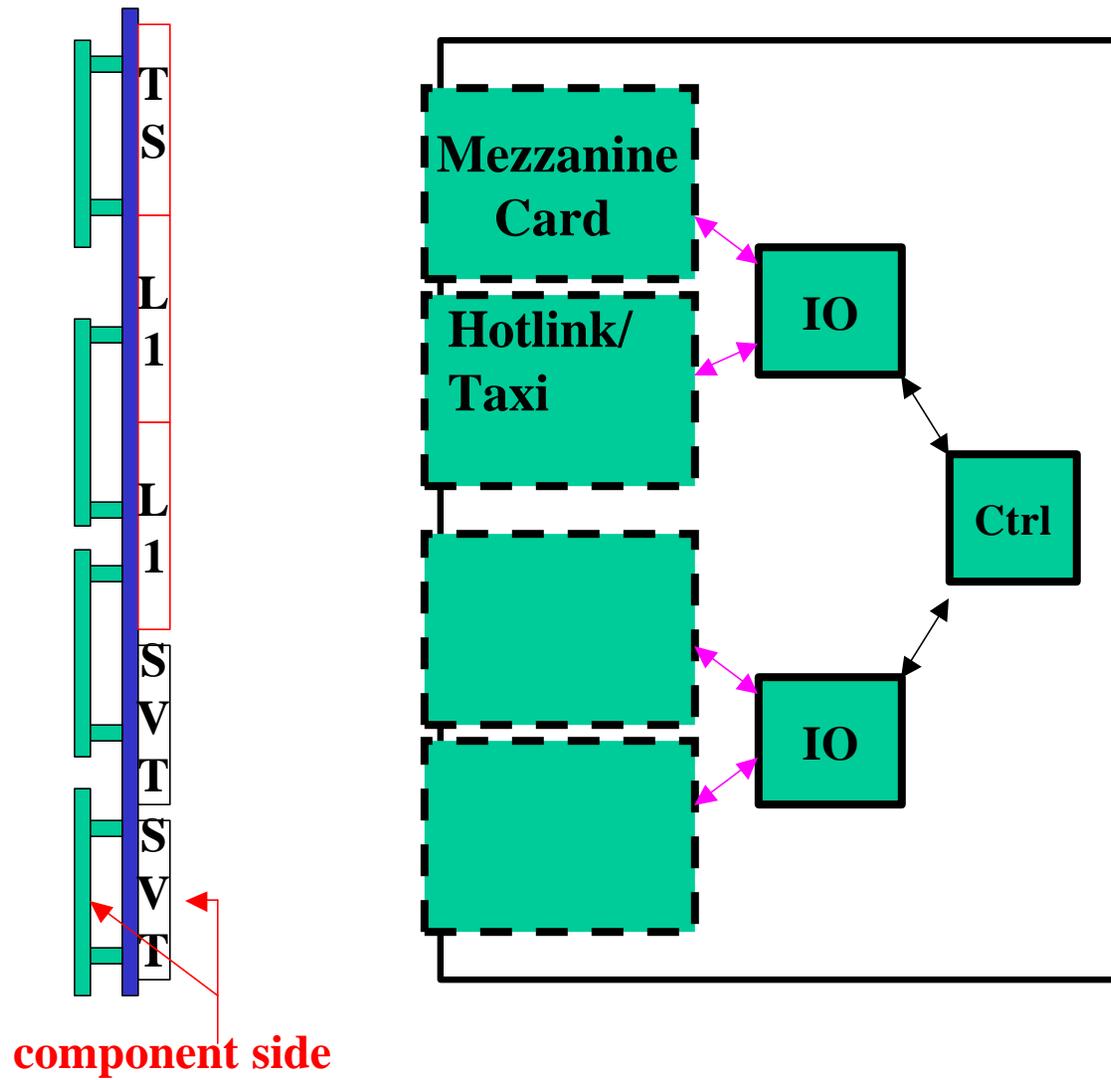
Any Pulsar board can drive and listen to these 5 lines from P2.

## Some details on SVT/XTRP, L1 and TSI interfaces



Front-panel  
(double width)

PULSAR design as L2 teststand tool only



component side

Other connectors (2 L1 outputs, 1 TS) will stay inside the board.

The mezzanine card connectors are used for optical I/O (hotlink and taxi)

*Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count*      *Notes (1), (2)*

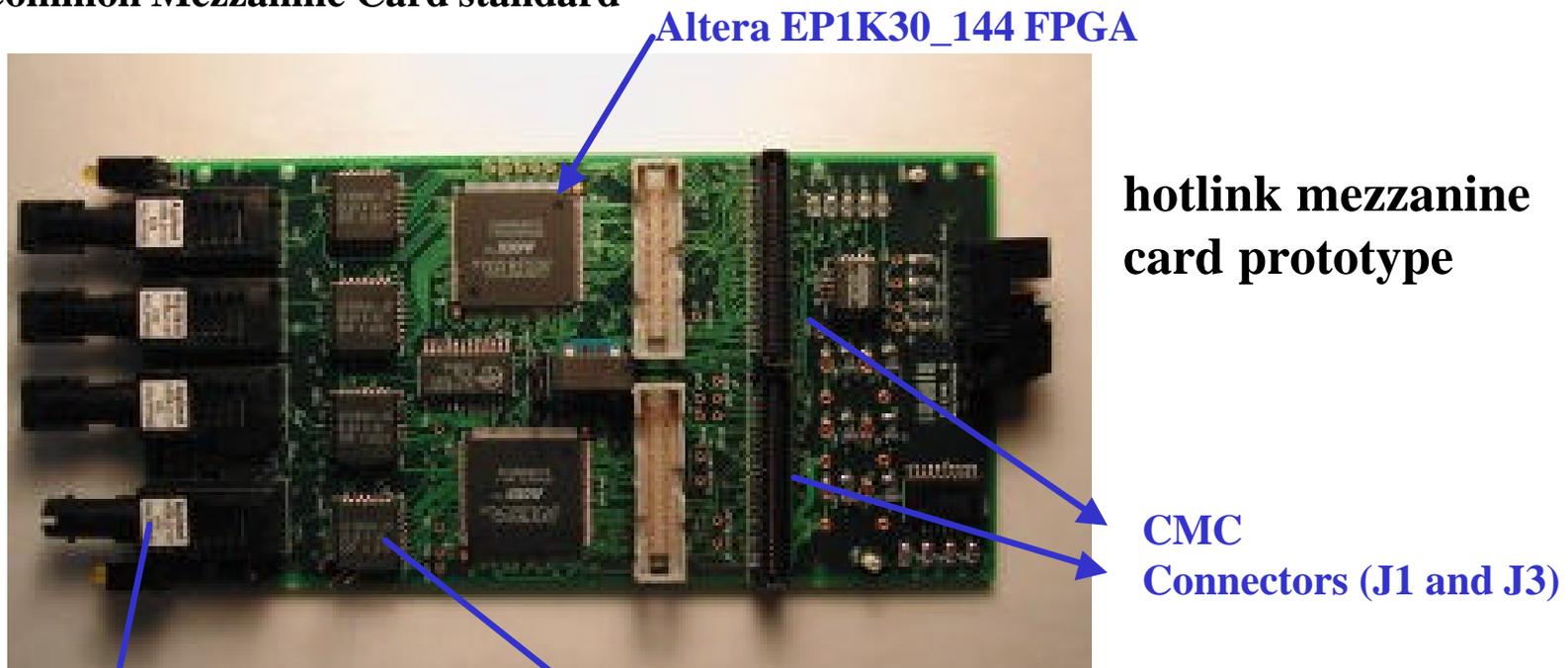
Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30 E	92	125				
EP20K60 E	92	143	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
<u>EP20K400</u>					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000 E					488	
EP20K1500 E					488	

**FPGA choice:** the 356-Pin BGA package only allows us to choose up to EP20K200 (with only 271 user I/O pins), while 652-pin BGA package (~500 user I/O pins) allows us to chose anything above EP20K200...prefer 5 V compatible which leaves **EP20K400** the only choice. EP20K400 has 26KB internal RAM capability which should be big enough.

## Custom Mezzanine cards (**follow CMC standard**)

- Hotlink: Tx and Rx (CLIST, Muon data paths)
- Taxi: Tx and Rx (Iso, Reces data paths)

CMC: Common Mezzanine Card standard



Hotlink Optical Tx/Rx: HFBR-1119T/2119T

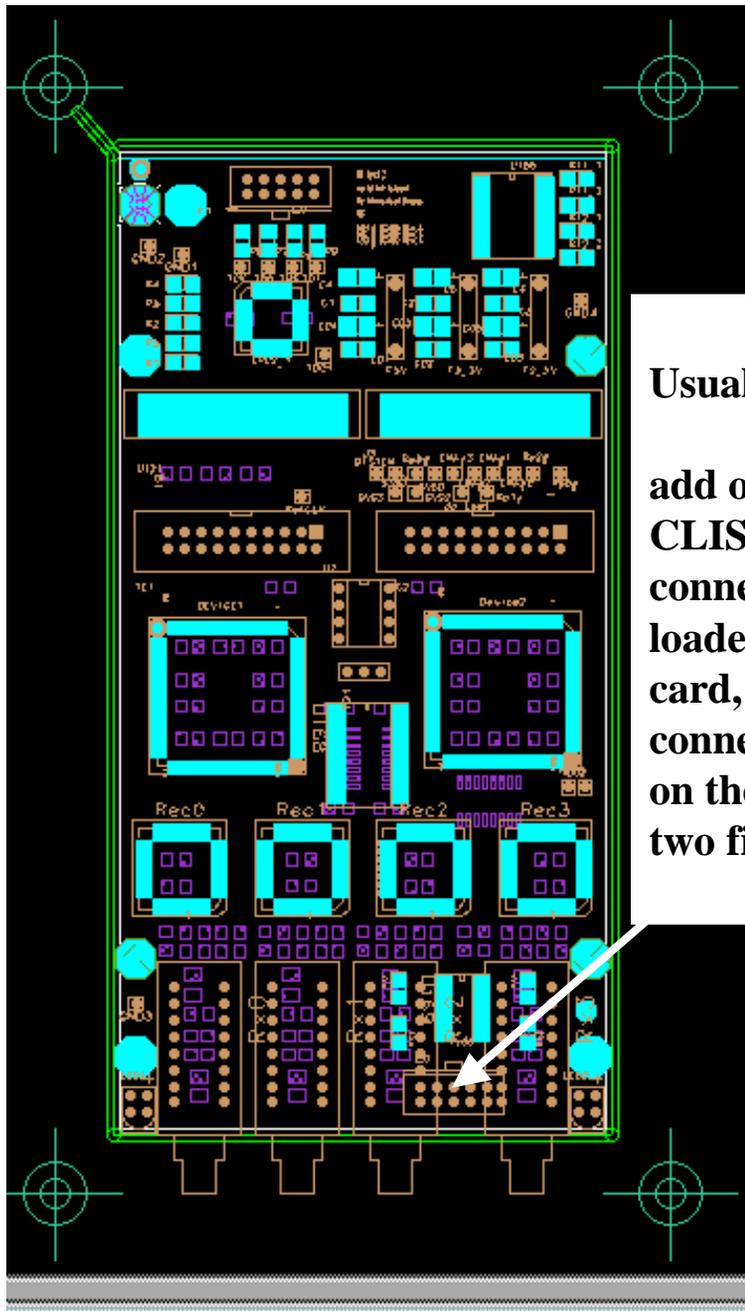
Taxi Optical Tx/Rx: HFBR-1414T/2416T

Hotlink or Taxi Tx/Rx chips

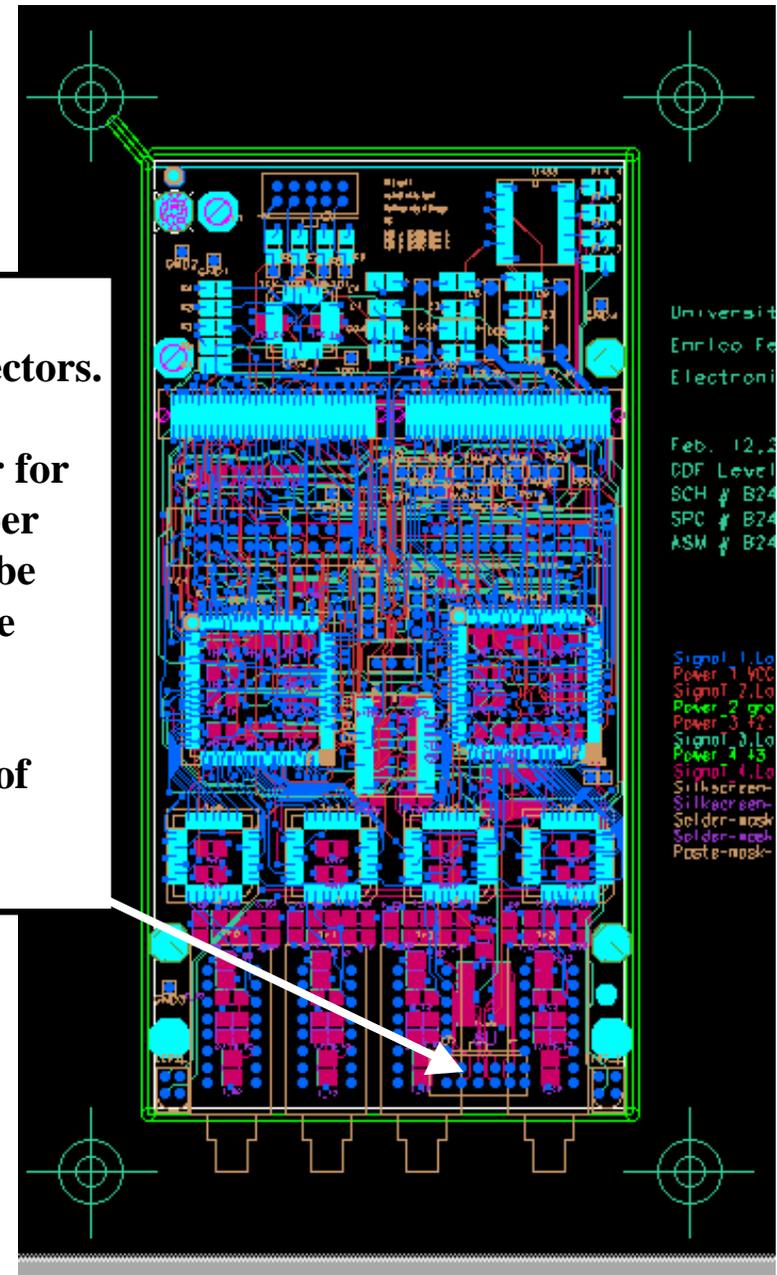
Hotlink Tx/Rx: CY7B923JC/933JC

Taxi Tx/Rx: AM7968/7969-175JC

## Hotlink Rx mezzanine



## Hotlink Tx mezzanine



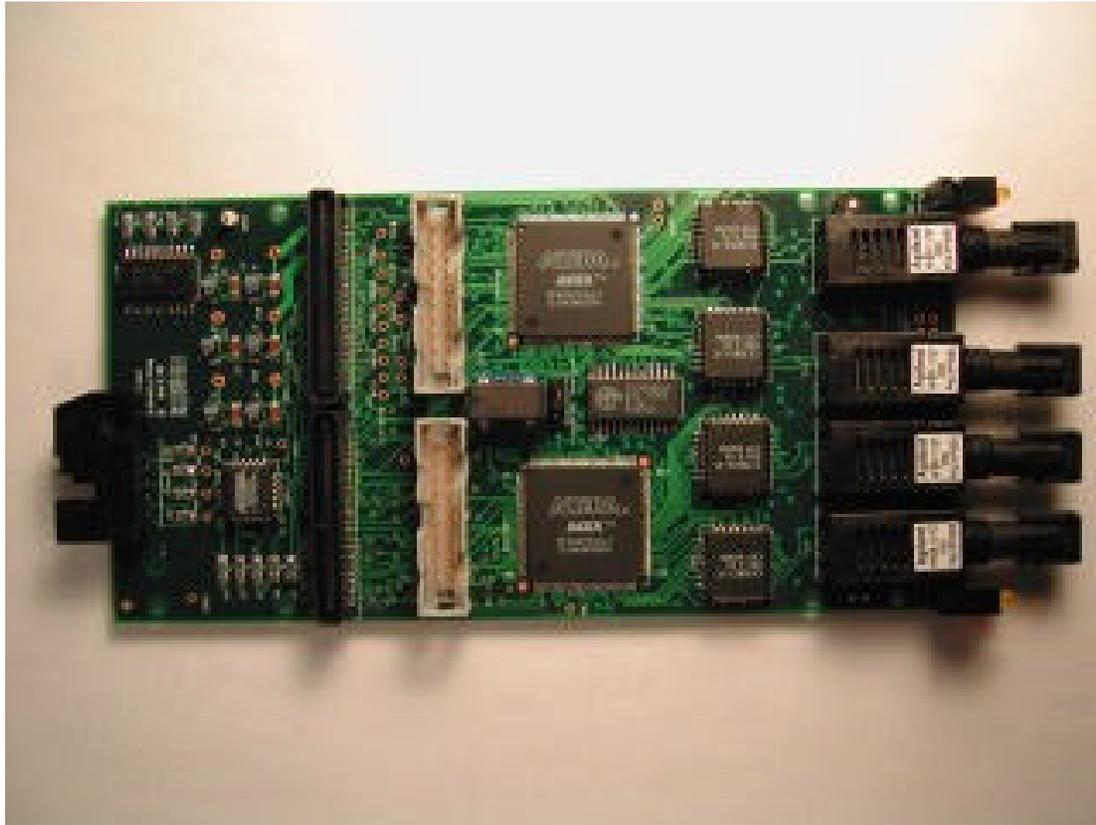
Usually has 4 fiber connectors.

add one LVDS connector for CLIST case: only two fiber connector (left side) will be loaded for one Mezzanine card, and one LVDS connector will be loaded on the right side instead of two fiber connectors

Universit  
Enrico Fe  
Electroni

Feb. 12, 2  
CDF Level  
SCH # B24  
SPC # B24  
ASM # B24

Signal 1.Lo  
Power 1.W00  
Signal 2.Lo  
Power 2.gro  
Power 3.V2.  
Signal 3.Lo  
Power 4.45  
Signal 4.Lo  
Silkscrpt  
Solder-mask  
Solder-mask  
Post-mask



Hotlink mezzanine cards  
prototypes (Tx and Rx)

Natalia will talk about  
the details next week



## Pulsar design (cont.):

→ From test stand tool to a general purpose tool

Since there are some spare FPGA IO pins left, decided to use them to enhance Pulsar capability.

A few simple modifications:

- (1) Add signal traces to P3 connector for SLINK IO, this allows Pulsar to interface directly with a PC via commercially available SLINK to PCI cards
- (2) Make L1 and SVT/XTRP inputs visible to all 3 FPGAs instead of just one FPGA

**Note:** the mezzanine card connector is already compatible with SLINK mezzanine cards as both of them follow CMC standards. This allows us to test Pulsar prototype with SLINK test tools as well.

Since the modification is simple enough at hardware level, it doesn't hurt to add them in, to make the board more general purpose. It provides the interface to a PC (via SLINK to PCI board) which could be very useful as a general purpose diagnostic tool.

To learn more about SLINK, see CERN web page:

<http://hsi.web.cern.ch/HSI/s-link/>



## **S-LINK on the web**

**[www.cern.ch/hsi/s-link](http://www.cern.ch/hsi/s-link)**

### **General information**

- News, Specifications, Introduction

### **Projects using S-LINK**

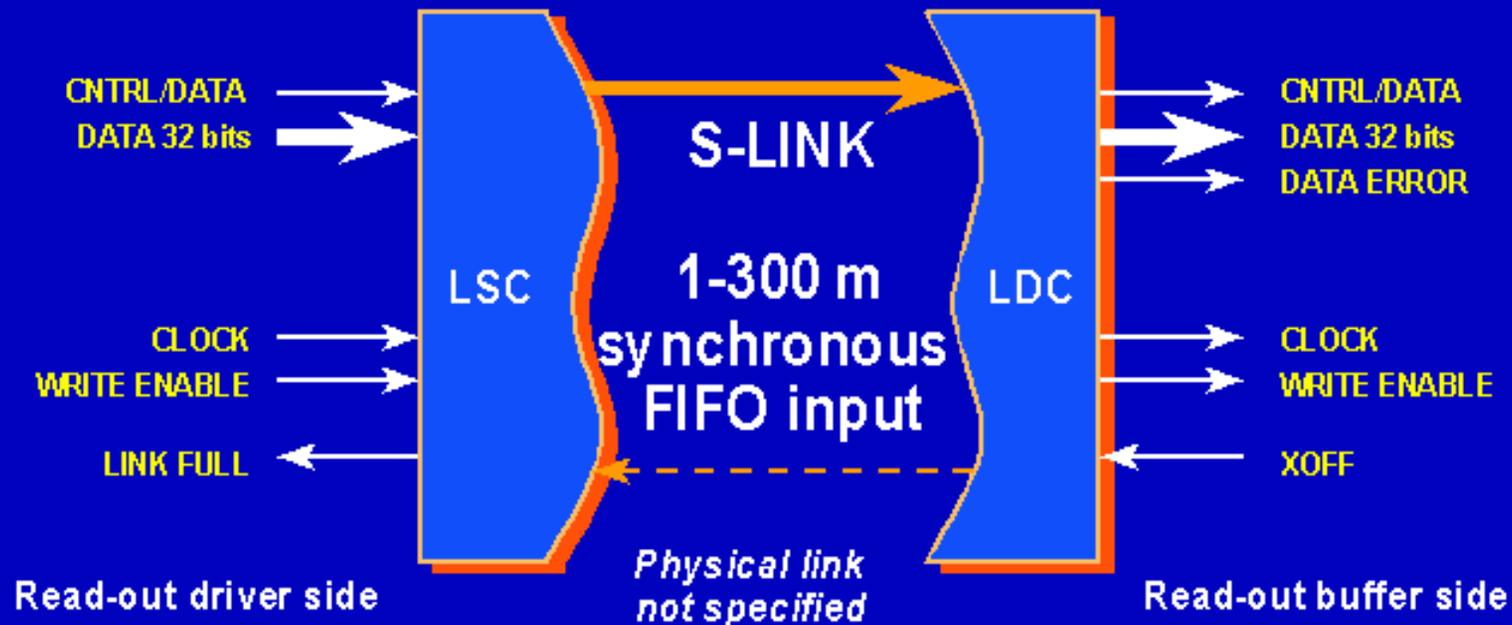
- Experiments
- Insitutes outside HEP

### **S-LINK products**

- FEMBs
- S-LINK Implementations
- ROMBs
- Testing devices
- Models



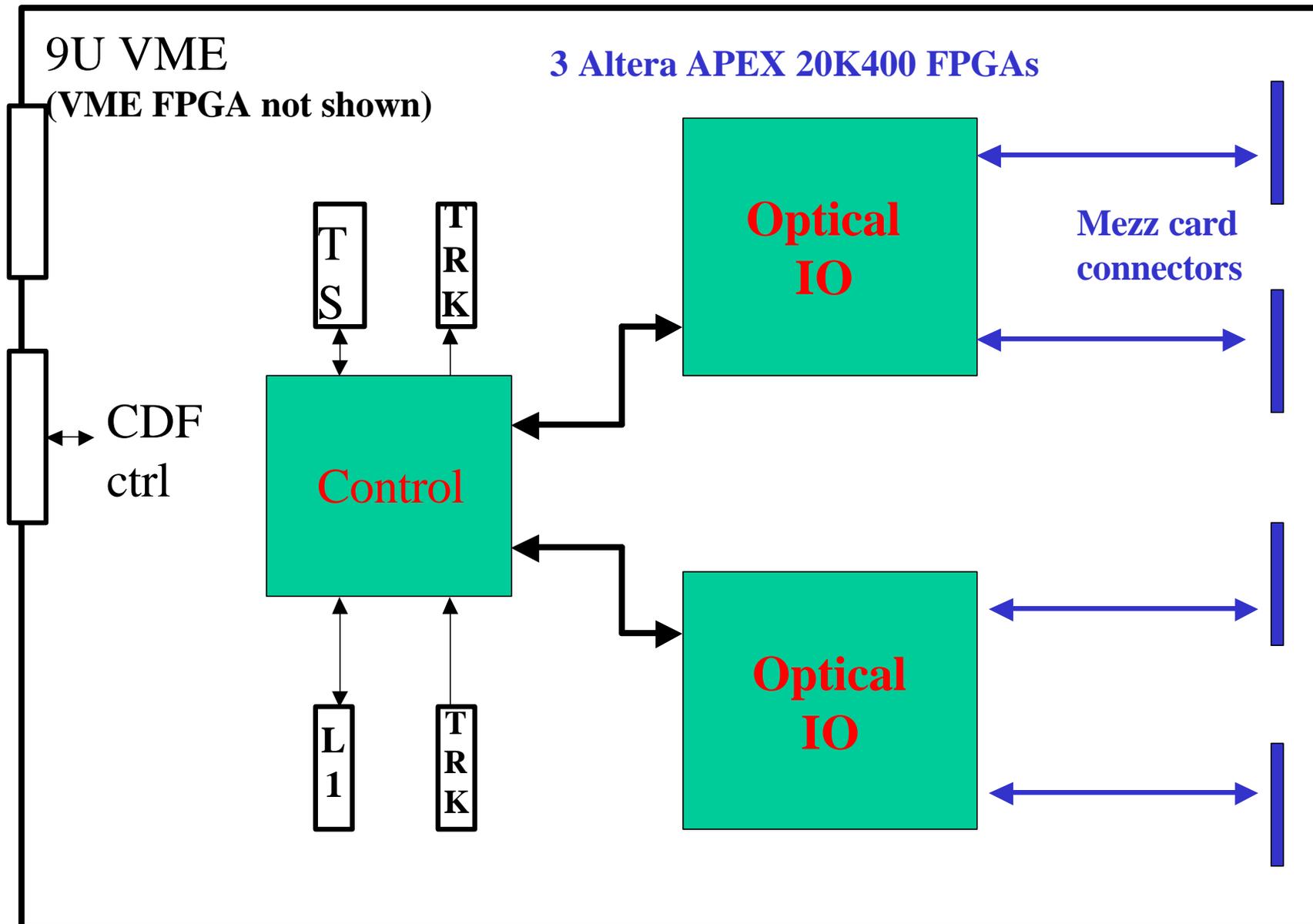
# S-LINK is just like a loooong FIFO



Features not shown:

- Self test mode
- Link down signalling
- Return lines

# Level2\_Pulsar design (as a tester only)

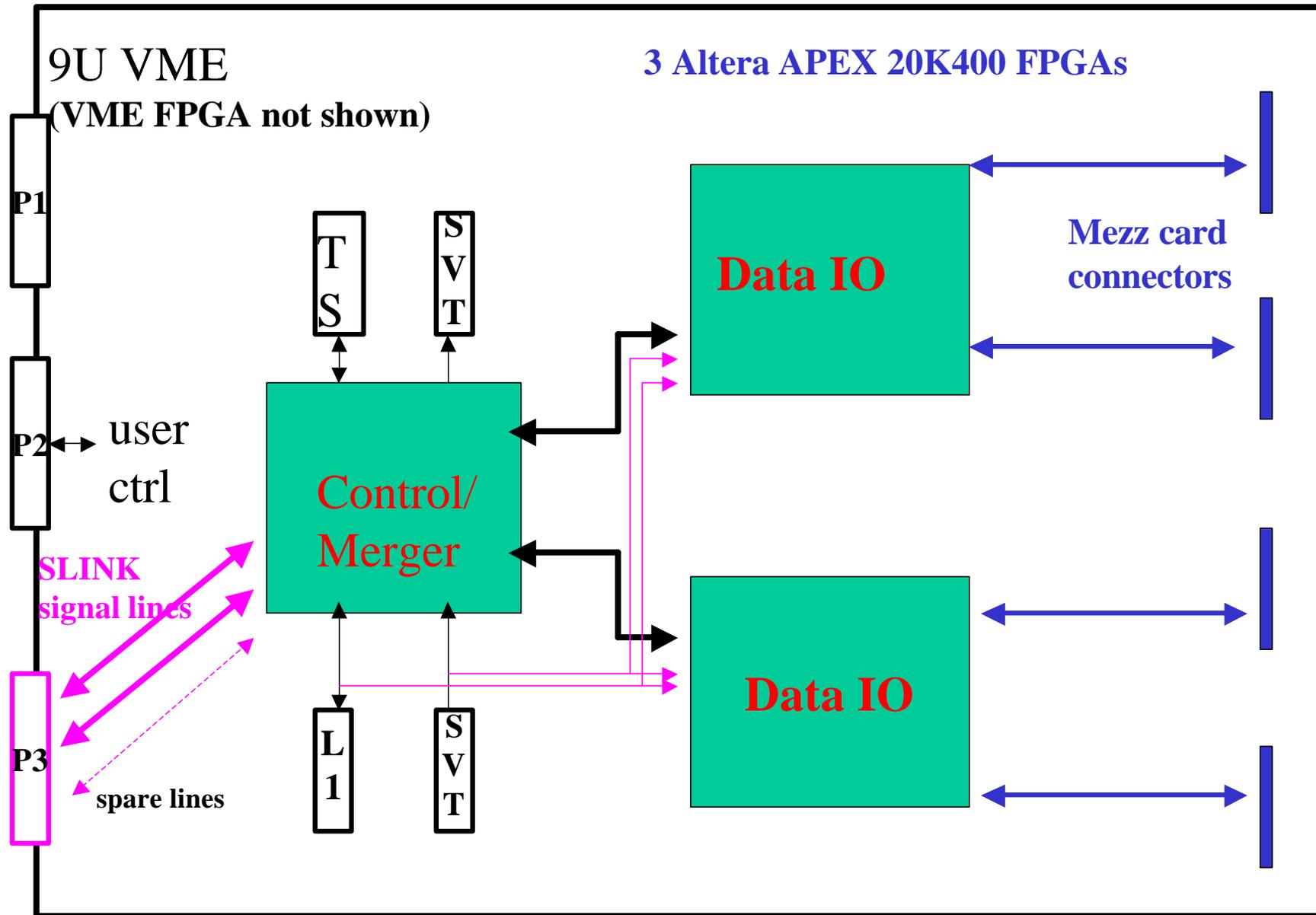


With minor modifications:



see next

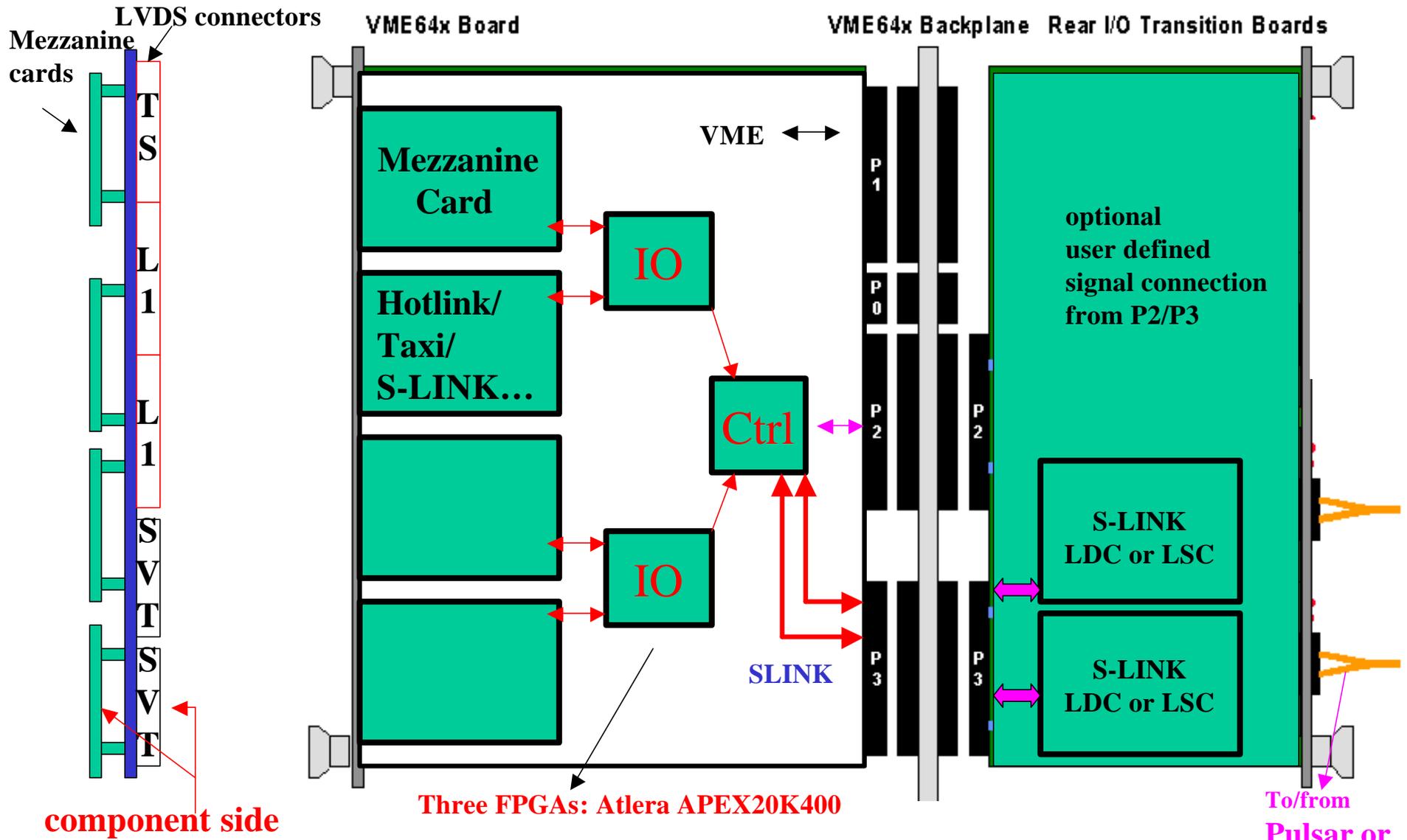
# Pulsar design (general purpose tool)



With minor modifications

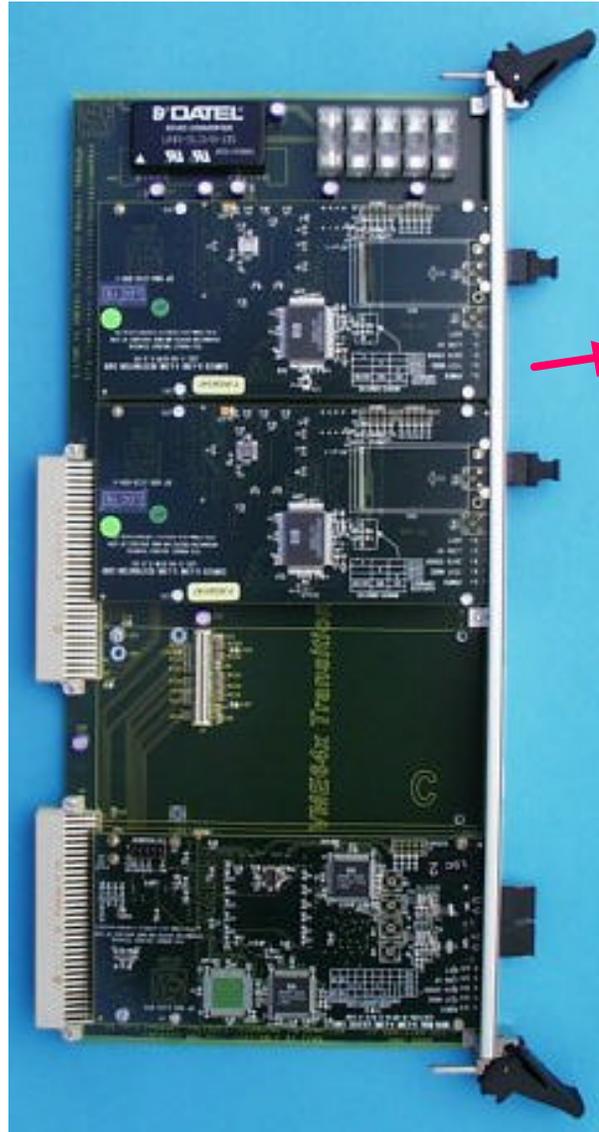
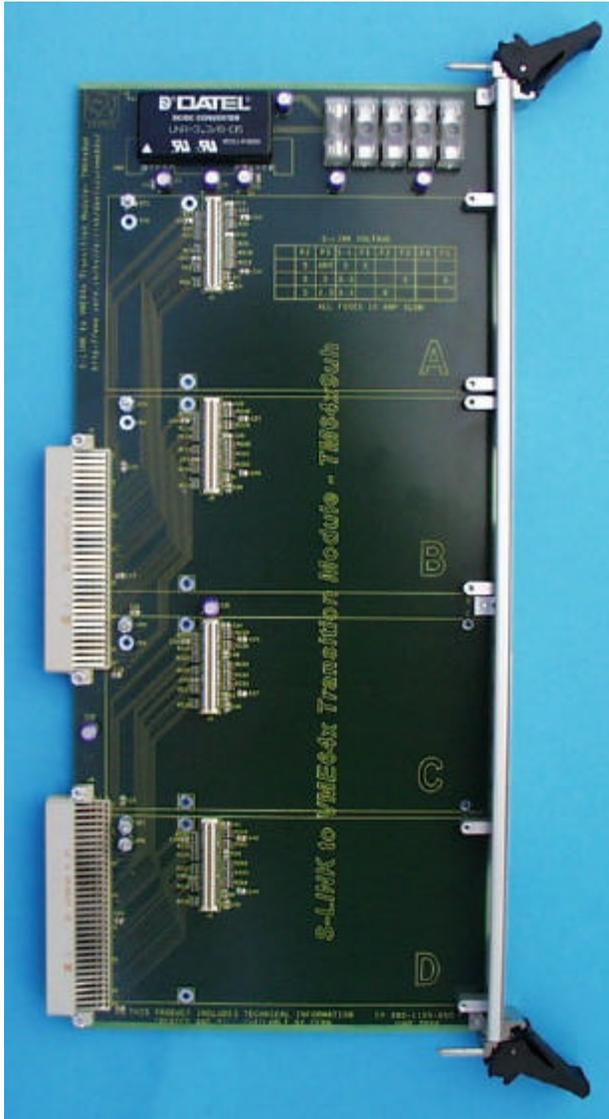
# Front-panel (double width)

# PULSAR design



The mezzanine card connectors can be used either for user I/O or SLINK cards

To/from  
Pulsar or  
a PC



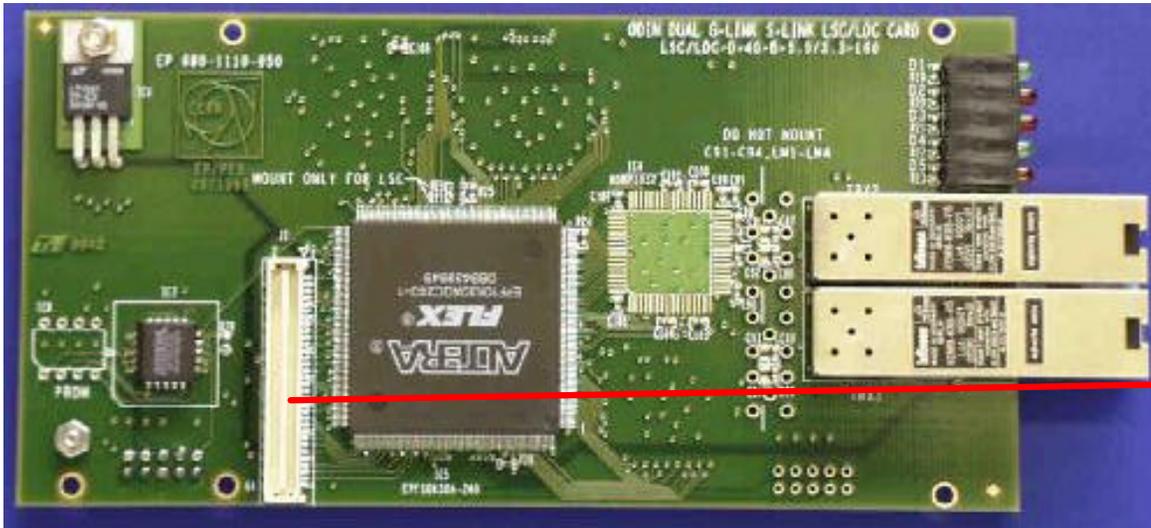
Loaded with SLINK Mezzanine cards

Can simply use CDF CAL backplane.

CERN sent us two transition modules

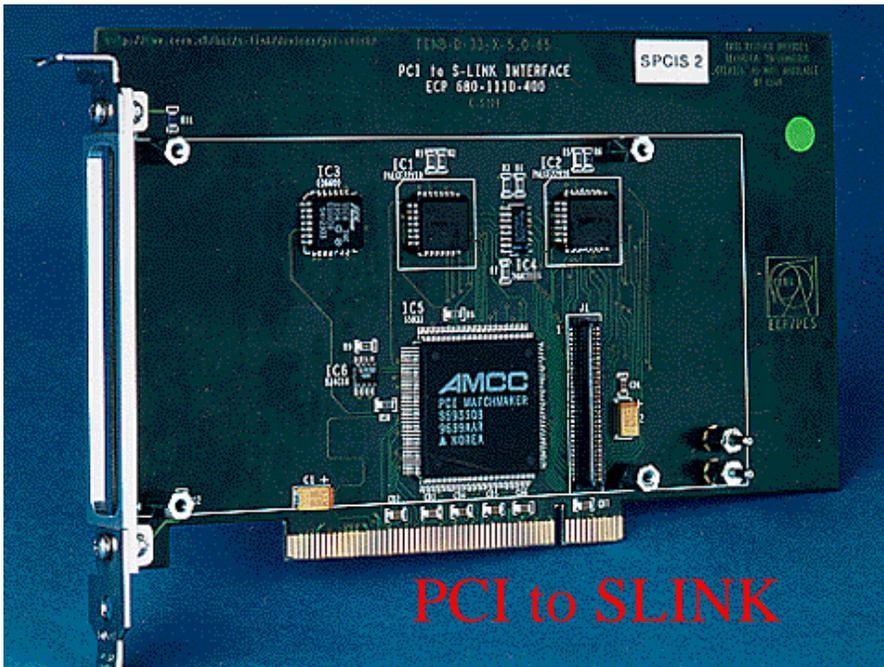
The transition module is very simple (just a few SLINK CMC connectors). It uses P2 type connector for P3. We will only use P3 for SLINK and spare (user defined) signals. (it doesn't have to be P2 type connector).

# Examples of SLINK products

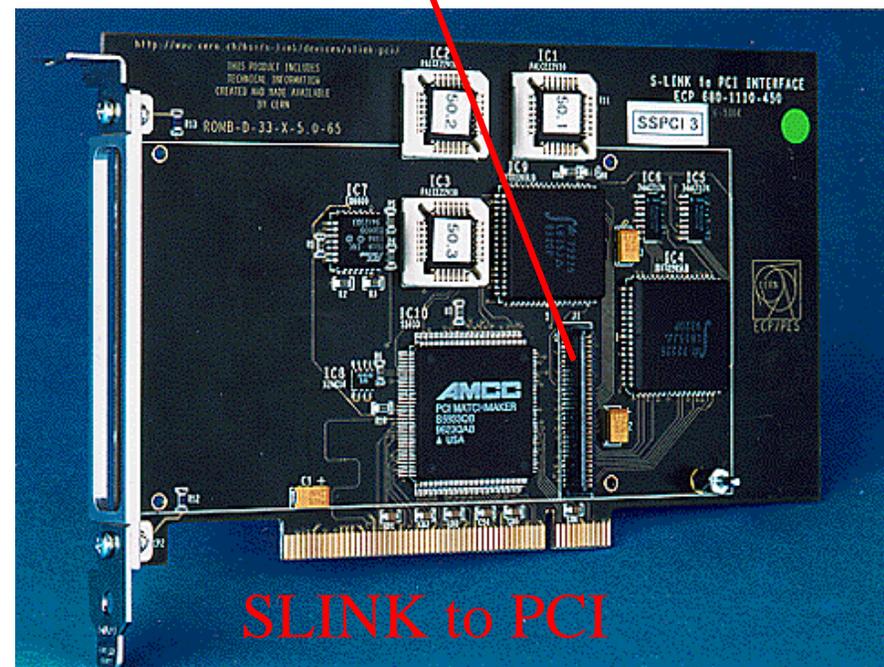


**LSC (Link Source Card),  
LDC (LINK Destination Card)**

**Mezzanine card which can plug  
onto motherboard via  
CMC(Common Mezzanine Card)  
Connector (just like PMC).**



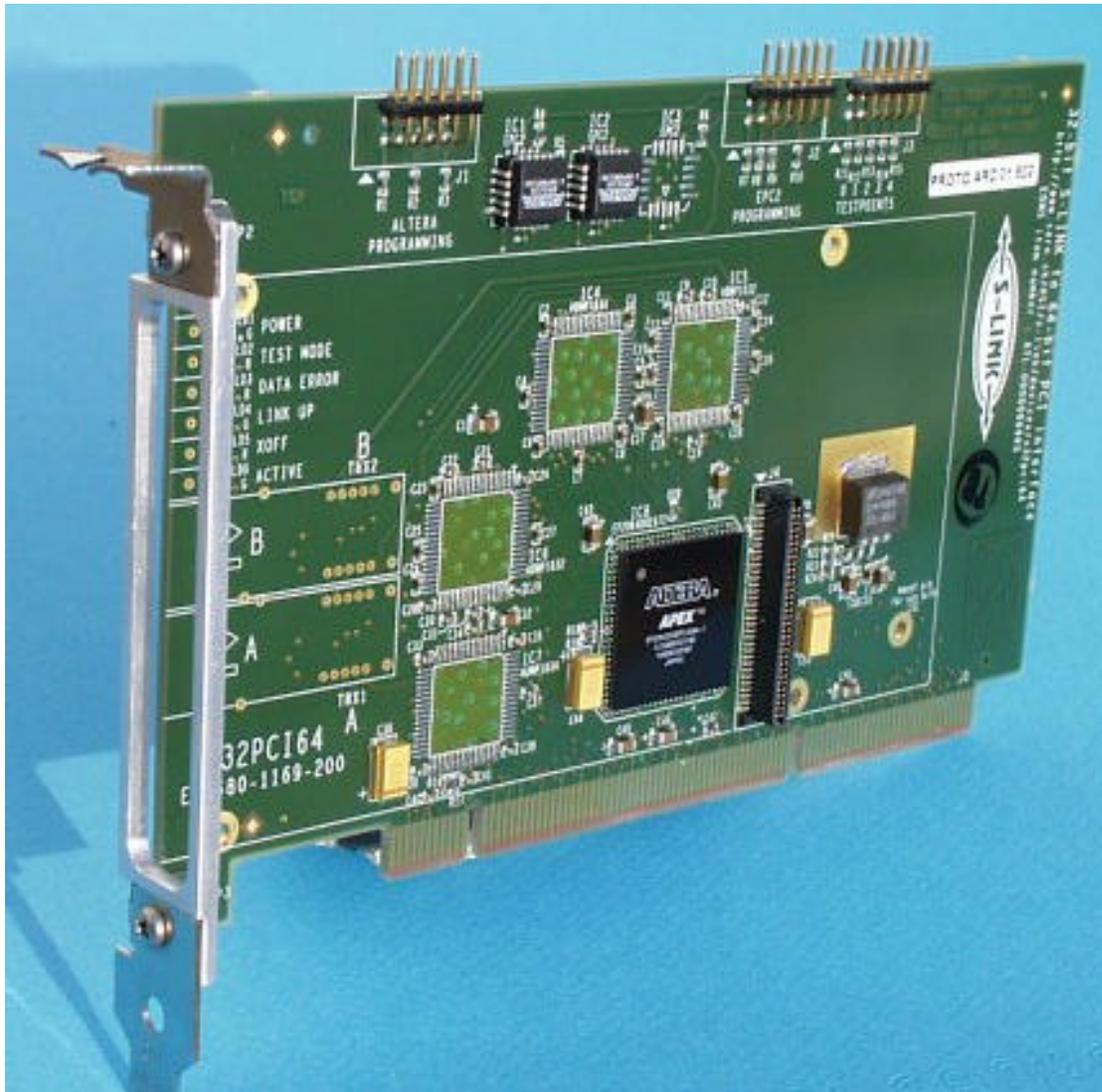
**PCI to SLINK**



**SLINK to PCI**

**Proven technology, has been used by a few experiments to take  
hundreds of TB data in the past few years**

## New 32-bit SLINK to 64 bit PCI interface card: S32PCI64

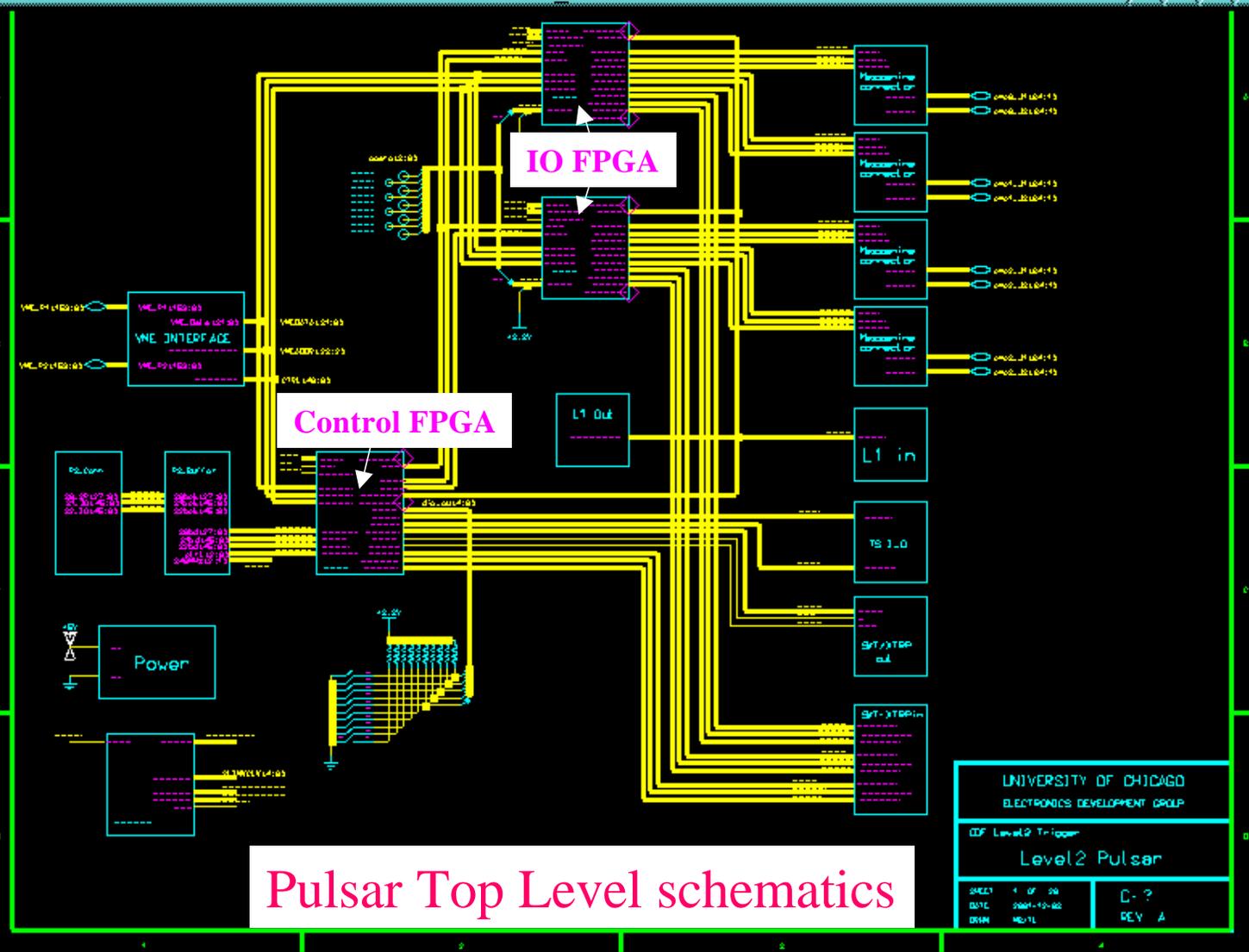


- highly autonomous data reception
- 32-bit SLINK, 64-bit PCI bus
- 33MHz and 66 MHz PCI clock speed
- up to 260MByte/s bandwidth

High-speed follow up of the Simple SLINK to PCI interface card

## SLINK format example: ATLAS SLINK data format

<b>Beginning of Block control word</b>
<b>Start of Header Marker</b>
<b>Header Size</b>
<b>Format Version No.</b>
<b>Source Identifier</b>
<b>Level 1 ID</b>
<b>Bunch Crossing ID</b>
<b>Level 1 Trigger Type</b>
<b>Detector Event Type</b>
<b>Data or Status elements</b>
<b>Status or Data elements</b>
<b>Number of status elements</b>
<b>Number of data elements</b>
<b>Data/Status First Flag</b>
<b>End of Block control word</b>



# Pulsar Top Level schematics

UNIVERSITY OF CHICAGO  
ELECTRONICS DEVELOPMENT GROUP

ODF Level2 Trigger  
Level2 Pulsar

SHEET	1 OF 20	C-?
DATE	2004-12-02	REV A
DRAWN	HEJL	

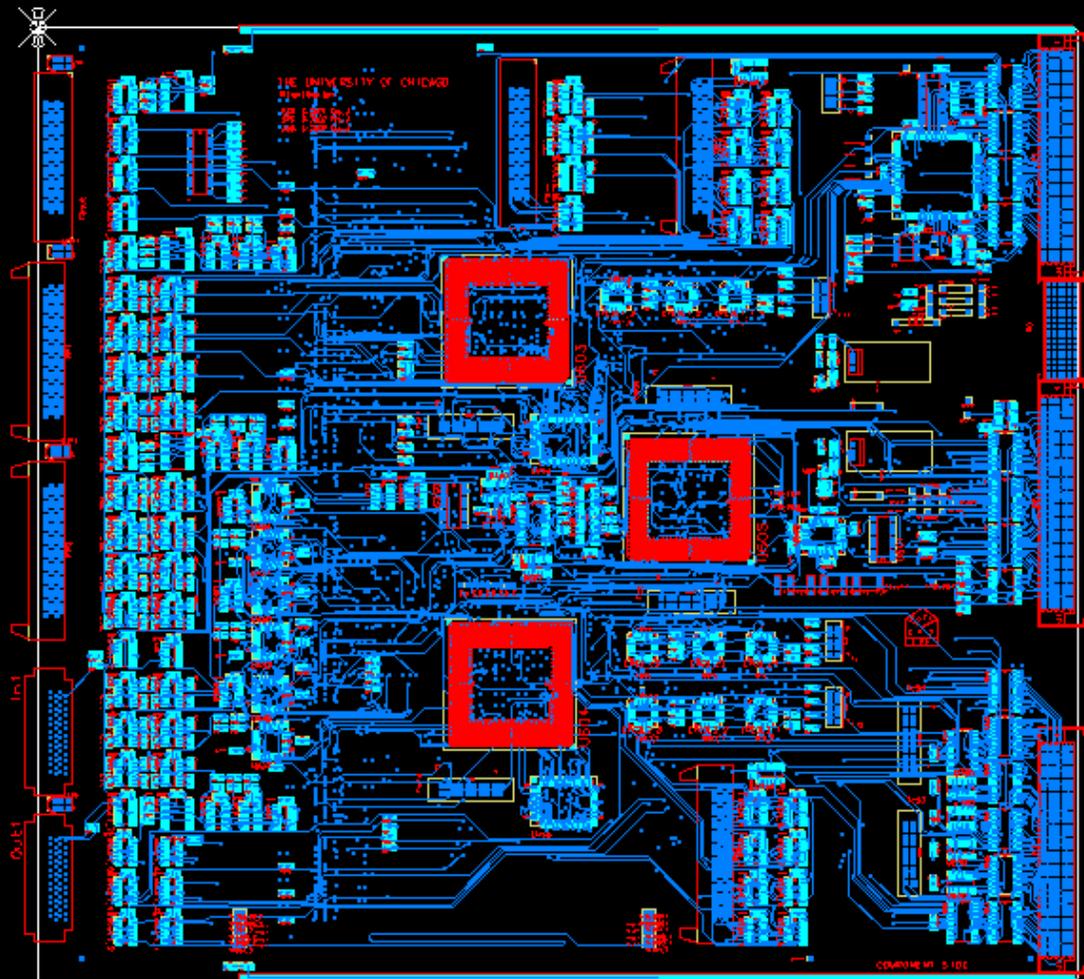


MGC File Geometries Setup Setup Placement Setup Routing Check Report Properties View Help Support

BO\$9UVME

V A I O R

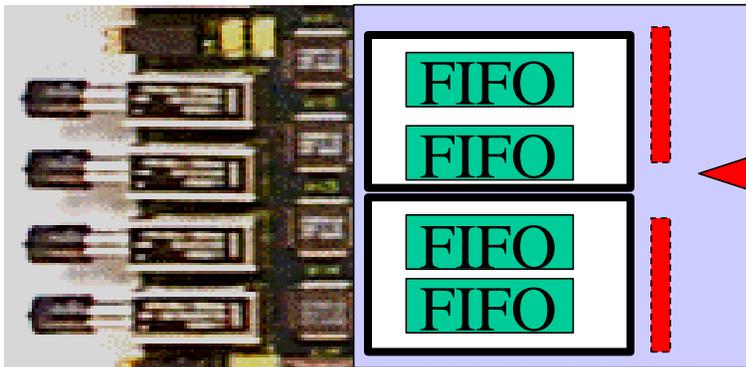
Selected: 0 Check On Components: 822 (0) Traces: 9189 (0) None 0.006  
Delta: 2.7539, -0.4635 Abs: 1.7, -16.05 In. Grid: X 0.025, Y 0.025 SIGNAL 1



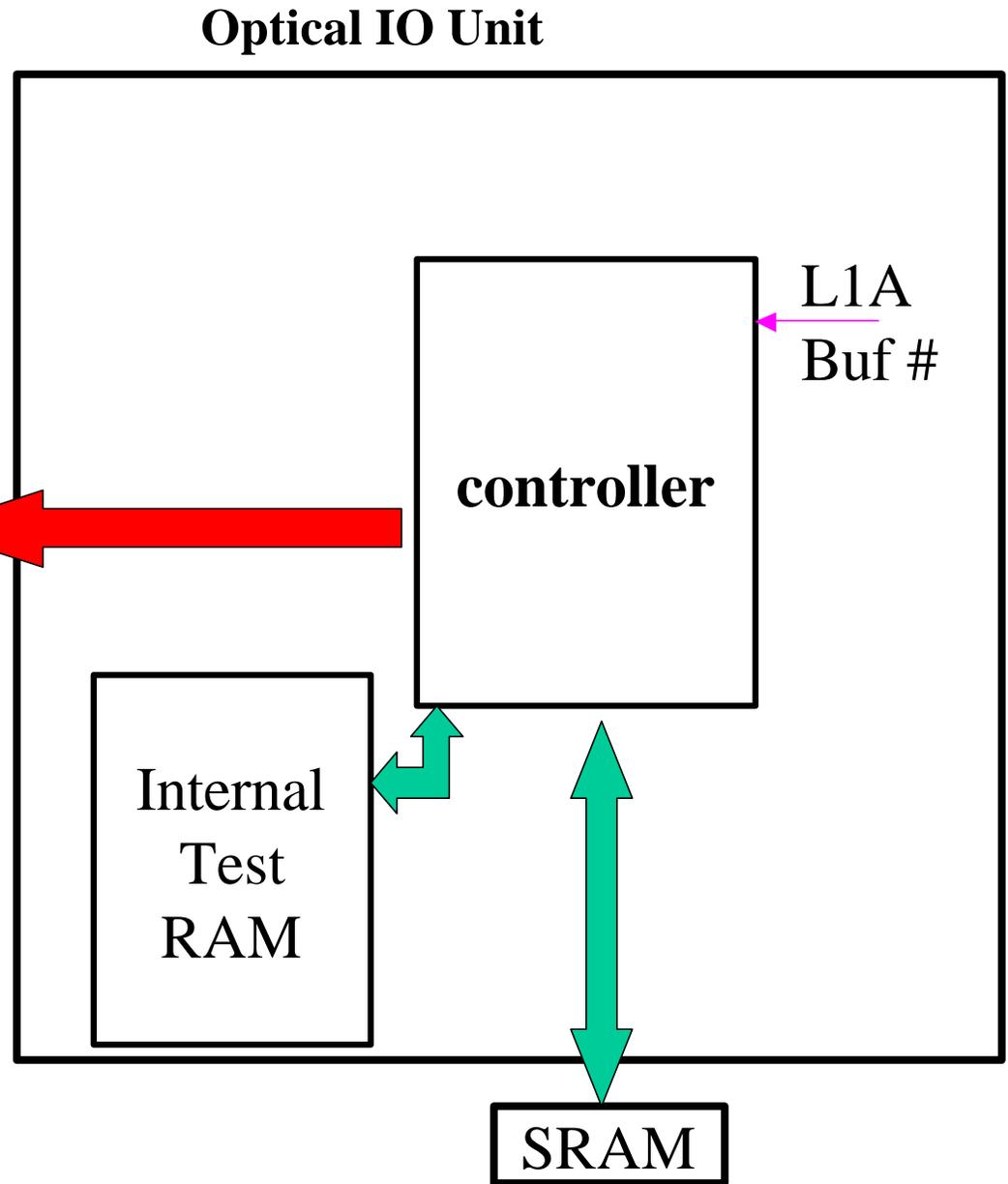
Pulsar layout

Pulsar in **pulser** mode:  
**hotlink examples:**

Muon case  
(only one mezzanine card shown)

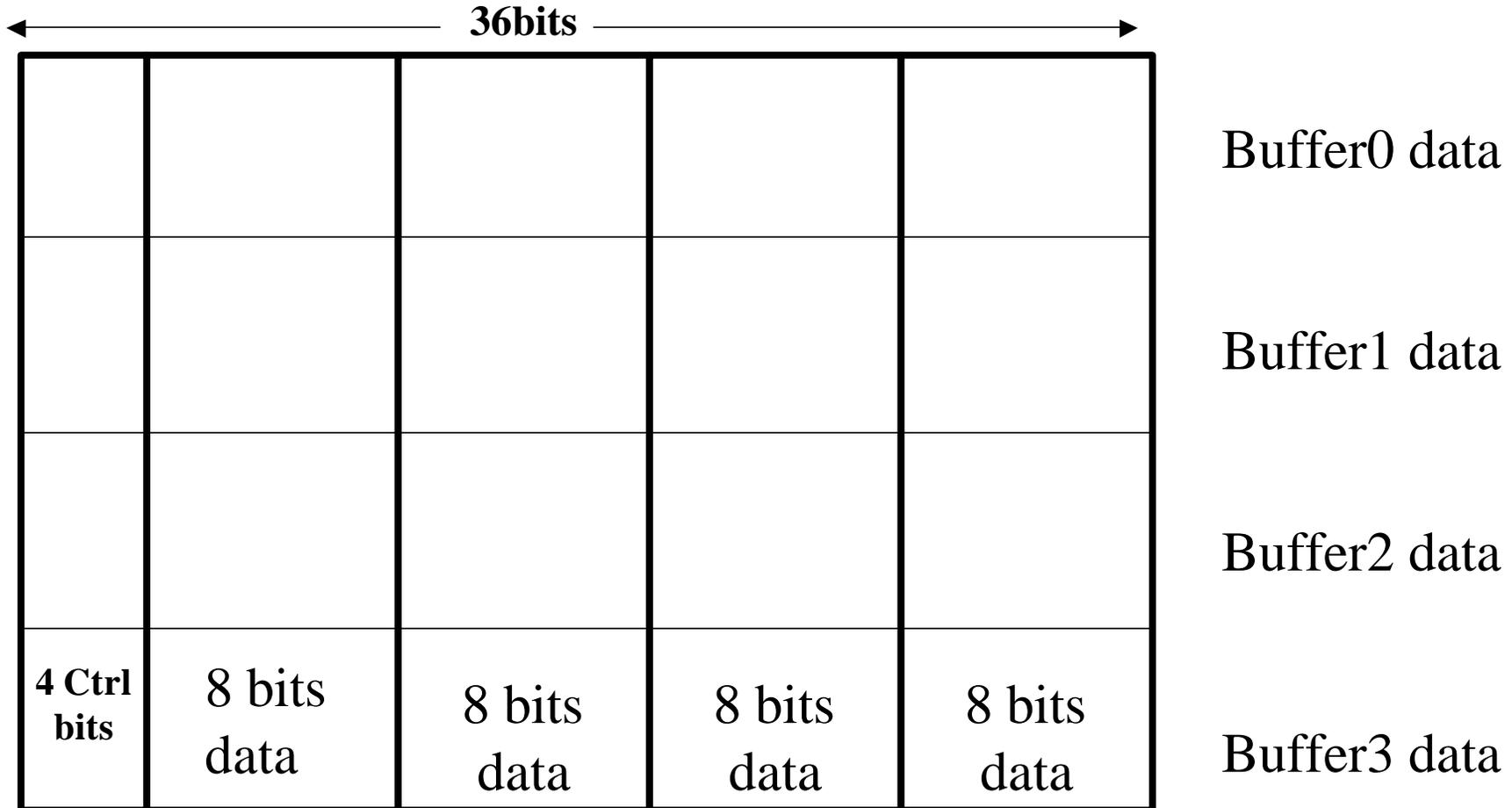


The latency is controlled  
by when the data is clocked  
out the FIFO



**load test pattern memory:**

use 36 bits data width, 32 will be for 4 fiber output (4 x 8), the highest 4 bits will be used as control bits to mark the content of data. For each event worth data, the first one will be the header, and the 32 bits data will contain the latency (&number of words etc) for this particular event and this particular path. The last one is the trailer, which can contain other info if needed (such as what L2 decision should be etc **(either use internal RAM or use 128K x 36 external SRAM, CY7C1350):**



**The highest two address bits will be controlled by buffer number to divide automatically the memory for 4 buffers**

**How does it work:**

- (1) after L1A, read the first word(header) and get the latency, at the same time start a counter;
- (2) continue to readout the rest of the data words from the memory and clock them into a FIFO, until the trailer is reached (can get the L2 decision information there)
- (3) once the counter reaches latency threshold, clock the data out from the FIFO at the speed which matches with the subsystem.

**this way the latency for each event and each data path can be individually controlled by user.**

header	Latency for this event, and other info			
	data 1 <sup>st</sup> event	data	data	data
trailer	Other information (what L2 decision should be etc)			

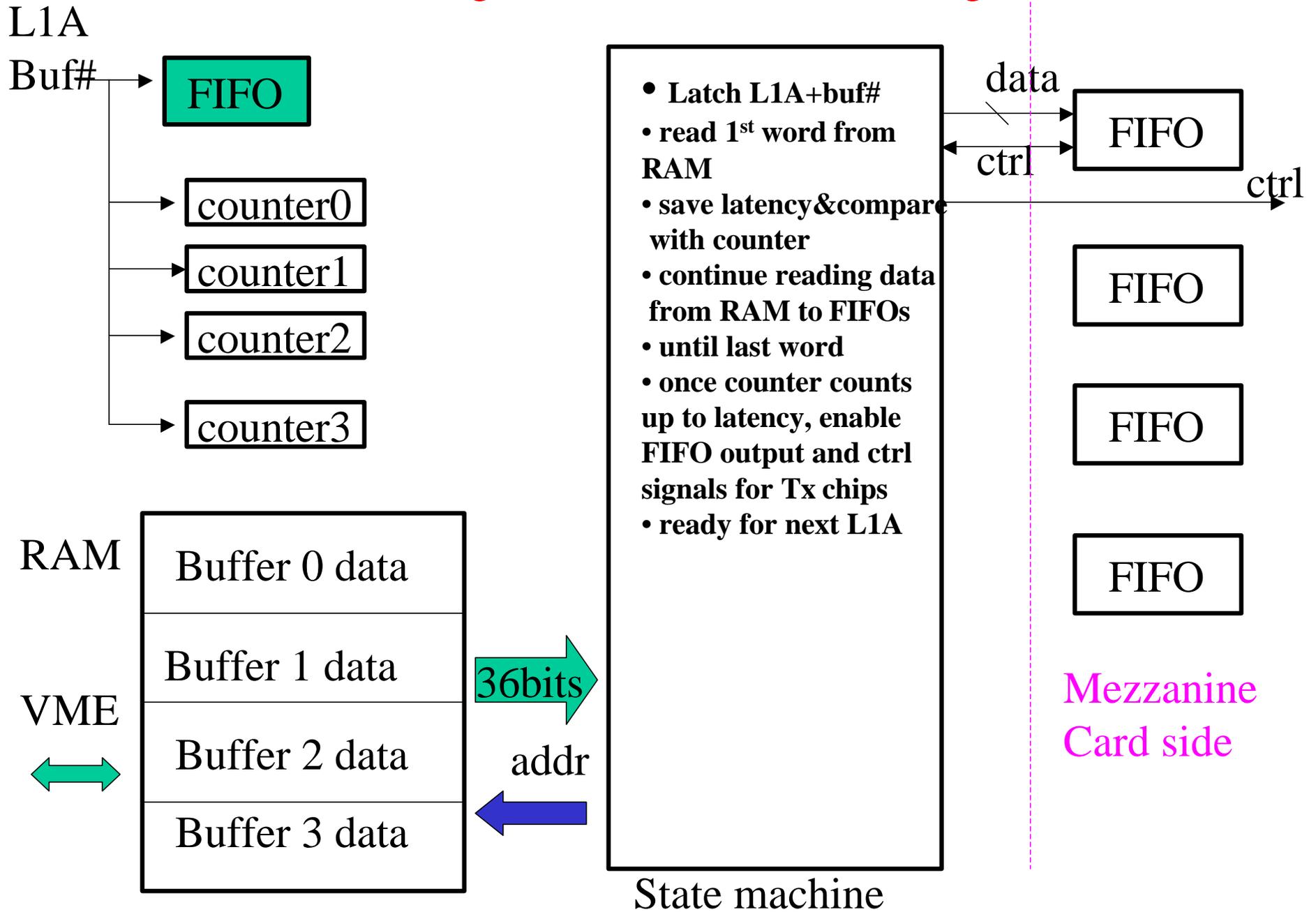
One could have more control by inserting gaps in between data words...etc using the 4 control bits, to better mimic the real situation for certain data paths.

**This approach seem to be quite flexible**

- Ctrl bit 35: header**
- Ctrl bit 34: trailer**
- Ctrl bit 33: gap**
- Ctrl bit 32: reserved**

Buffer 0 data memory

# Initial thoughts on tester firmware design



## Possible implementation A:

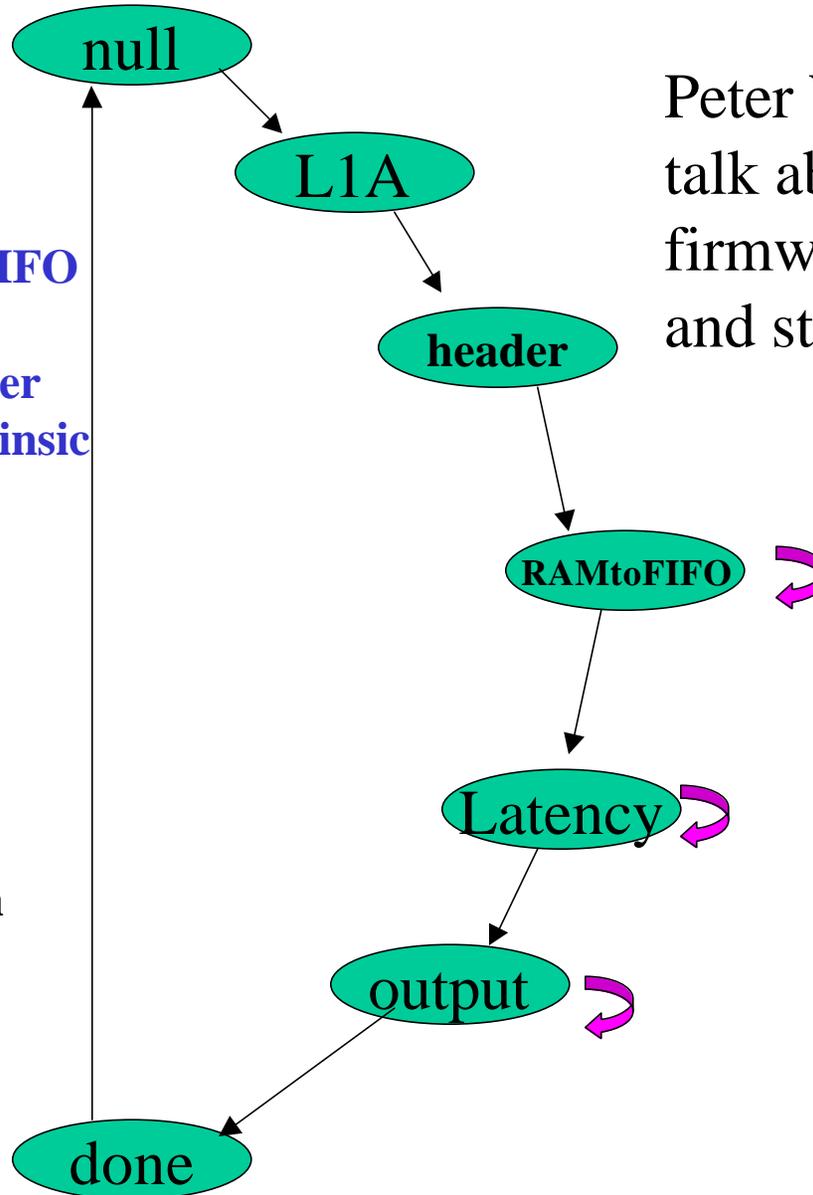
**Comments:**

**Pro:** simple

**Con:** not so elegant, as the state machine has to finish sending all data out of the FIFO before able to process next one. Maybe ok if run at higher clock rate. Will be some intrinsic delay between events.

**Good starting point, allow us to simulate the board soon.**

**Would be better to separate the RAM to FIFO part from the actual data sending part**



Peter Wittich will talk about **pulser** mode firmware design detail and status soon.

## Possible implementation B:

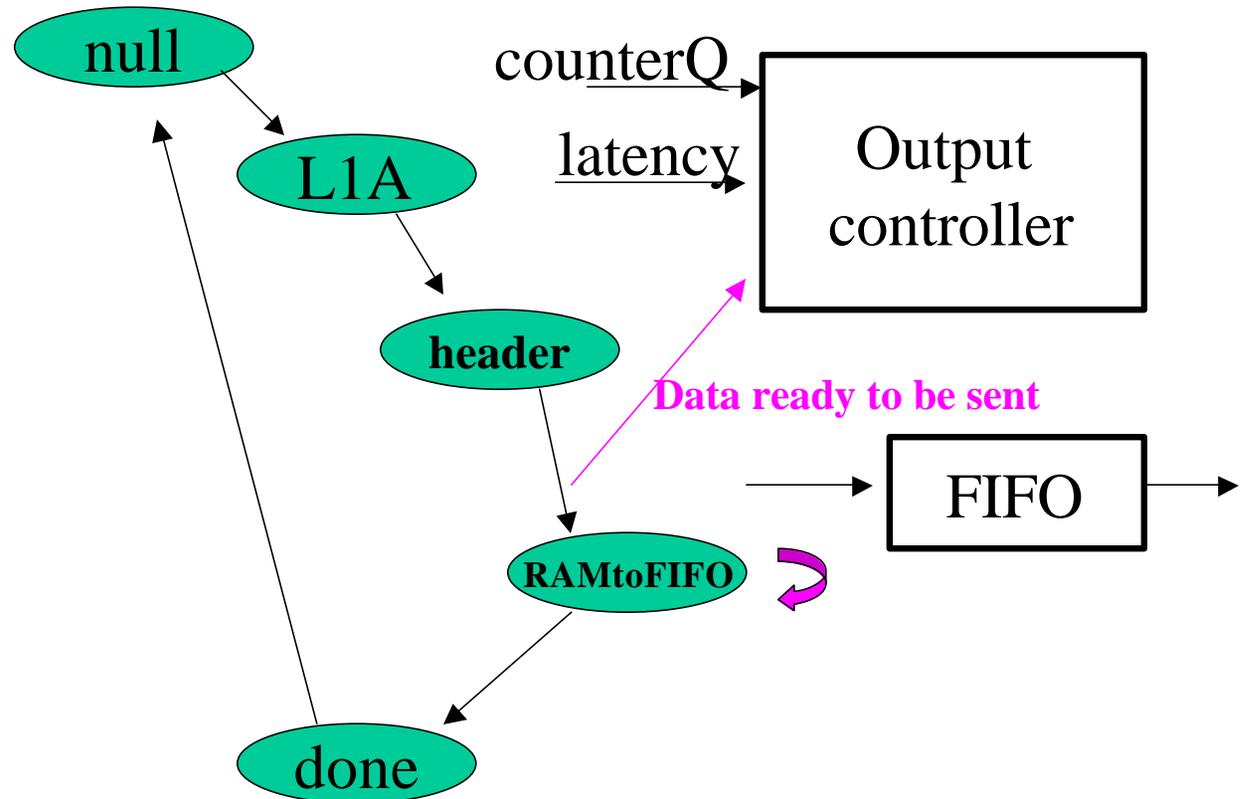
**Comments:**

**Pro:** more elegant

**Con:** somewhat more involved.

**Implement this later for the real thing.**

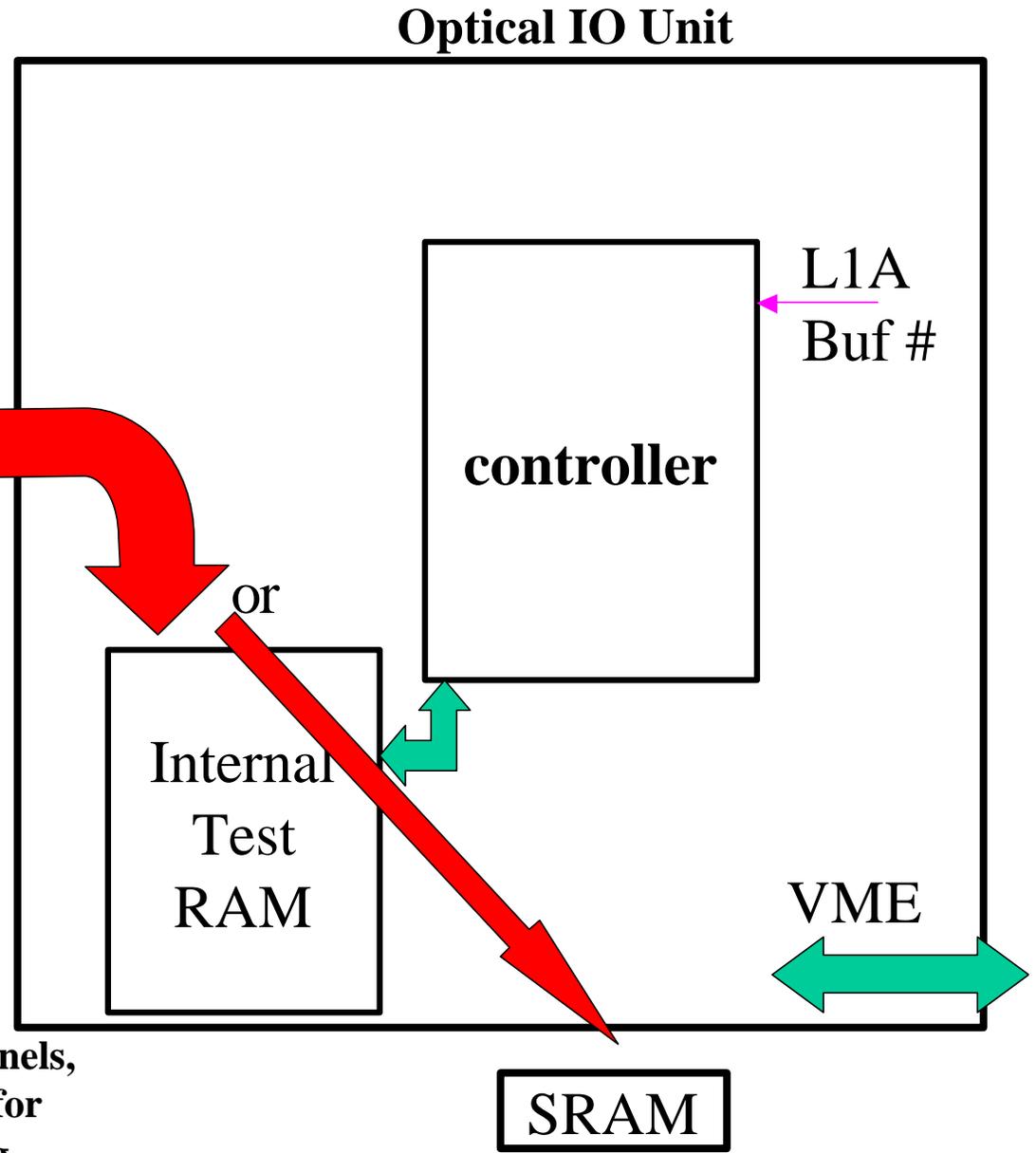
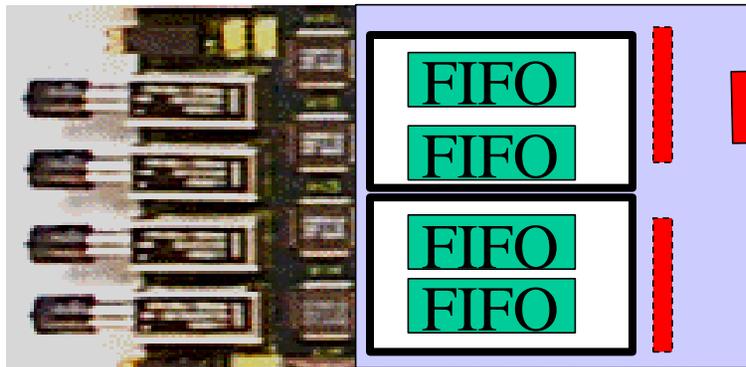
**We decided to go for implementation A first.**



# Pulsar in recorder mode (readout via VME)

hotlink examples:

(only one mezzanine card shown)

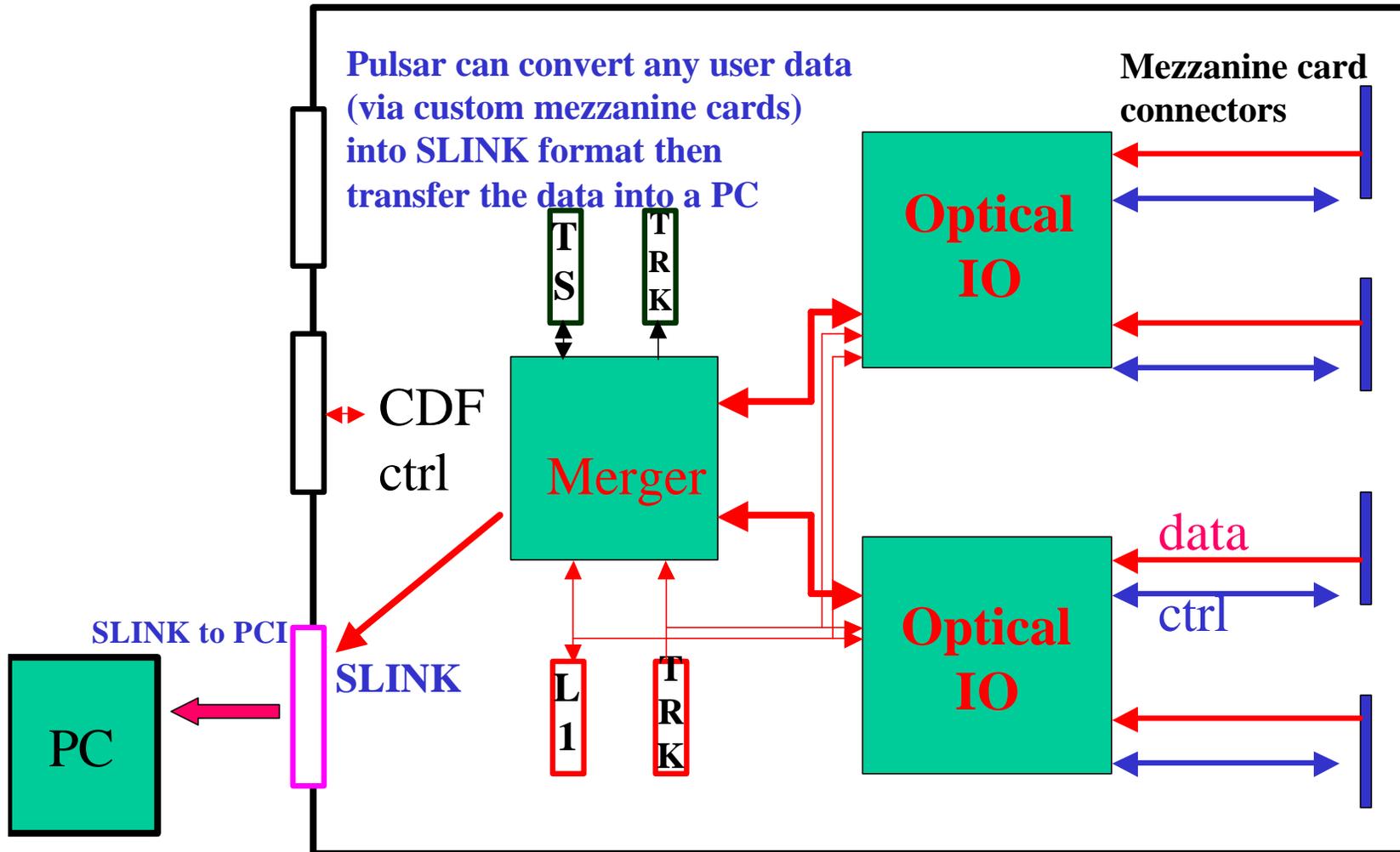


Configure the (S)RAM as a circular buffer for recording (for each L1A) and can be stopped and read out via VME.

Each Optical IO FPGA looks at 8 fiber channels, SRAM has 32+4 bits. So need ping-ponging for recording (recording is at twice the incoming data rate, 60MHz)

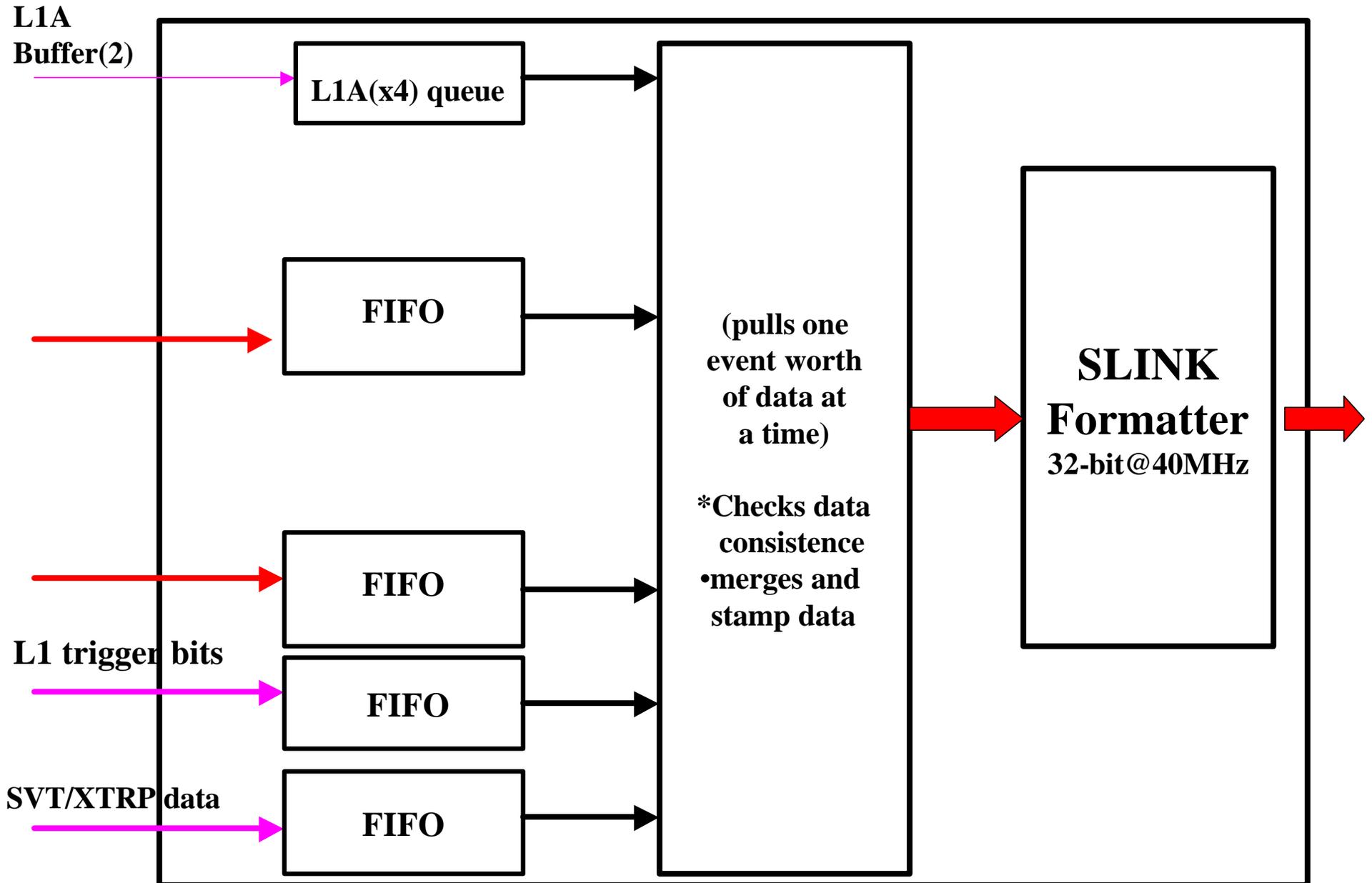
Natalia is working on this part of firmware

# Pulsar in (general purpose) recorder mode (directly into a PC)



**Firmware:** this mode exercises the whole board. The core firmware has been written in this mode and we have been simulating the whole board this way since April. Will talk about the details later. The firmware in this mode can be used initially to test the prototype board by using SLINK test tools.

**Pulsar in recorder mode(into a PC): firmware design is similar to all three FPGAs**





**Pulsar firmware in CVS**

- common: library for lower level VHDL code
- fpgapinmap: IO pin assignment files, compile setting files, VHDL templates etc
- Rx: VHDL code in various receiving modes
- Tx: VHDL code in various pulser modes

**crucial for team work and long term maintenance**

Pulsar is designed for long term maintenance for Level 2

## Possible applications for Pulsar

- **As Pulser for L2 decision crate:**
  - can source any data path as well as multiple paths at the same time
- **As Recorder for L2:**
  - can record data from upstream for any data path (or multiple paths)
- **As Pulser for Hit-Finder boards in SVT system:**
  - with a **G-LINK mezzanine card**, Pulsar can pulse SVT system by sending **fiber data** into **Hit Finder boards**:
    - \* can receive SVT cable input from Hit Finder output (for on-the-fly loop test)
- **Can sink/source G-link/TAXI/HotLink/LVDS data for generic DAQ/trigger diagnostics**
- ....

This could be important for long term maintenance for the system

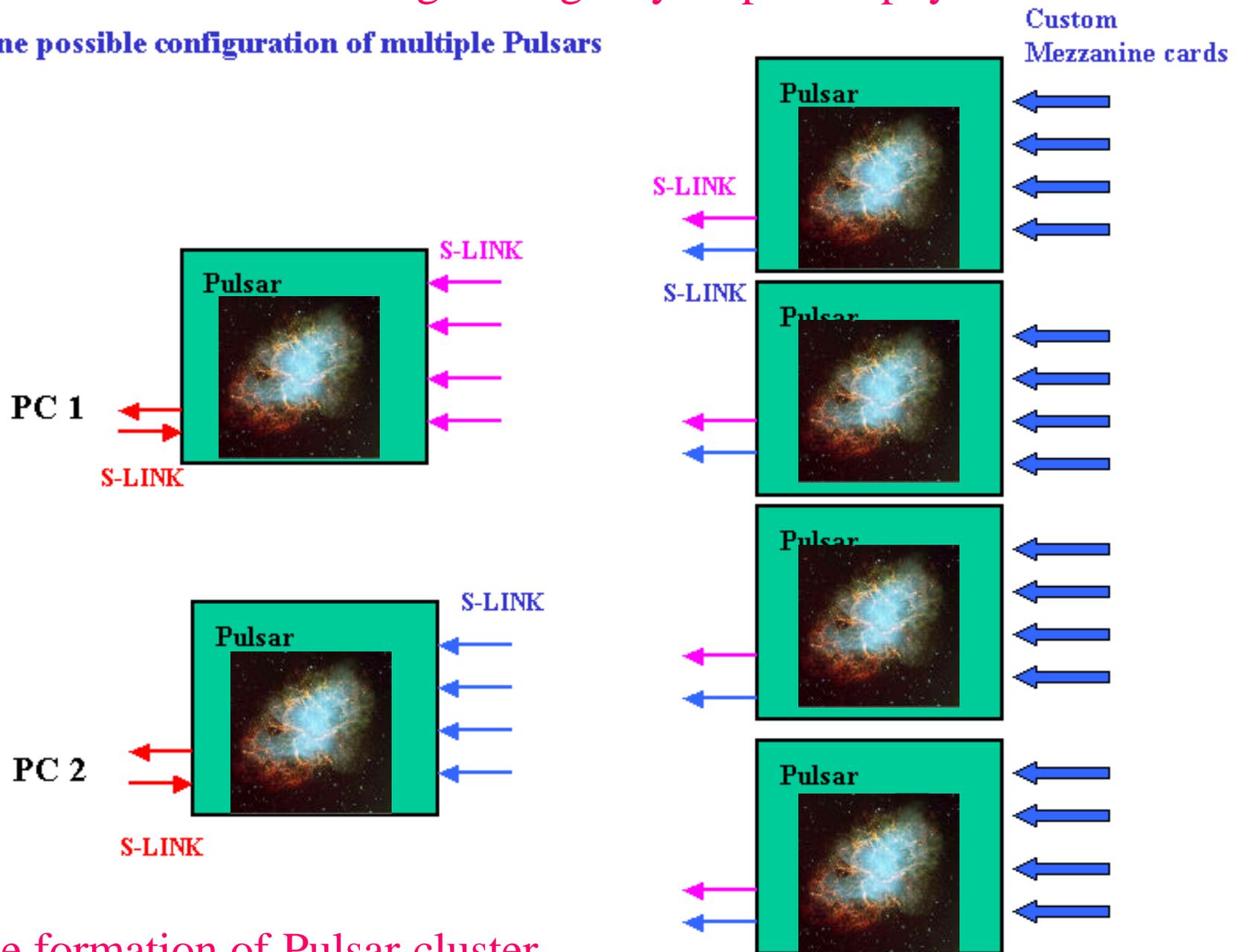
### Other possible/potential applications:

- As a simple standalone DAQ system (in a test beam environment with custom mezz cards)
    - can receive external trigger signals (NIM etc) via AUX card in the back
  - maybe possible to use it as a general diagnostics tool for beams division...?
  - Future expansion is as cheap/fast/easy as designing a mezzanine card .....
- the rest are all commercially available ...**

The flexible design (“lego style”) makes it possible to use Pulsar as a general purpose tool within or outside CDF ...

# Flexible design: “Lego style” philosophy

One possible configuration of multiple Pulsars



The formation of Pulsar cluster

## Board Level simulation and prototype testing plan

**Pulsar Mezzanine cards:** hotlink Tx and Rx mezzanine cards have been simulated together, has a teststand setup at UC for prototype testing.

**Pulsar motherboard:**

### Board Level simulation:

- intensive board level simulation in progress
- prepare for multi-board simulation: Pulsar + mezzanine cards
- schedule depends on board level simulation work...
- the goal is to validate the design with **INTENSIVE** board level simulation by the end of June. Send out the prototype early July, and continue board level simulation...
- a new visiting student (**Sakari Pitkanen**) from Finland just joined this effort

### Prototype testing plan:

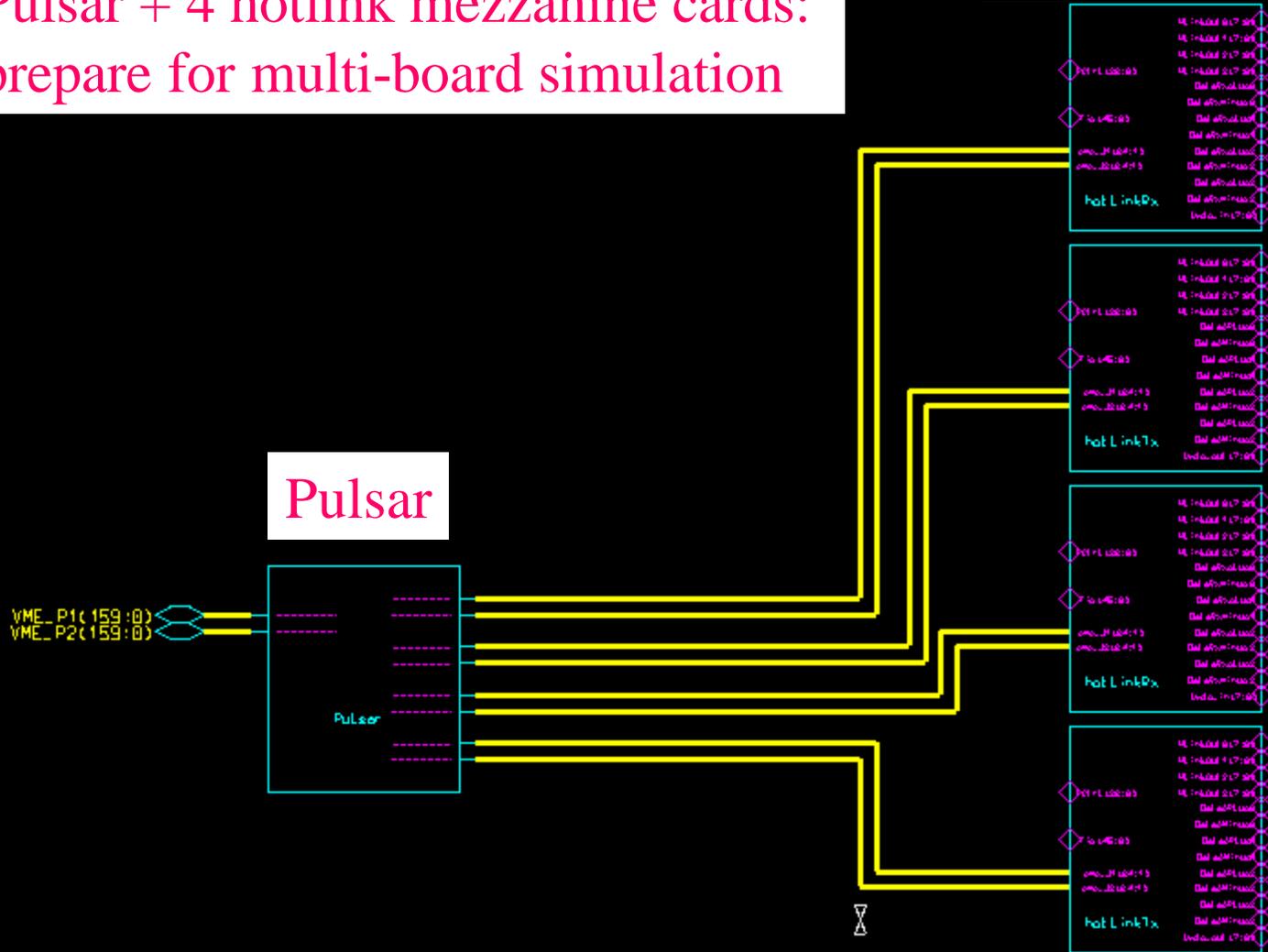
- can use SLINK test tools first
- then test with custom mezzanine cards





Pulsar + 4 hotlink mezzanine cards:  
prepare for multi-board simulation

Mezzanine cards



Pulsar

VME\_P1(159:0)  
VME\_P2(159:0)

hot Link0x

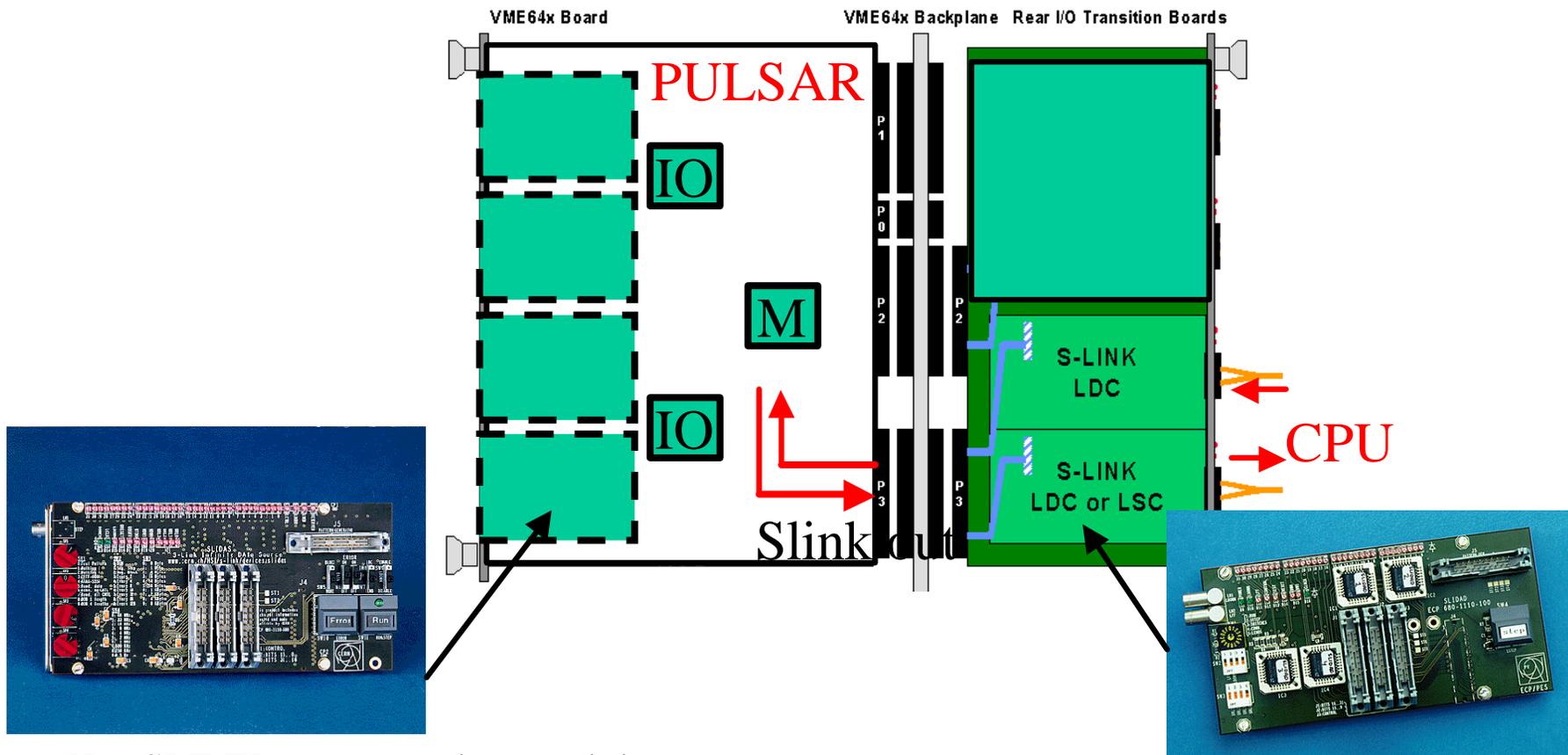
hot Link1x

hot Link2x

hot Link3x

## Initial test plan for Pulsar board prototype

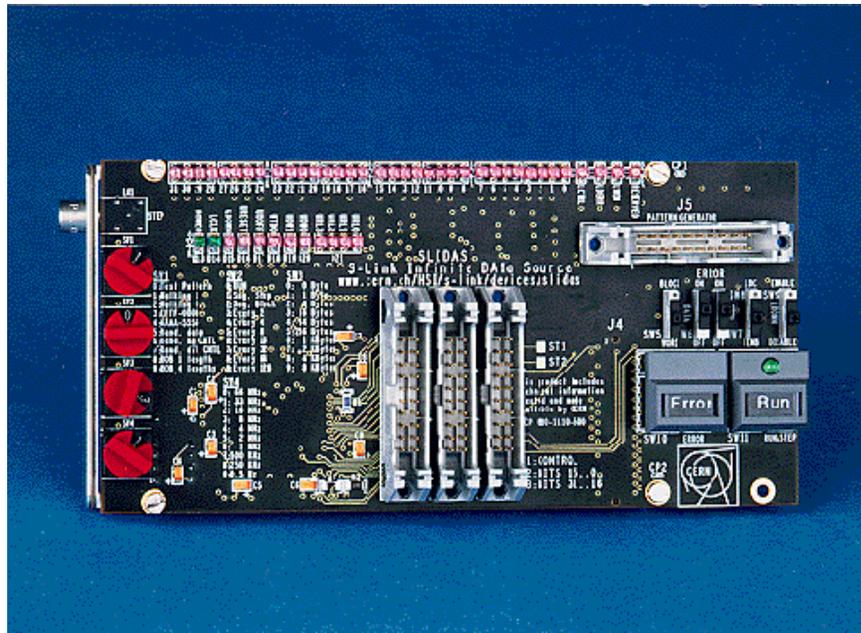
Pulsar board prototype can be first tested with SLINK test tools, then can be tested with custom mezzanine cards



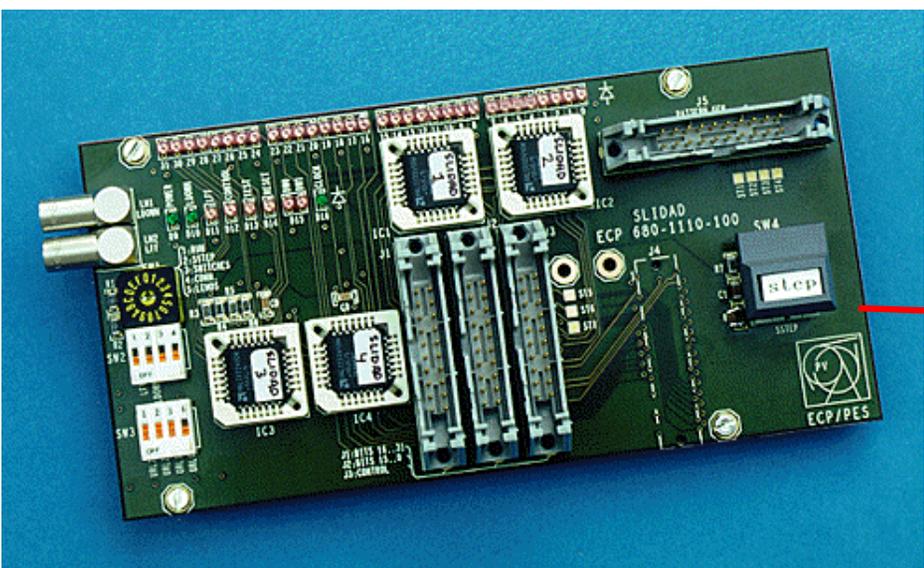
Use SLINK source card to send data

Use SLINK data sink to check data

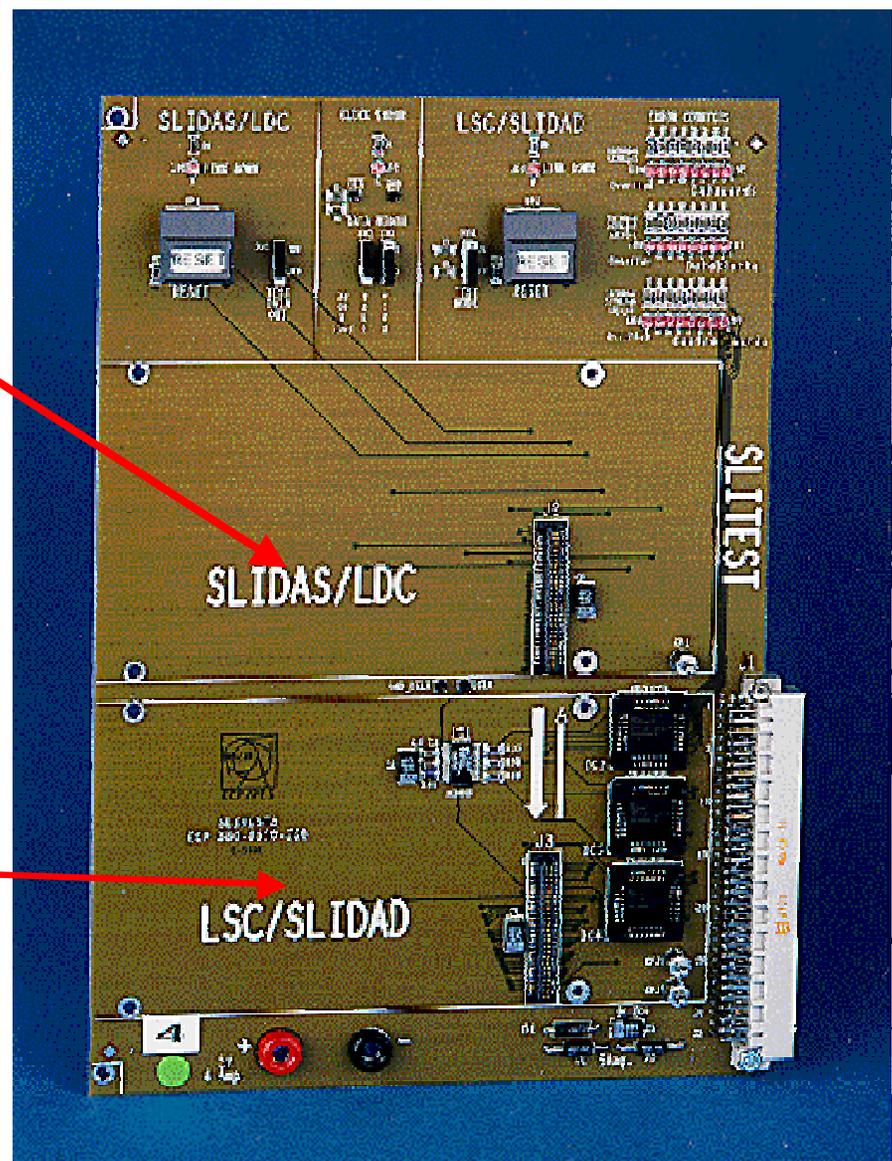
SLIN data source test board



(ideal for initial Pulsar prototype testing)



SLINK data Drain test board



## Prototype test plan II: use one Pulsar prototype board

this would allow full tests (including the CMC connectors)

