



Pulsar Status: *what has been done since May 10th*

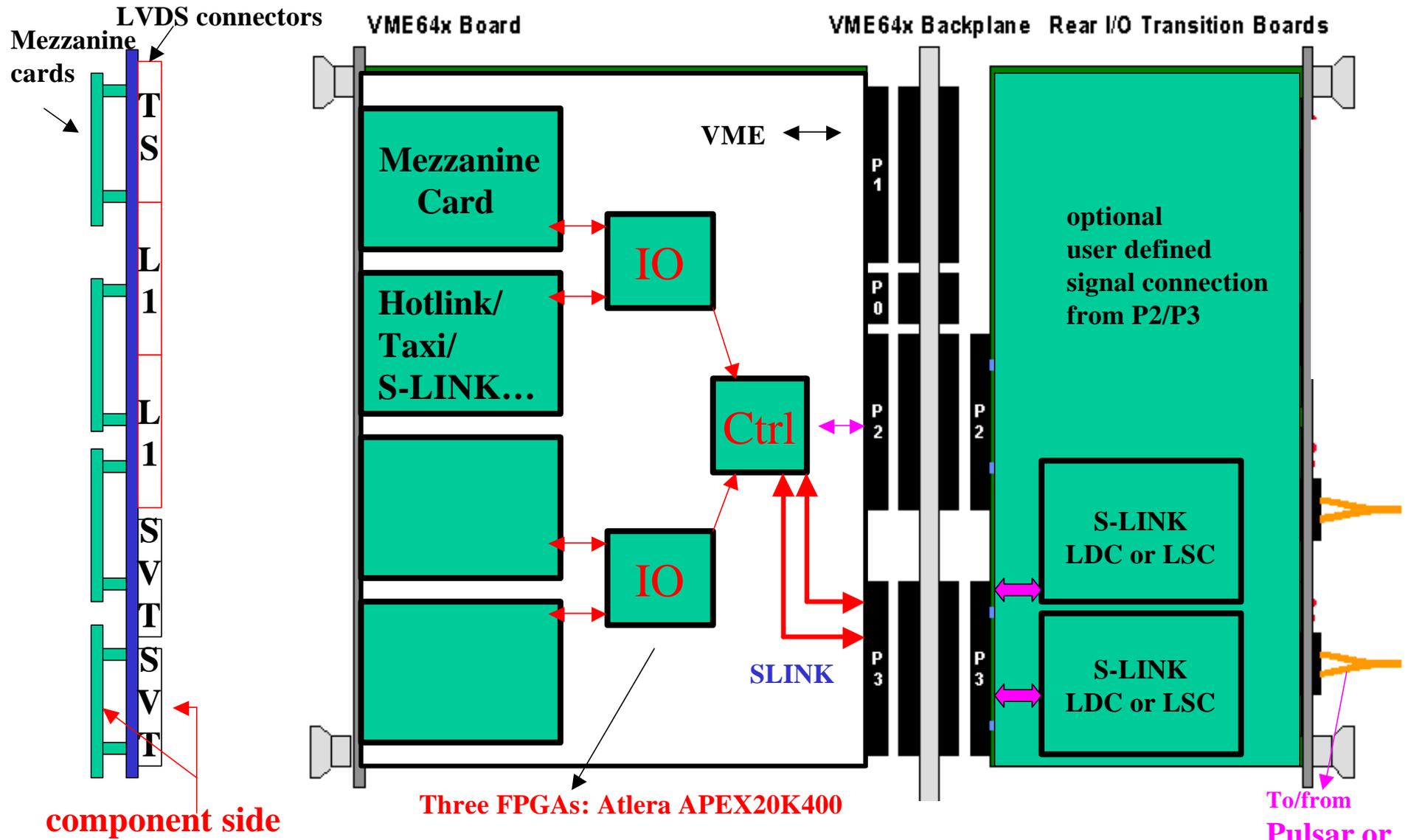
- hotlink mezzanine cards (Tx and Rx) testing finished successfully (Natalia/Peter)
- Pulsar schematics finalized and carefully checked by hand (Mircea/TL)
- Pulsar component placement **optimized for routing** (Mircea/TL)
- 1st round routing finished and trace analysis starts (Mircea)
- **intensive board level simulation successfully done** (Sakari Pitkanen supervised by TL)
 - (1) “boundary scan” to check the connectivity for **every** connector pin to each FPGA for the **entire** board;
 - (2) VME access to all FPGAs (internal registers, internal RAMs etc) and on board external SRAMs are done. Initial VME address map in place;
 - (3) SLINK merger firmware has been modified to be able to receive data from hotlink mezzanine cards
 - (4) **successfully simulated one Pulsar (in Rx mode) with eight daughter cards together**
- SLINK (to PCI) software for Pulsar prototype testing **is ready**, lots progress made. more work in progress (Derek Kingrey with help from Peter)

Summer student from Cornell

(TL) Friday Trigger Meeting, June 28, 2002

Front-panel (double width)

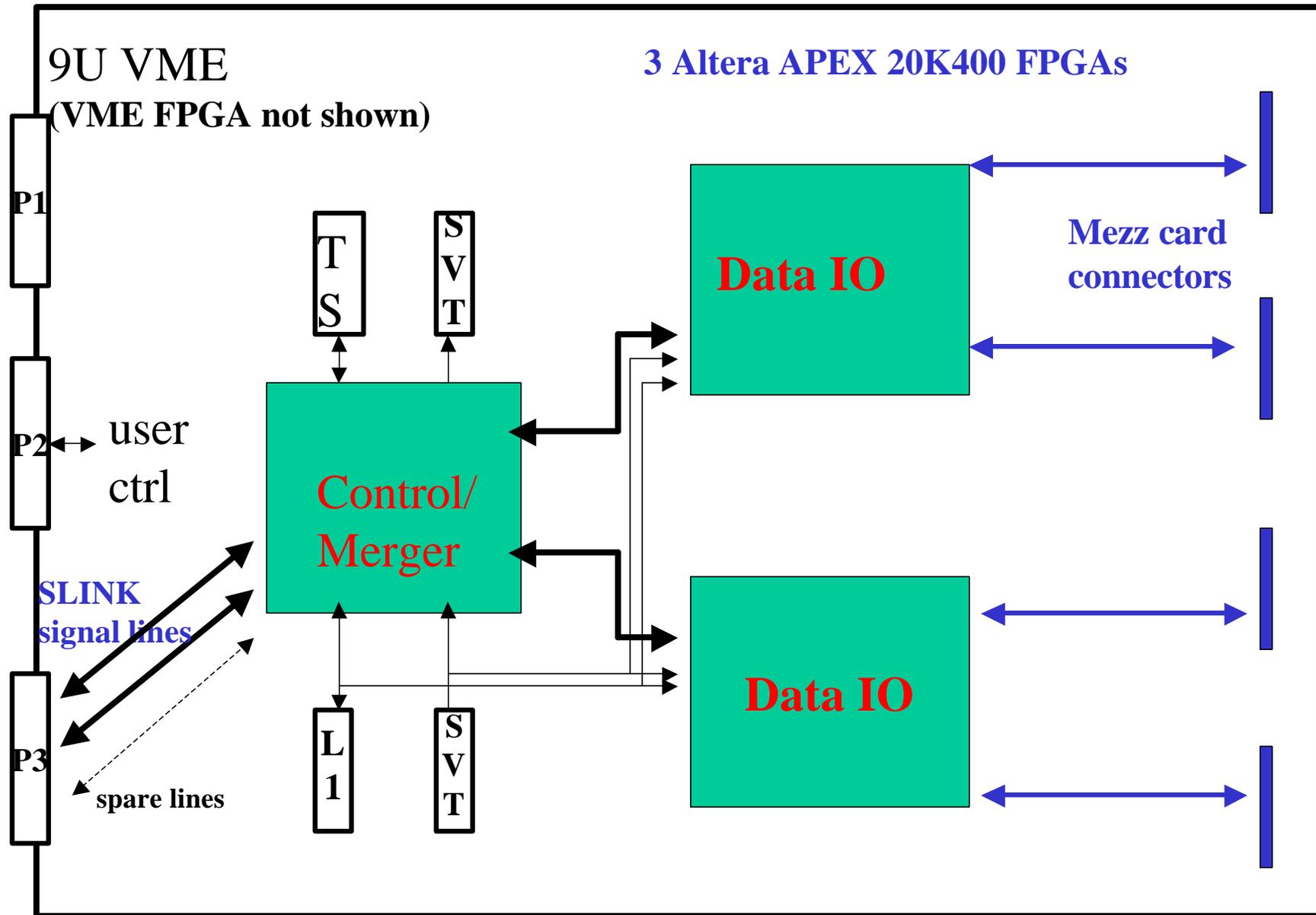
PULSAR design



The mezzanine card connectors can be used either for user I/O or SLINK cards

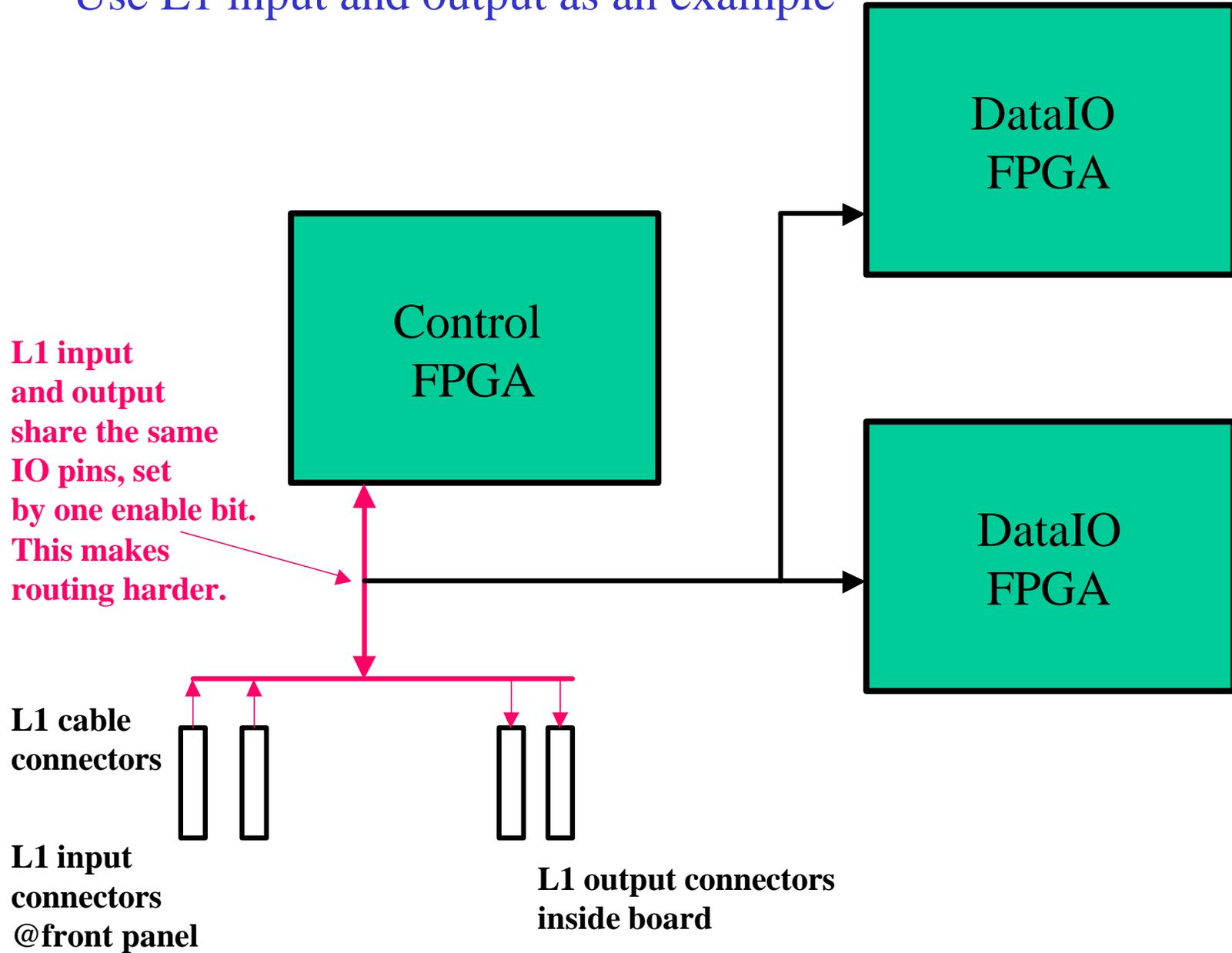
To/from Pulsar or a PC

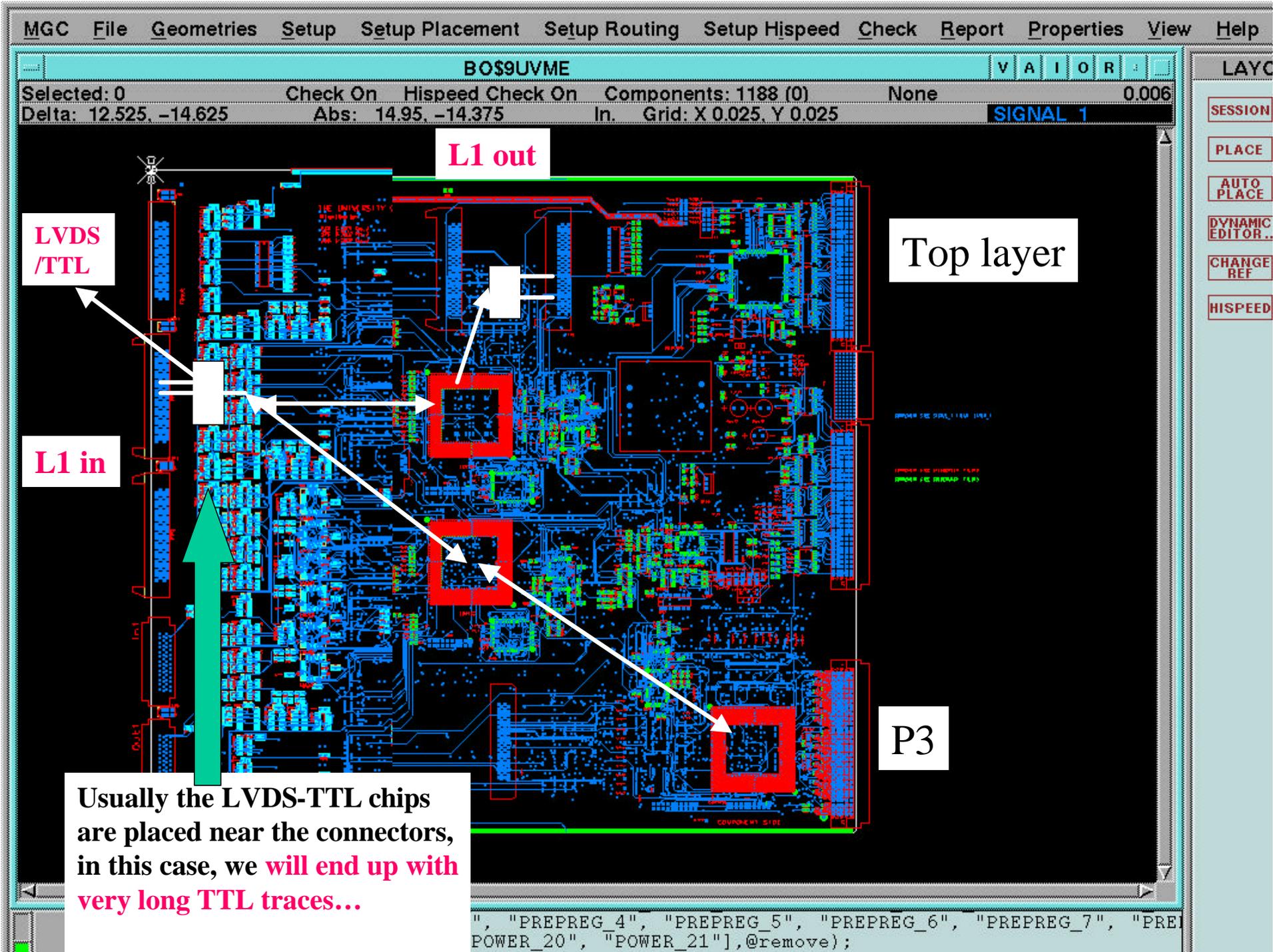
Pulsar design (general purpose tool)



optimized component placement for routing

Use L1 input and output as an example





LVDS /TTL

L1 in

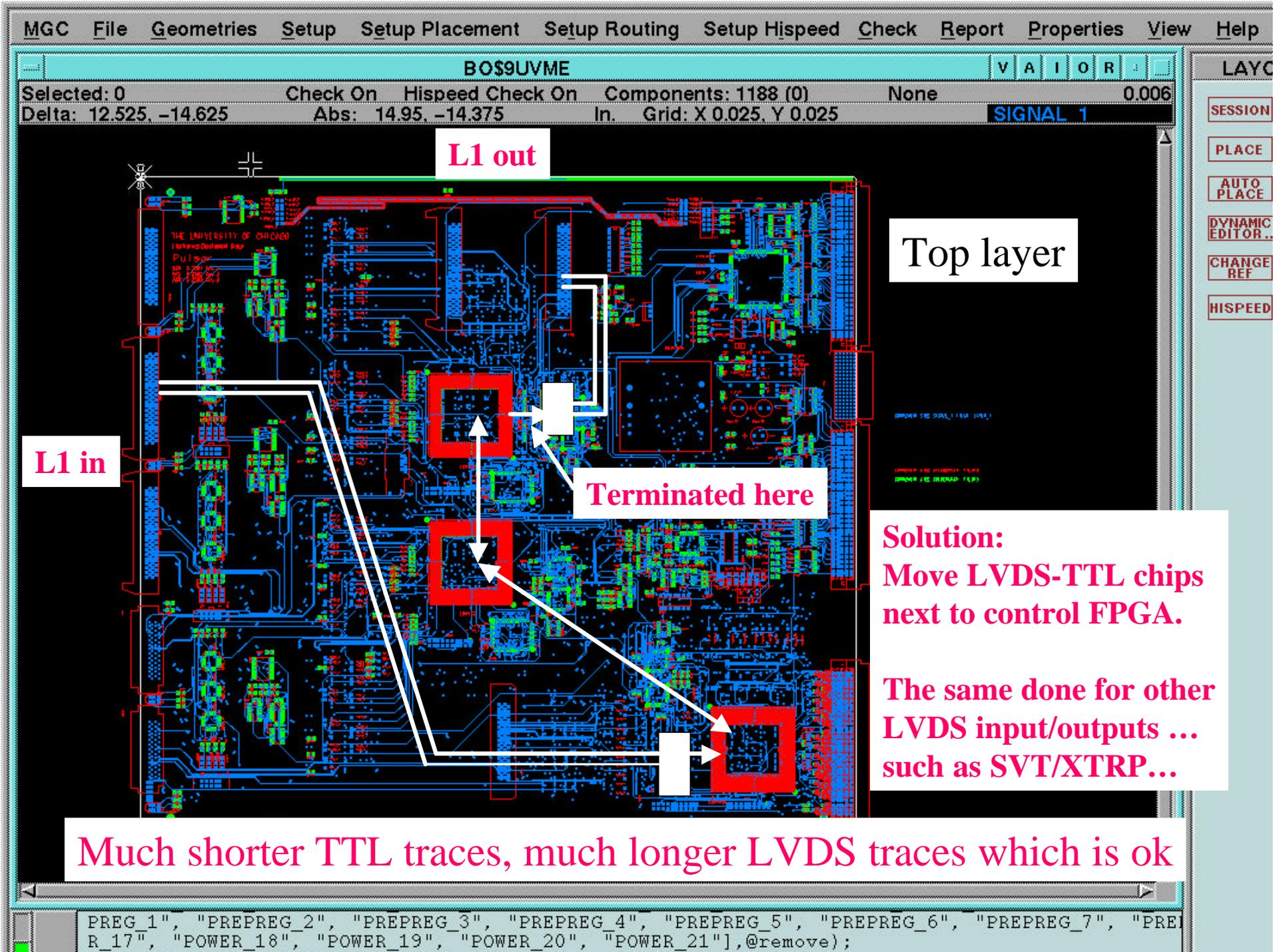
L1 out

Top layer

P3

Usually the LVDS-TTL chips are placed near the connectors, in this case, we will end up with very long TTL traces...

","PREPREG_4", "PREPREG_5", "PREPREG_6", "PREPREG_7", "PREPREG_8", "PREPREG_9", "PREPREG_10", "PREPREG_11", "PREPREG_12", "PREPREG_13", "PREPREG_14", "PREPREG_15", "PREPREG_16", "PREPREG_17", "PREPREG_18", "PREPREG_19", "PREPREG_20", "POWER_21"],@remove);



Top layer

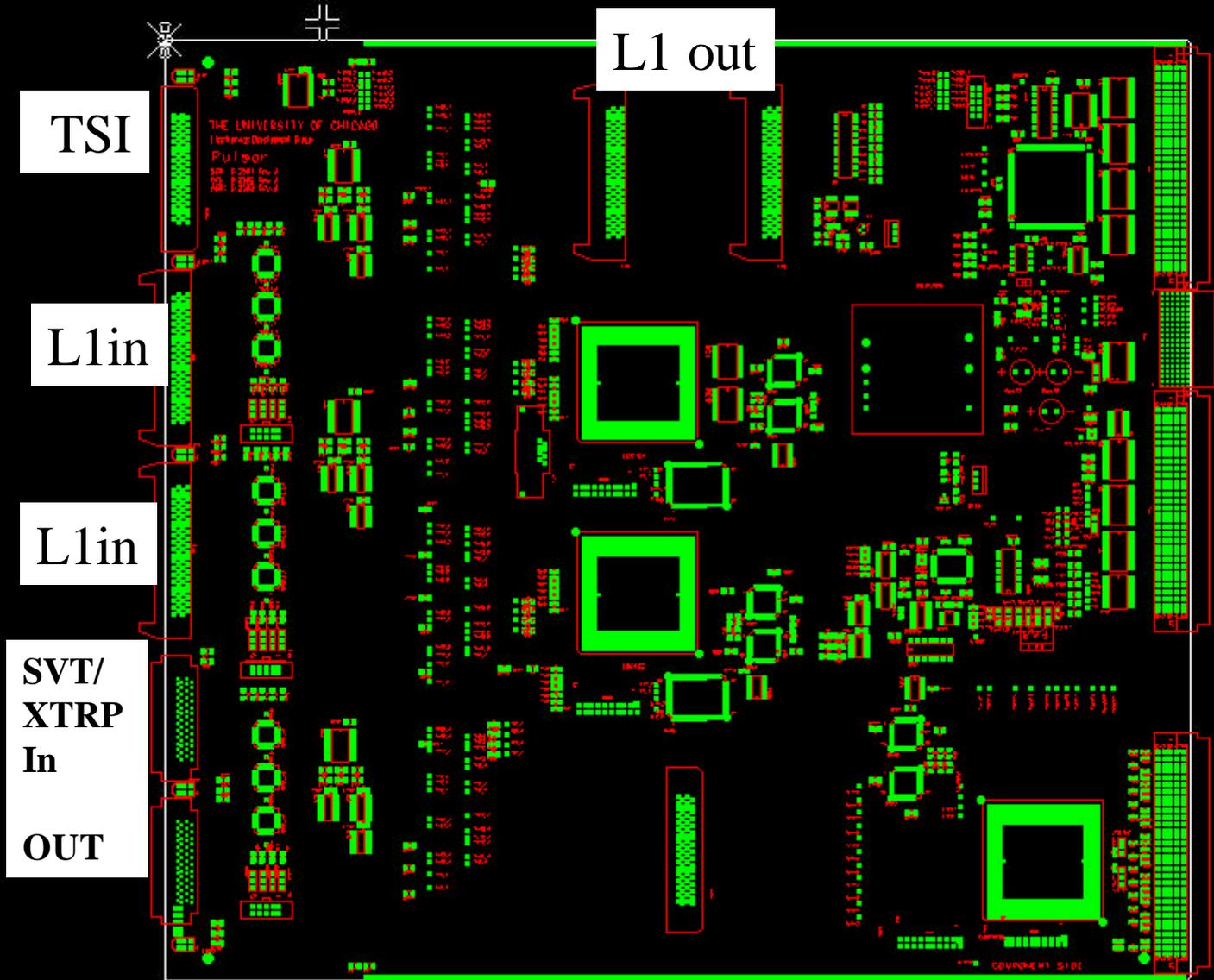
Solution:
Move LVDS-TTL chips next to control FPGA.
The same done for other LVDS input/outputs ... such as SVT/XTRP...

Much shorter TTL traces, much longer LVDS traces which is ok

BO\$9UVME

V A I O R

Selected: 0 Check On Hspeed Check On Components: 1188 (0) None 0.0
Delta: 14.975, -11.425 Abs: 17.4, -11.175 In. Grid: X 0.025, Y 0.025 SIGNAL 1



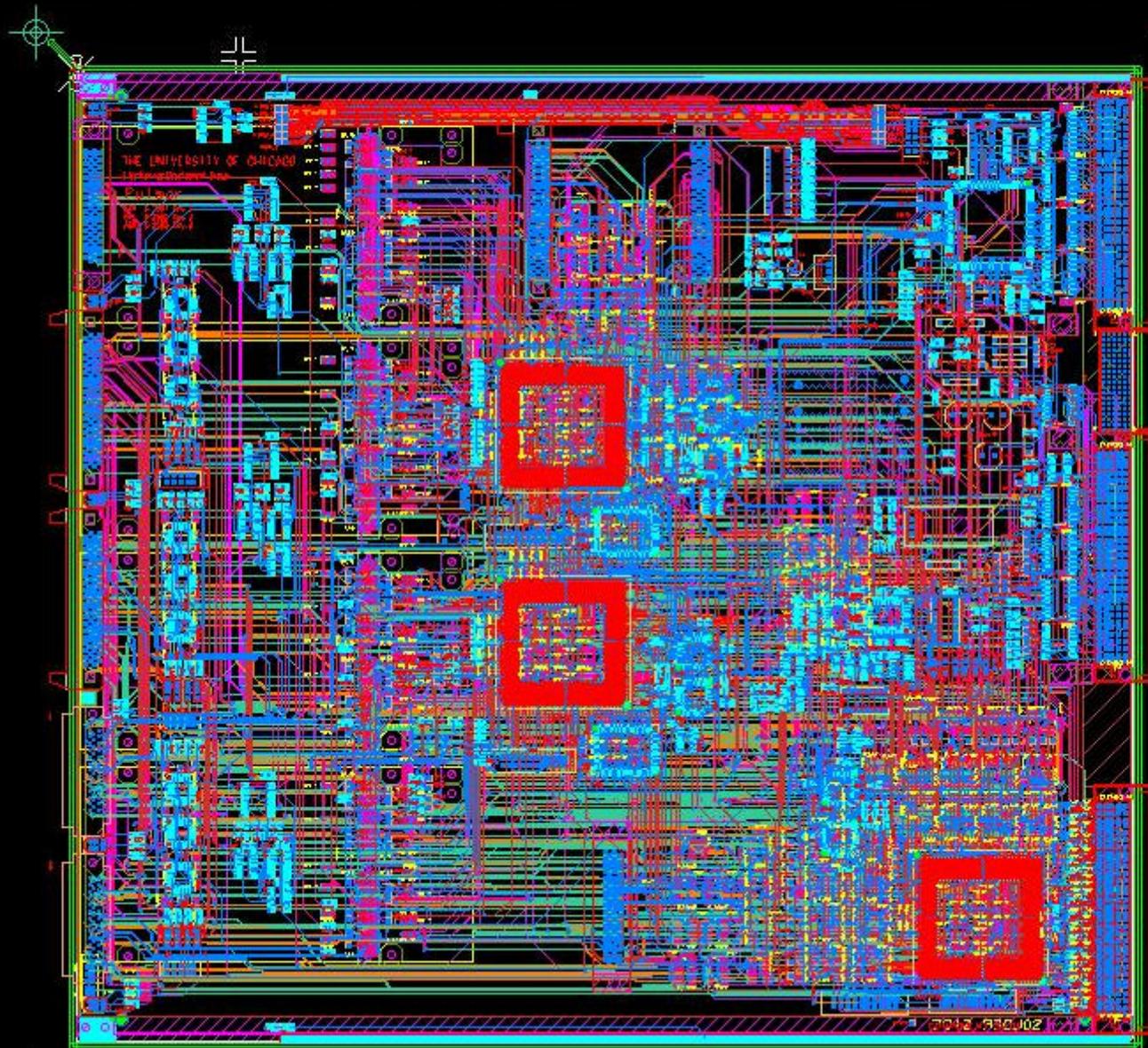
Top placement

MGC File Geometries Setup Setup Placement Setup Routing Setup Hispeed Check Report Properties

BO\$9UVME

V A I O R

Selected: 0 Check On Hispeed Check On Components: 1188 (0) None 0.0
Delta: 14.65, -9.05 Abs: 17.075, -8.8 In. Grid: X 0.025, Y 0.025 SIGNAL 1



ALL layers.
Finished layout.
Trace analysis
just started.

High
Density
PCB
Trace
Analysis
Results
Report

High Density PCB Trace Analysis Results Report

Analysis Date: 10/10/2001 10:00:00 AM

Board Name: BO\$9UVME

Analysis Type: High Density PCB Trace Analysis

Analysis Results:

- Analysis completed successfully.
- Analysis results are displayed on the screen.
- Analysis results are also saved to the file: BO\$9UVME.HDR

Analysis completed successfully.

This slide is from last talk on May 10th. Now we have achieved all our goals set back then.

Board Level simulation

Pulsar motherboard:

Board Level simulation:

- intensive board level simulation in progress
- prepare for multi-board simulation: Pulsar + mezzanine cards
- schedule depends on board level simulation work...
- the goal is to validate the design with **INTENSIVE** board level simulation by the end of June. Send out the prototype early July, and continue board level simulation...
- a new visiting student (**Sakari Pitkanen**) from Finland just joined this effort



Pulsar board level simulation

Sakari will talk about the details later.

- **intensive board level simulation successfully done**

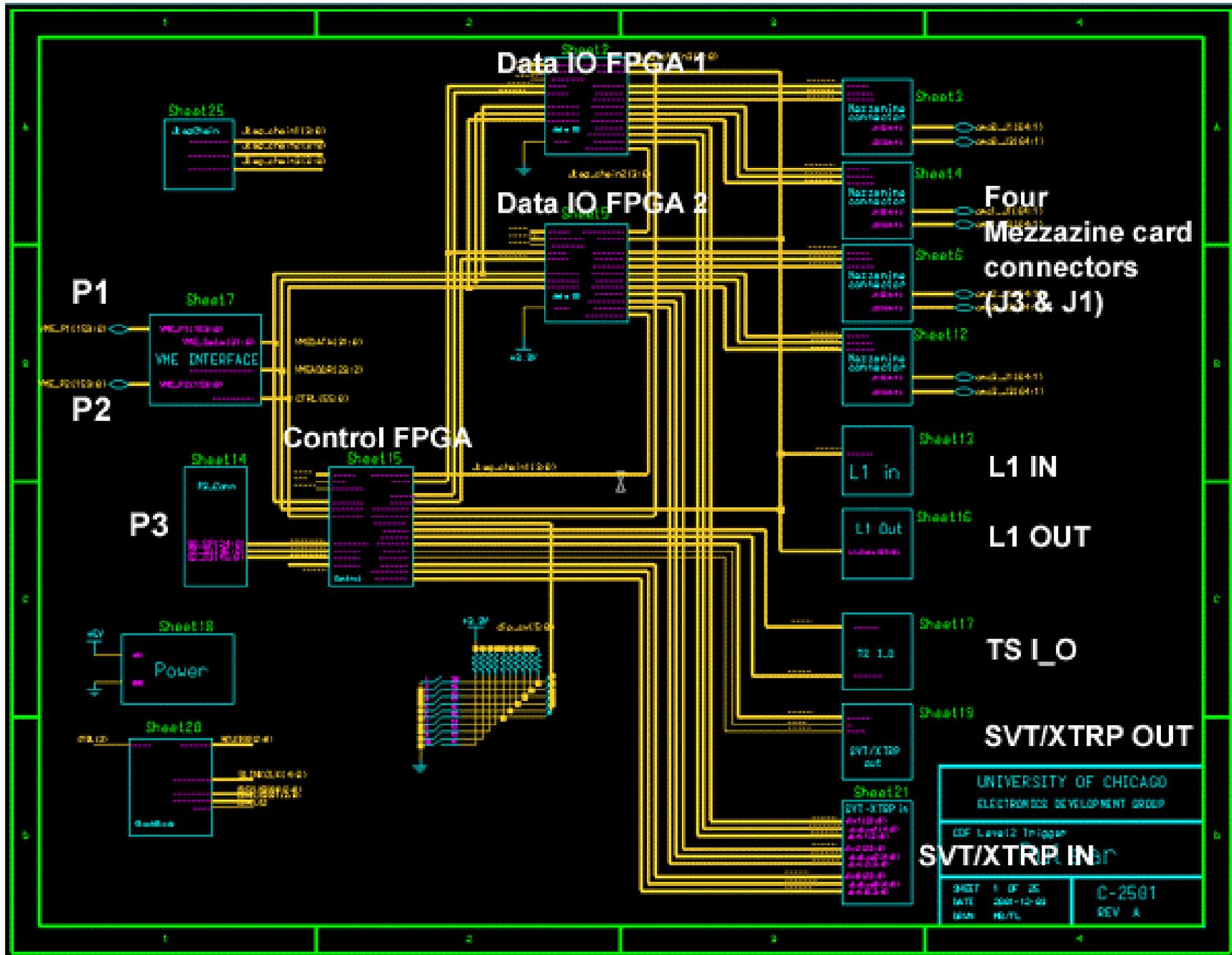
- (1) “boundary scan” to check the connectivity between **every** connector pin and each FPGA for the **entire** board: all mezzanine card connector pins, L1 input/output connector pins, TS connector pins, SVT/XTRP input and output connector and external FIFOs, all P2 backplane CDF ctrl signals, all used P3 connector pins.
- (2) VME access to all FPGAs (internal registers, internal RAMs etc) and on board external SRAMs are done. Initial VME address map in place;
- (3) SLINK merger firmware has been modified to be able to receive data from hotlink mezzanine cards
- (4) **successfully simulated one Pulsar (in Rx mode) with eight daughter cards together**

All simulation results are documented (incl. scripts, setups etc)

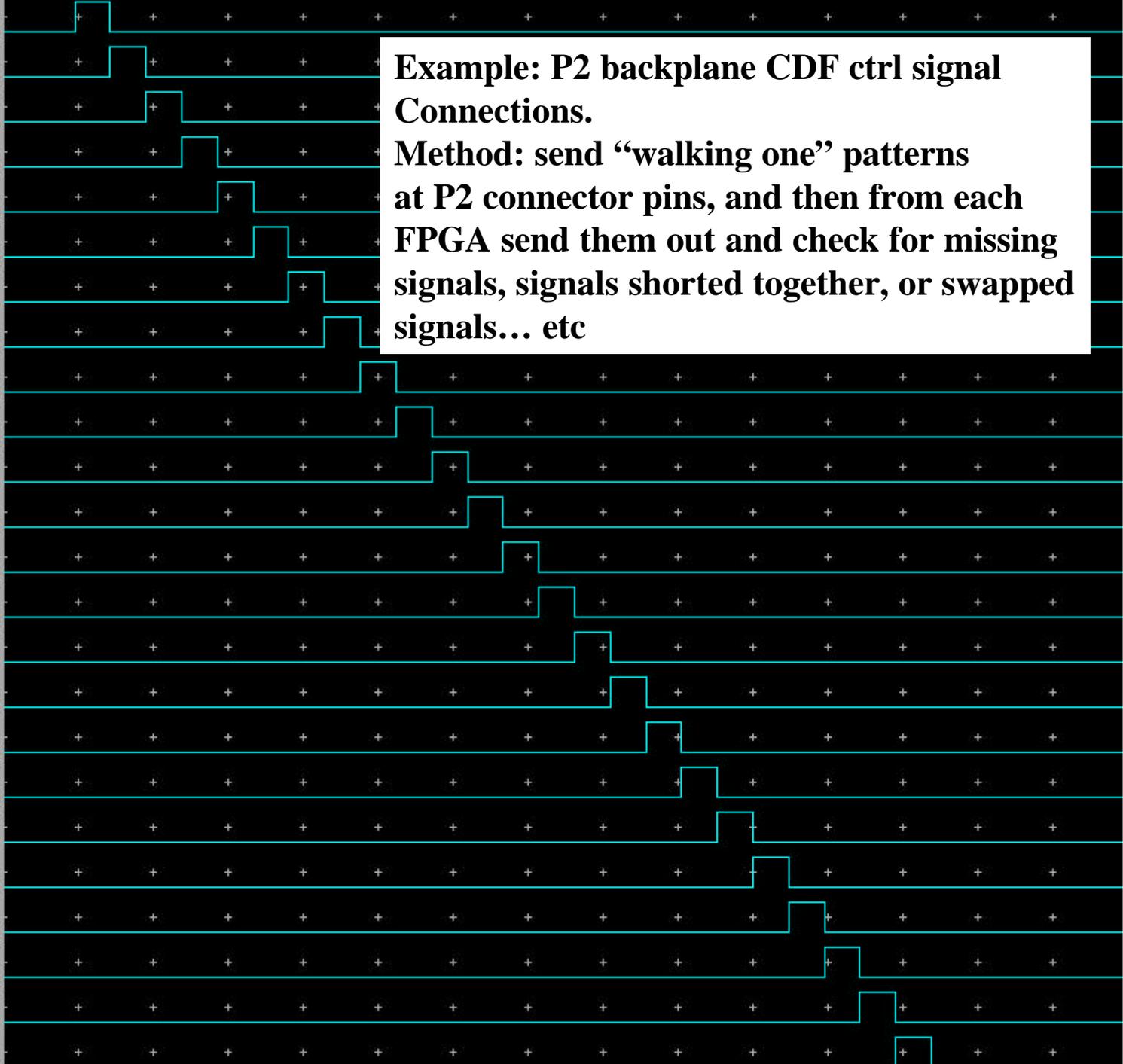
Most simulation work are done by Sakari who just joined us at the end of April. He is a wonderful student and it has been a real pleasure working with him!

(he needs to go back to Finland soon to renew his visa... we need him to come back!).

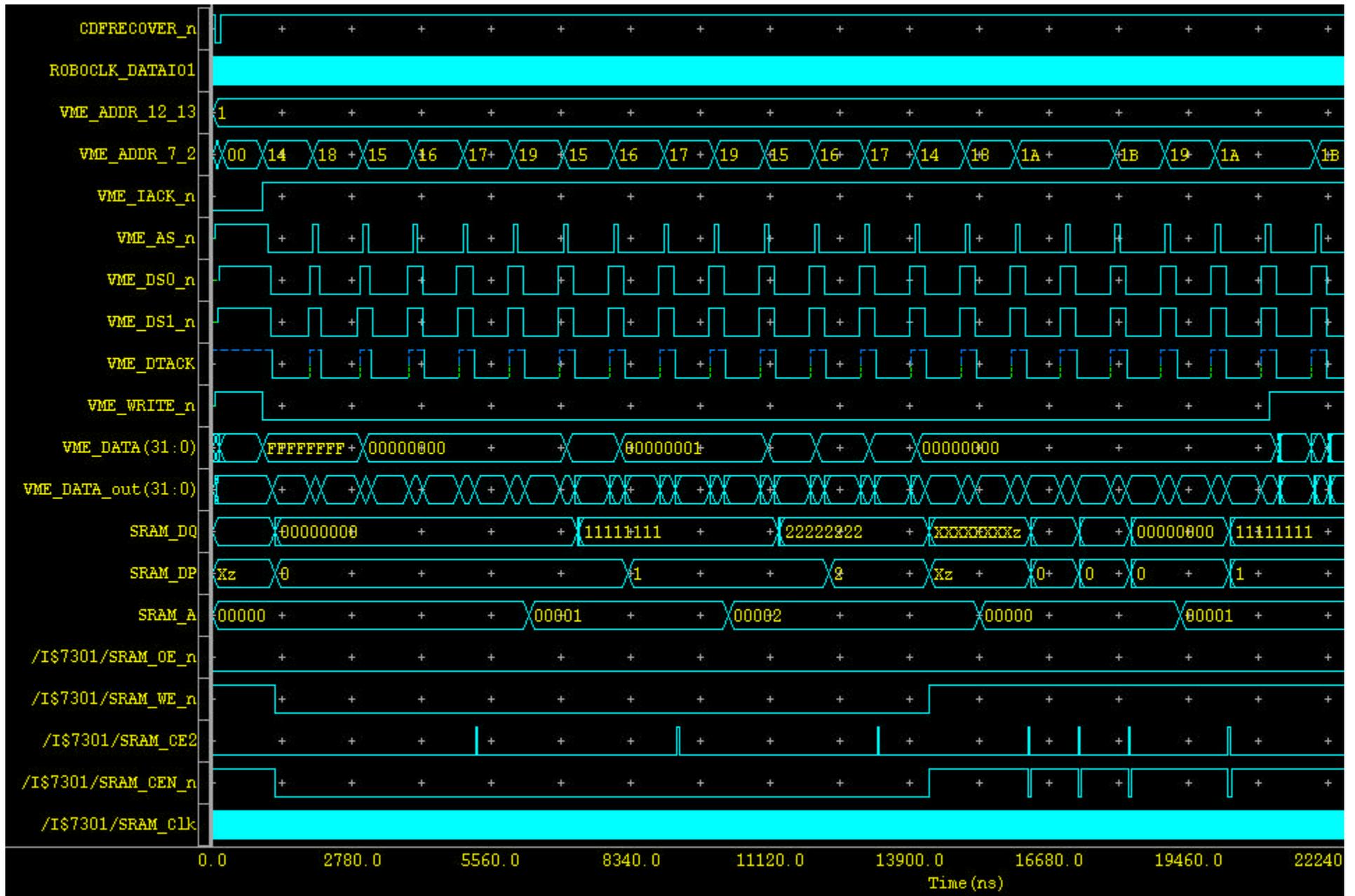
The connections checked by Sakari with board level simulation



\$I1115/P2_CUSTOM/PULSAR_ERROR*
1115/P2_CUSTOM/PULSAR_FREEZE*
15/P2_CUSTOM/PULSAR_LOSTLOCK*
\$I1115/P2_CUSTOM/PULSAR_SPARE*
/I\$1115/P2_CUSTOM/CDF_BC*
/I\$1115/P2_CUSTOM/CDF_B0*
/I\$1115/P2_CUSTOM/CDF_L1A*
/I\$1115/P2_CUSTOM/CDF_L2A*
/I\$1115/P2_CUSTOM/CDF_L1R*
/I\$1115/P2_CUSTOM/CDF_L2R*
/I\$1115/P2_CUSTOM/CDF_L2B0*
/I\$1115/P2_CUSTOM/CDF_L2B1*
/I\$1115/P2_CUSTOM/CDF_L2DB1*
/I\$1115/P2_CUSTOM/CDF_RL0*
/I\$1115/P2_CUSTOM/CDF_RL1*
/I\$1115/P2_CUSTOM/CDF_RL2*
/I\$1115/P2_CUSTOM/CDF_HALT*
I\$1115/P2_CUSTOM/CDF_RECOVER*
/I\$1115/P2_CUSTOM/CDF_ABORT*
/I\$1115/P2_CUSTOM/CDF_CALIB0*
/I\$1115/P2_CUSTOM/CDF_CALIB1*
/I\$1115/P2_CUSTOM/CDF_CALIB2*
/I\$1115/P2_CUSTOM/CDF_CALIB3*
/I\$1115/P2_CUSTOM/CDF_CALIB4*



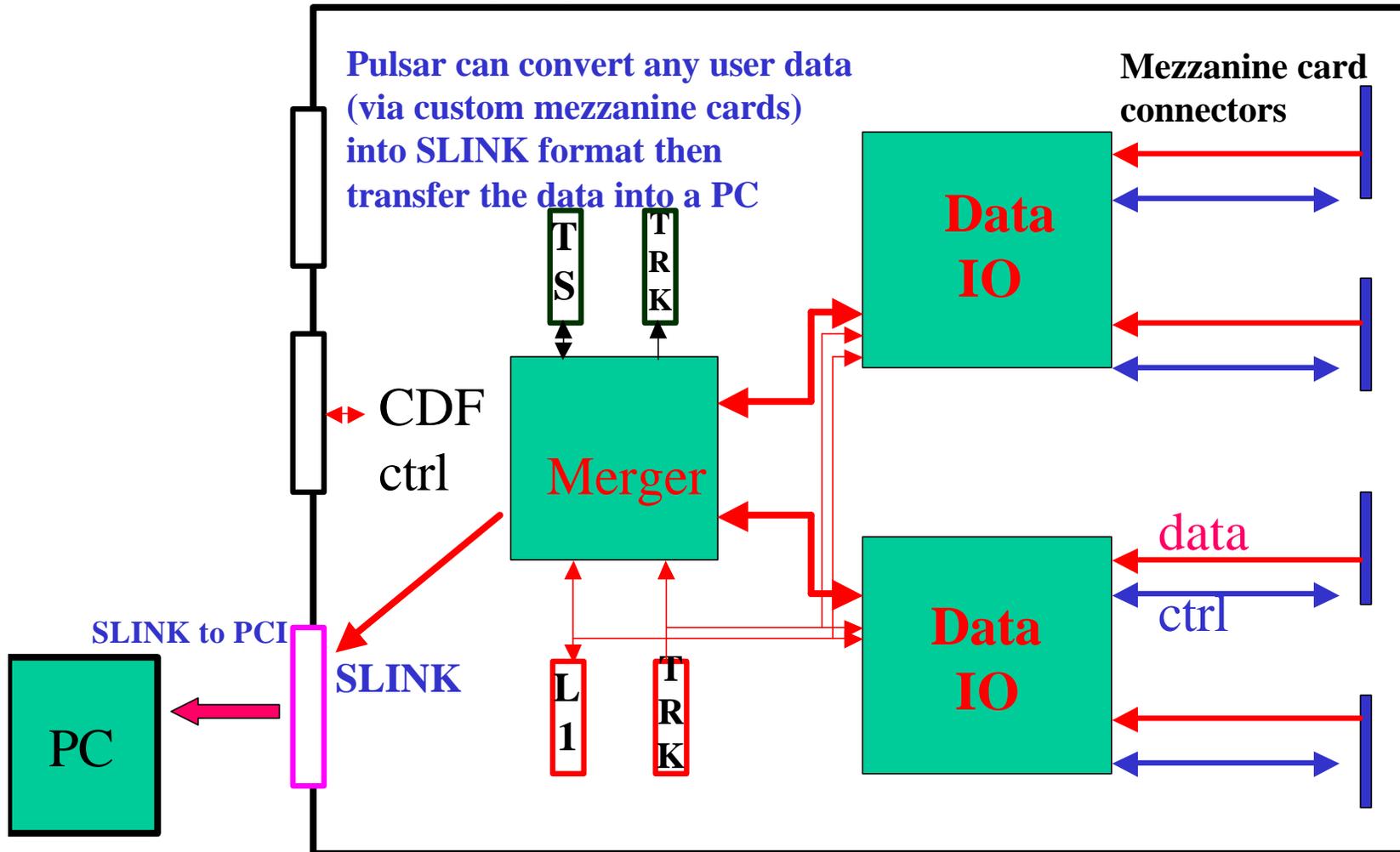
Example: P2 backplane CDF ctrl signal Connections.
Method: send “walking one” patterns at P2 connector pins, and then from each FPGA send them out and check for missing signals, signals shorted together, or swapped signals... etc



VME access to SRAM

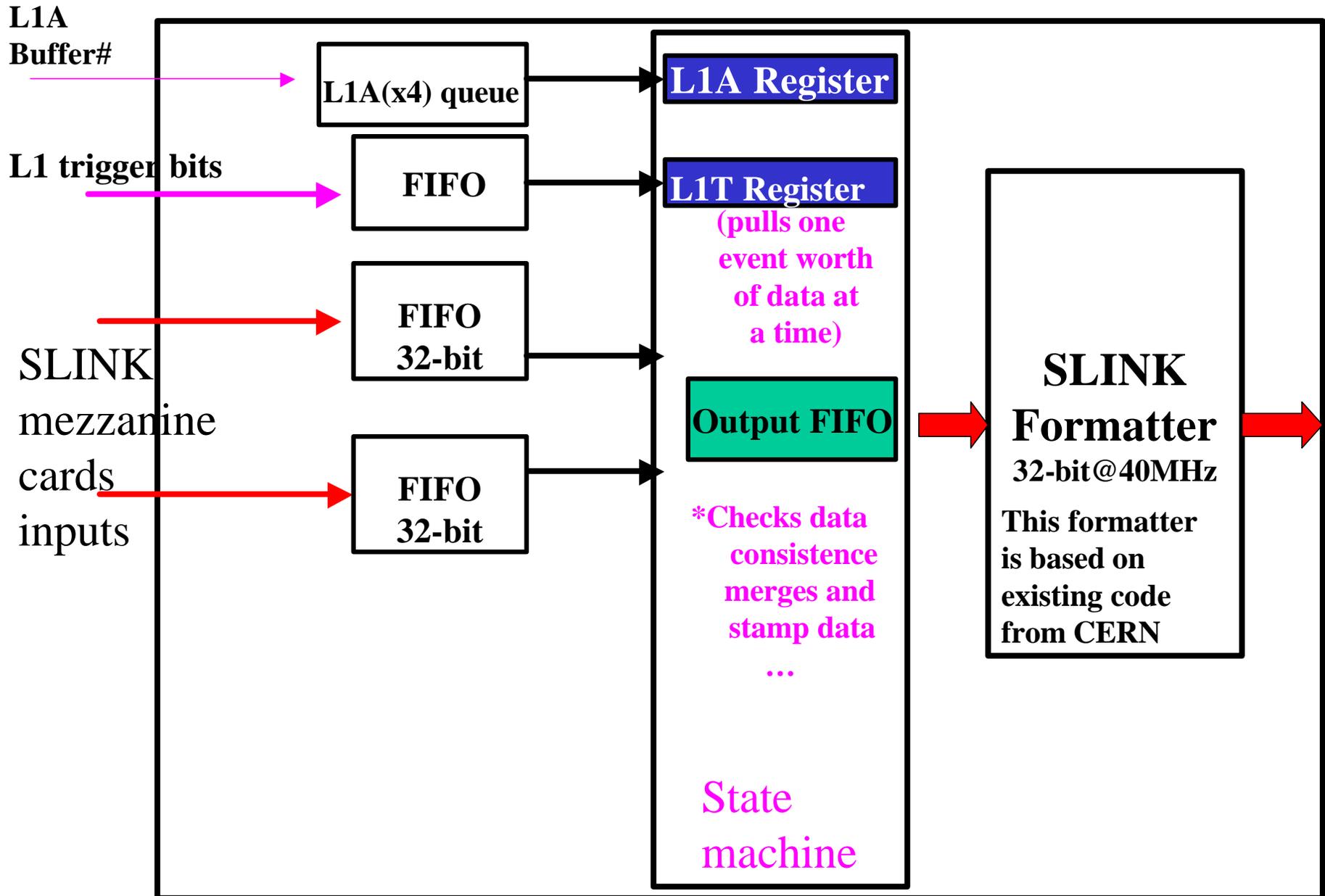
Before we talk about multi-board simulation, recall:

Pulsar in (**general purpose**) recorder mode (directly into a PC)



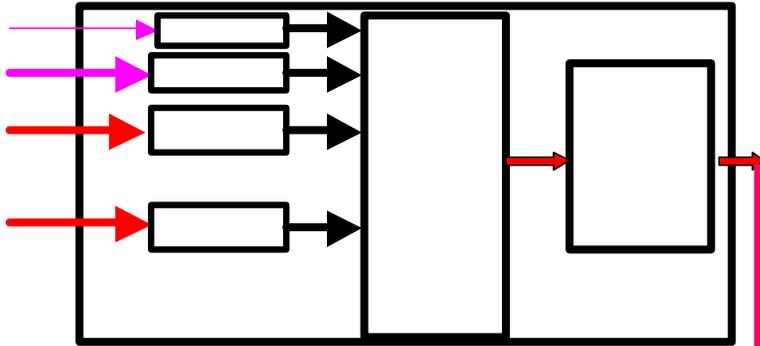
Firmware: this mode exercises the whole board. The core firmware has been written in this mode in Feb and we have been simulating the whole board this way since early April.

A few words on firmware for Pulsar in recorder mode(into a PC):

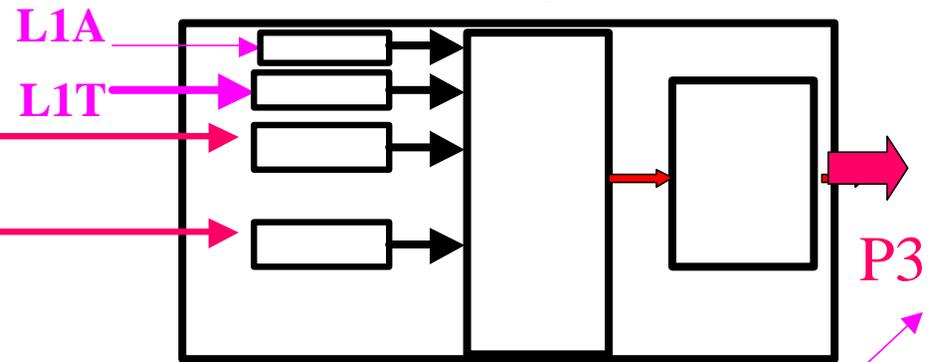


firmware design is similar to all three FPGAs

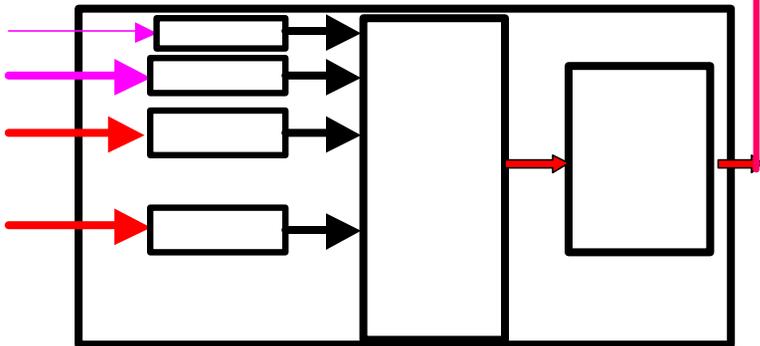
DataIO FPGA



Control/merger FPGA



DataIO FPGA



Data package (per L1A)
in SLINK format sent to PC...

SLINK message format



Trailer:

Data size

Error checking bits

etc ...

Header:

Source ID

L1A buffer #

L1T bits

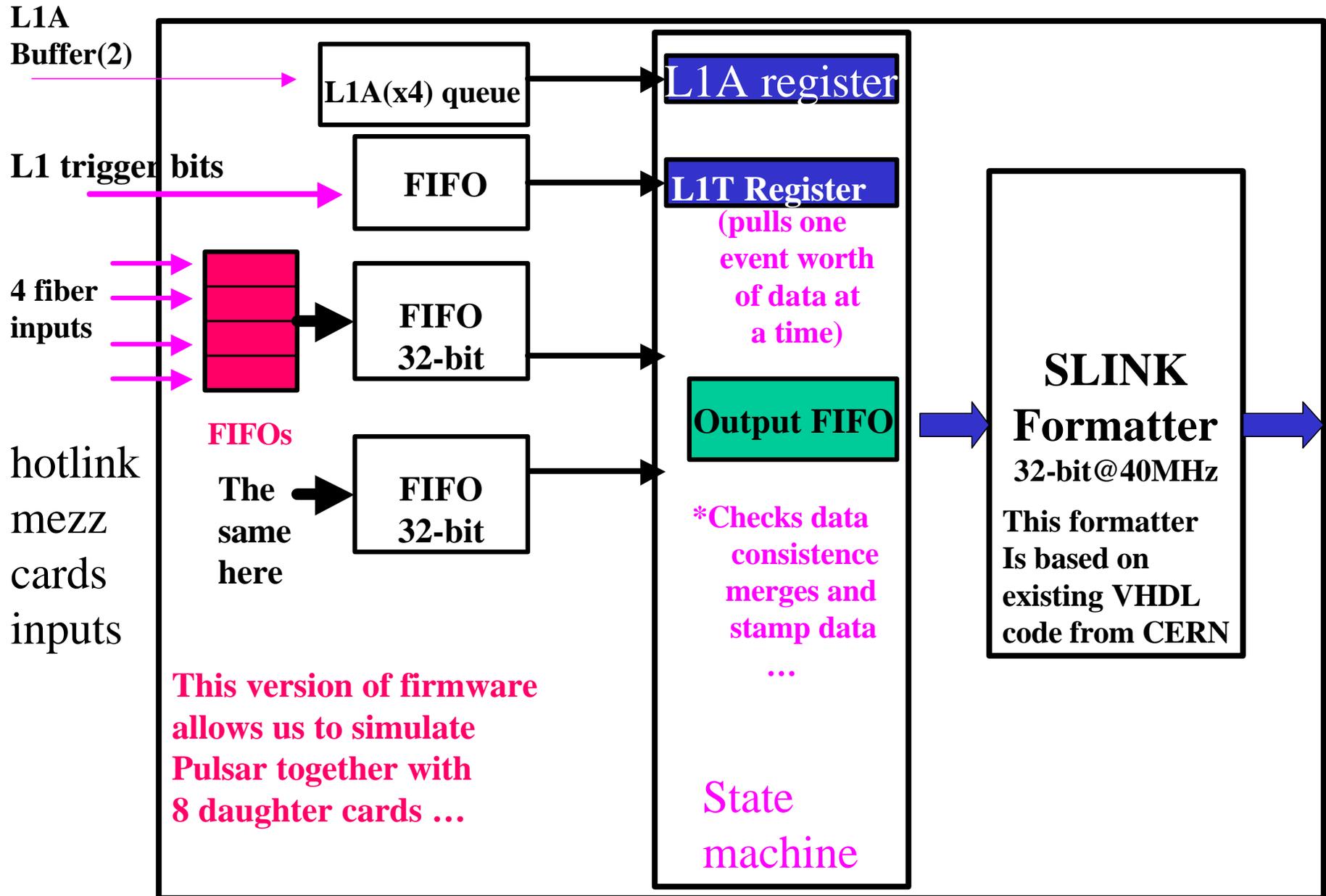
Format version #

header size etc...



First Board Level simulation result in April

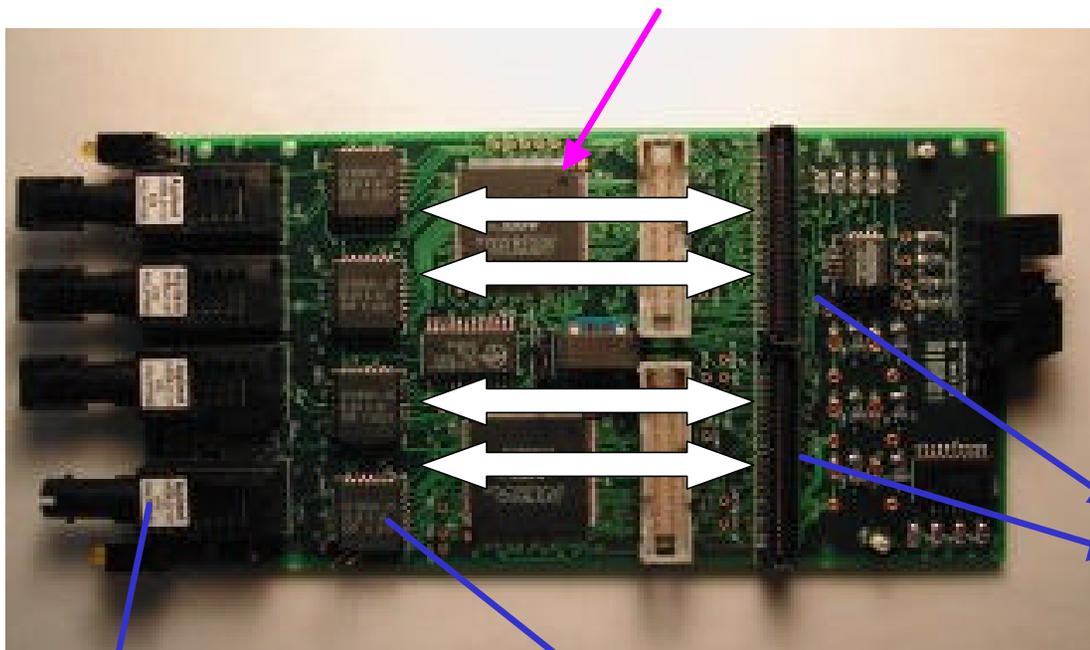
Now we added hotlink mezzanine card inputs (the rest is the same)



Custom Mezzanine cards (**follow CMC standard**)

- Hotlink: Tx and Rx

Altera EP1K30_144 FPGAs are bypassed,
FIFOs are implemented inside motherboard FPGAs for the simulation



hotlink mezzanine
card prototype

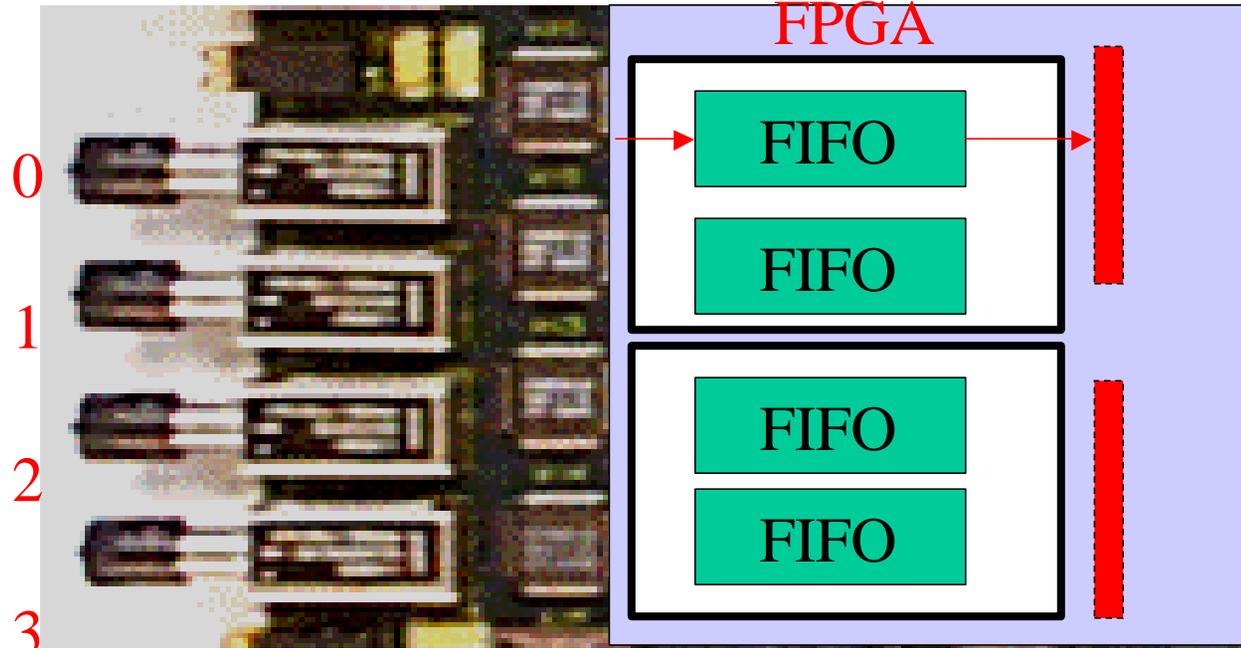
CMC
Connectors (J1 and J3)

Hotlink Optical Tx/Rx: HFBR-1119T/2119T

Hotlink or Taxi Tx/Rx chips

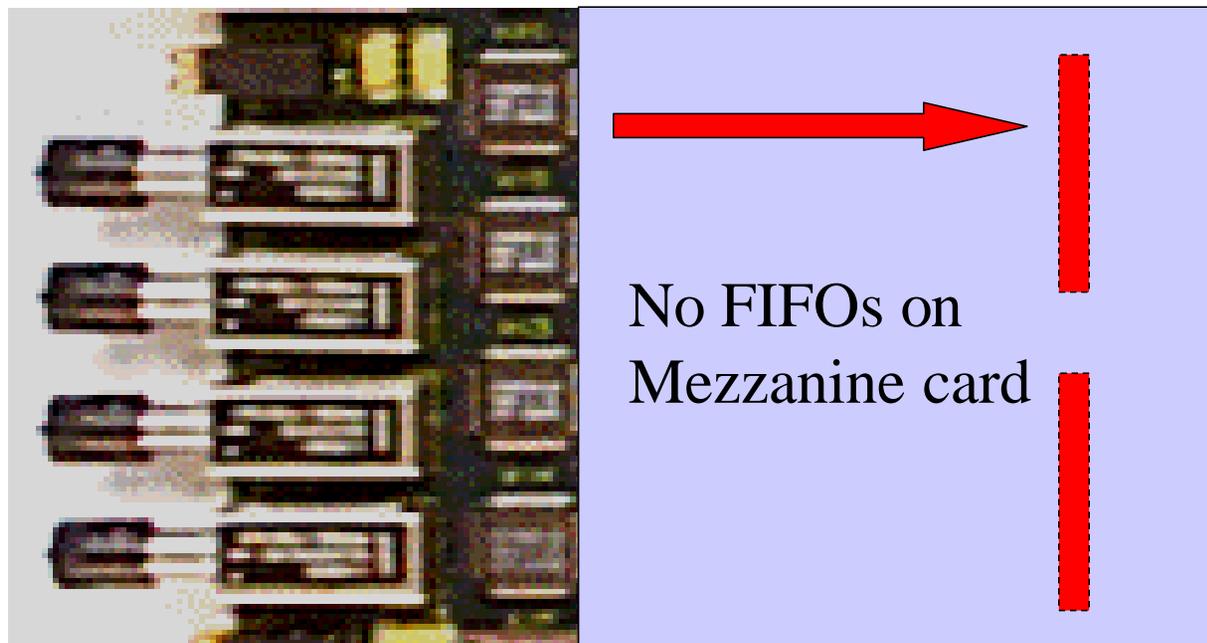
Hotlink Tx/Rx: CY7B923JC/933JC

With&without FPGA



Data is pushed into FIFOs on mezzanine card, then pulled by the motherboard

Receiver case

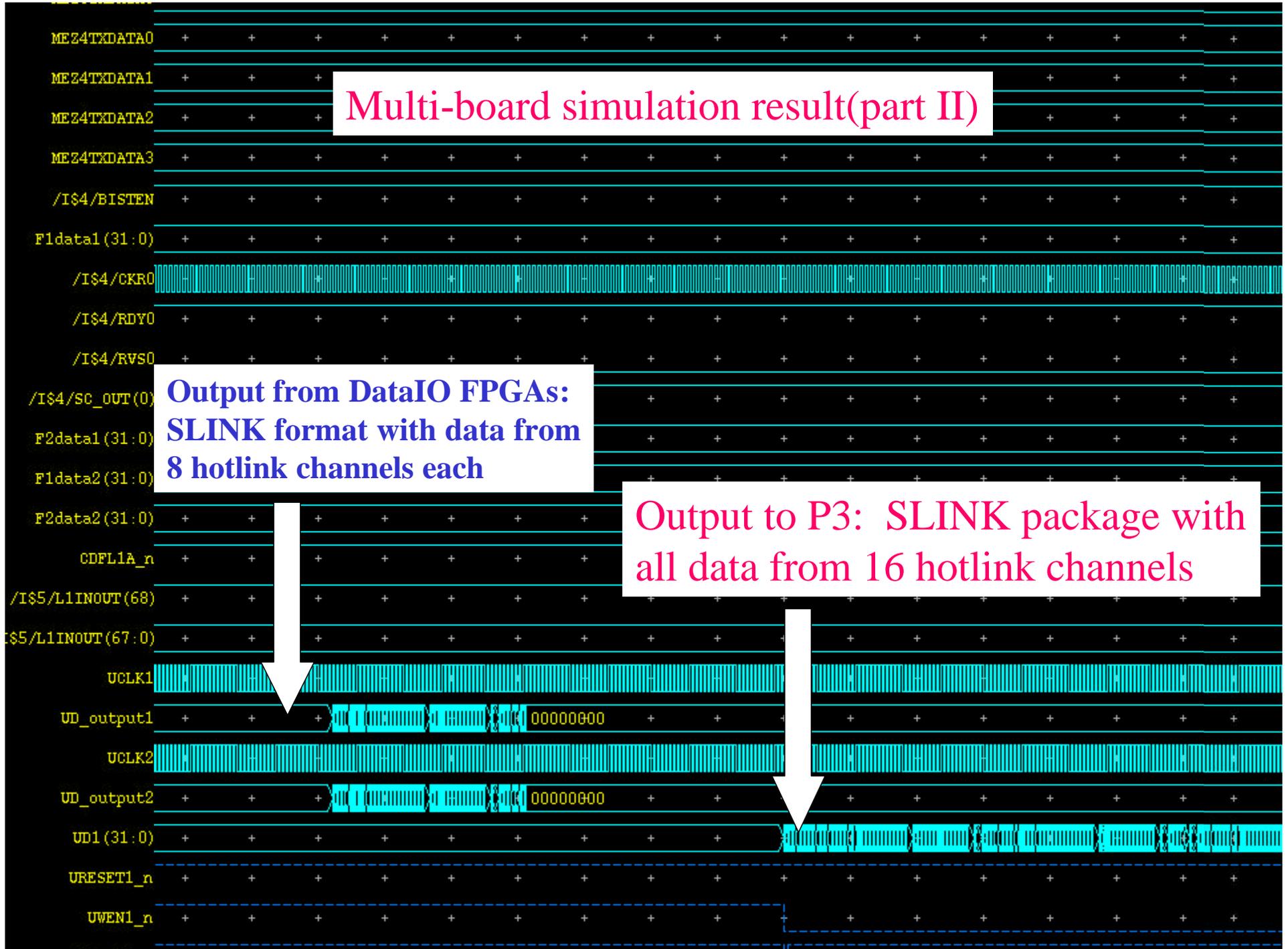


Data is pushed directly into FIFOs inside the FPGA on motherboard

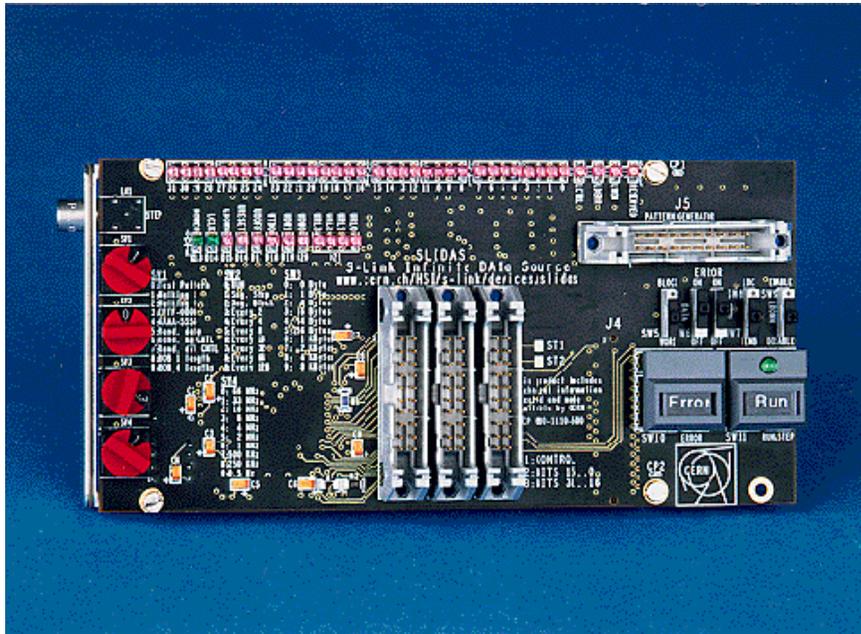
There is really not much difference between the two cases in terms of functionality



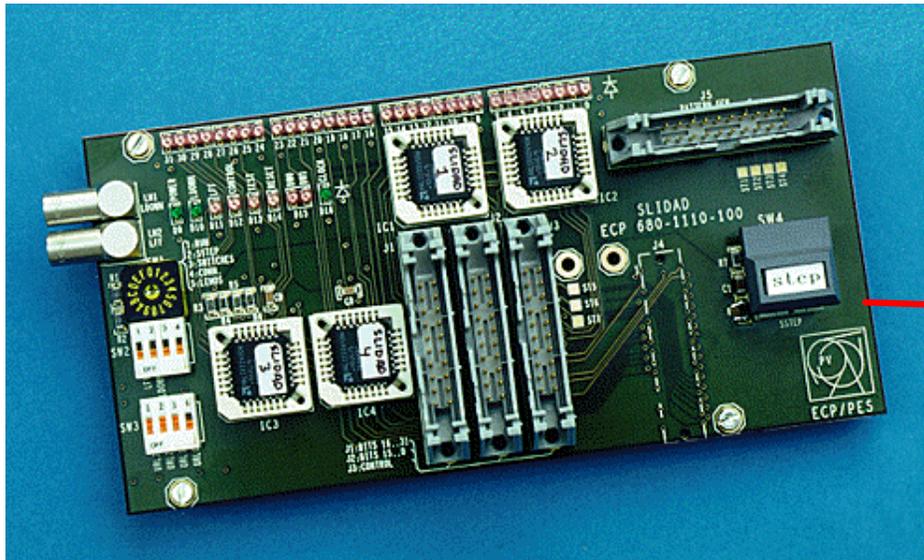
Multi-board simulation result(part II)



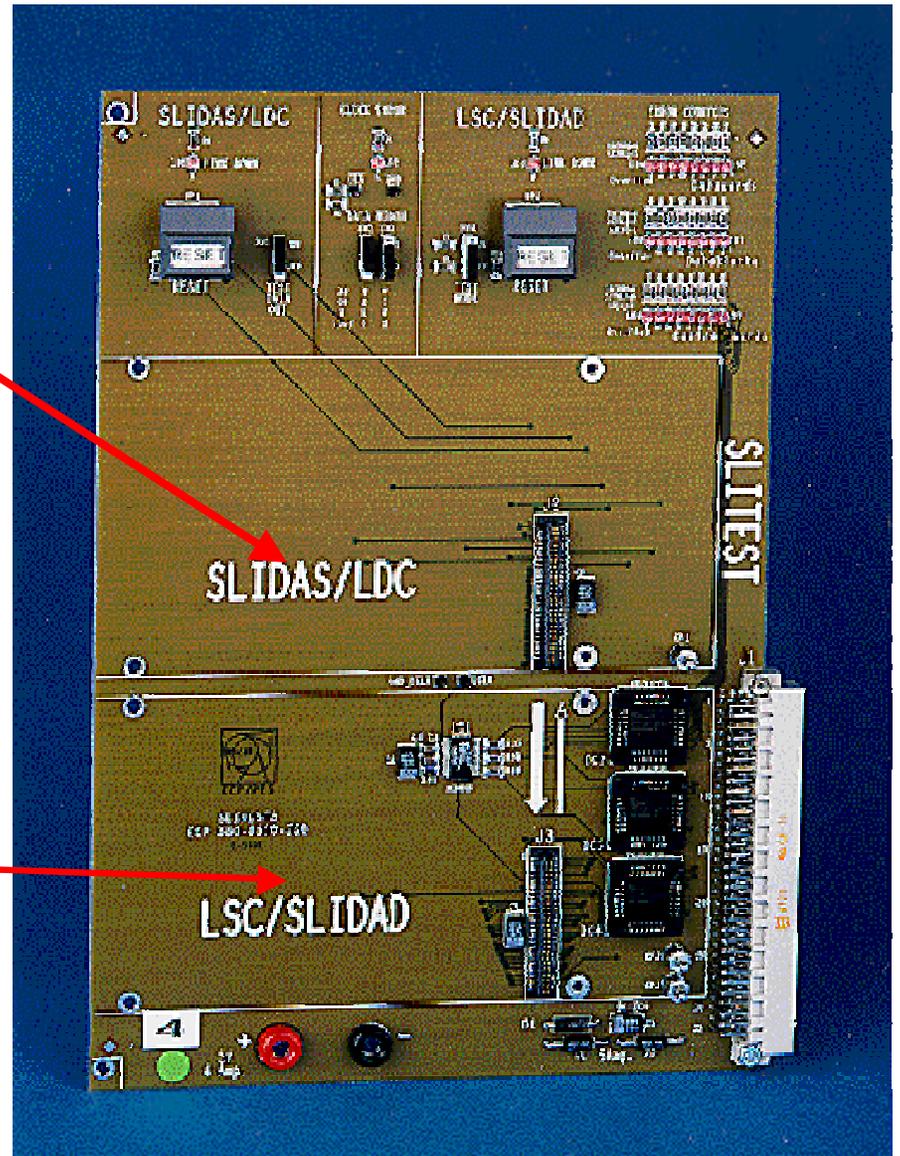
SLINK data source test board



(can be used for initial Pulsar prototype testing)

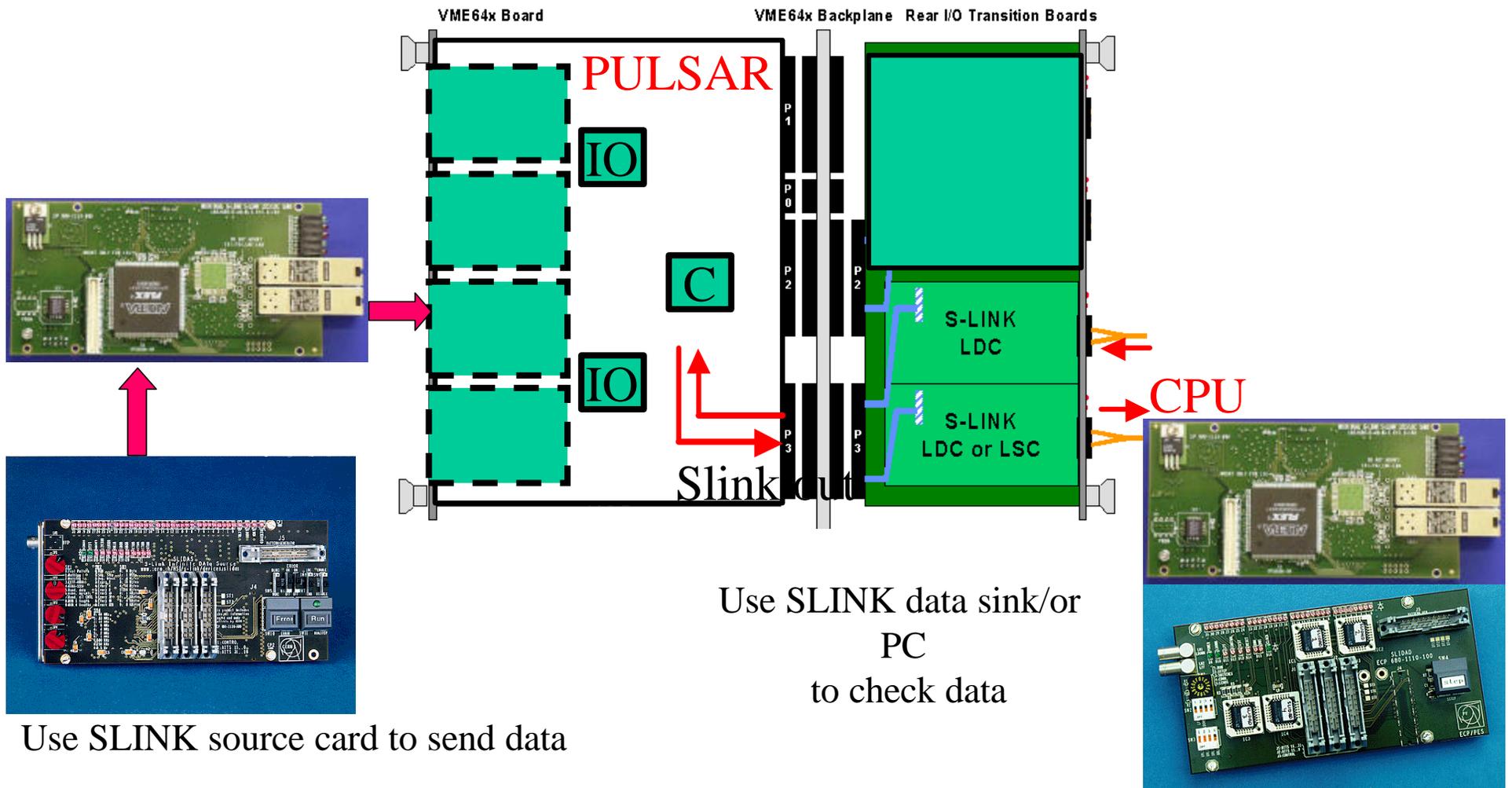


SLINK data Drain test board



Initial test plan for Pulsar board prototype

Pulsar board prototype can be first tested with SLINK test tools, then can be tested with custom mezzanine cards



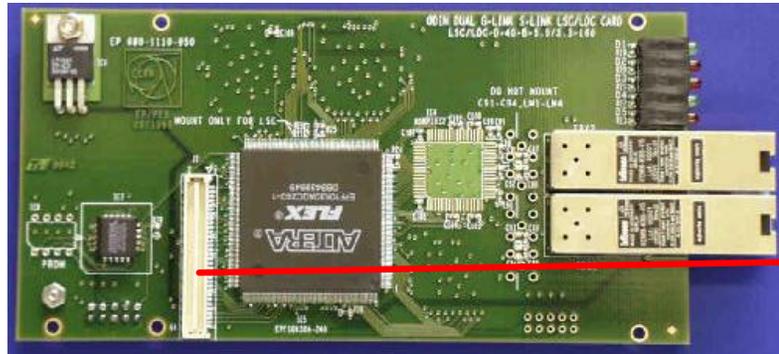
Will need SLINK/PCI software to test Pulsar board and to record data into a PC.

We have another wonderful (summer) student (Derek Kingrey from Cornell) who joined us early this month, and already made lots of progress.

Within the first week, he was able to get the basic code ready for Pulsar prototype testing, Now he is working on more advanced features... he will talk about the details later.

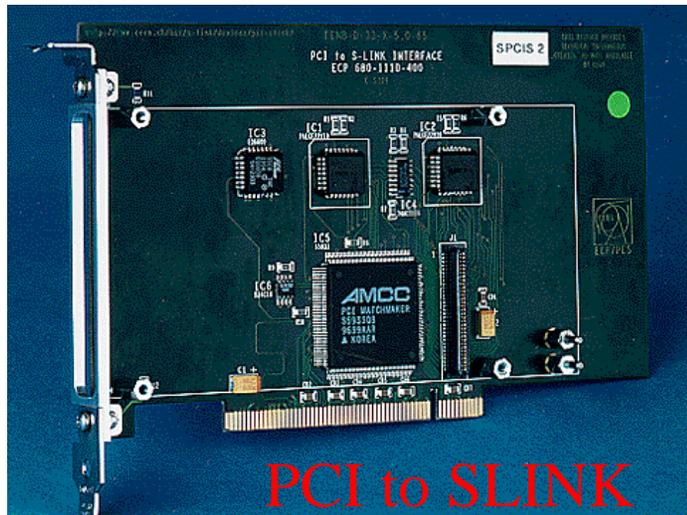
By the way, he is a physics major and will apply for graduate school next year!

We need students like Derek and Sakari in HEP...



CMC(Common Mezzanine Card) Connector (just like PMC).

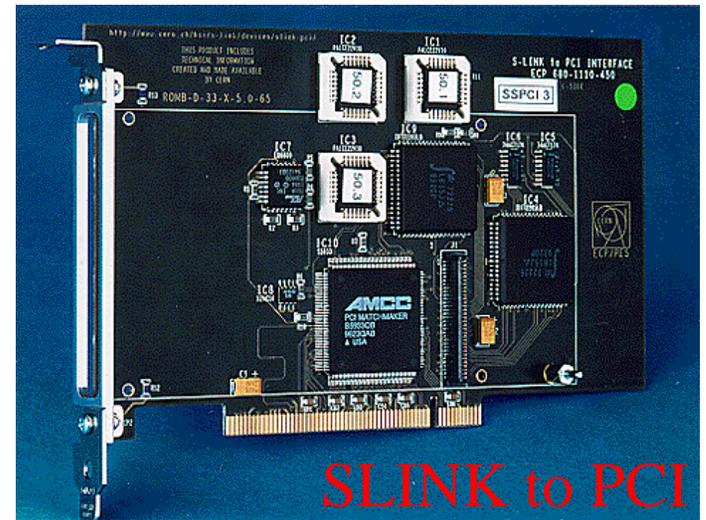
SLINK mezzanine card



PCI to SLINK

New SLINK PCI Cards are much simpler/faster to use, but only a few made so far.

We will use the old ones.



SLINK to PCI

Many device drivers exist (Linux, NT etc), Derek is now developing code based on the software from CFHT telescope project in Hawaii.

Summary

- Pulsar design finalized and optimized
- Initial routing is done, trace analysis will be done within one week or so, and routing can be finalized based on the results.
- Intensive board-level simulation has been done successfully
- SLINK/PCI software for prototype testing ready
- we have been busy and
we have two wonderful students: Sakari and Derek
- would like to request a **special meeting** soon where all trigger experts can look over the design details to make sure the design is right for Pulsar to be used as L2 teststand tool. All design details will be made available (on web) to everyone one week before the meeting.
- after that, will make two Pulsar prototype boards

Back in March, we have planned to have the design ready (to go) by 4th of July, currently we are about two weeks behind that schedule due to the extra time spent on component placement optimization for routing and more board level simulation...