

# Mezzanine cards for the Pulsar board

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## Outline

- What the mezzanine cards are for
- Design overview
- Prototype testing status
- Plans



# Design overview

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- The main components of a mezzanine card are:
  - Two ALTERA EP1K30-144-1 FPGAs
  - Four fiber optics HOTlink or TAXI connectors
    - HOTlink HFBR-1119T/2119T connectors + CYB923/CYB933 chips
    - TAXI HFBR-1414T/2416T connectors + AM7968/AM7969 chips
  - J1 & J3 connectors to the motherboard
  - An on-board oscillator, a programmable clock skew buffer (Cypress Robo Jr. clock) for CDF\_CLK, and a jumper to select between the two

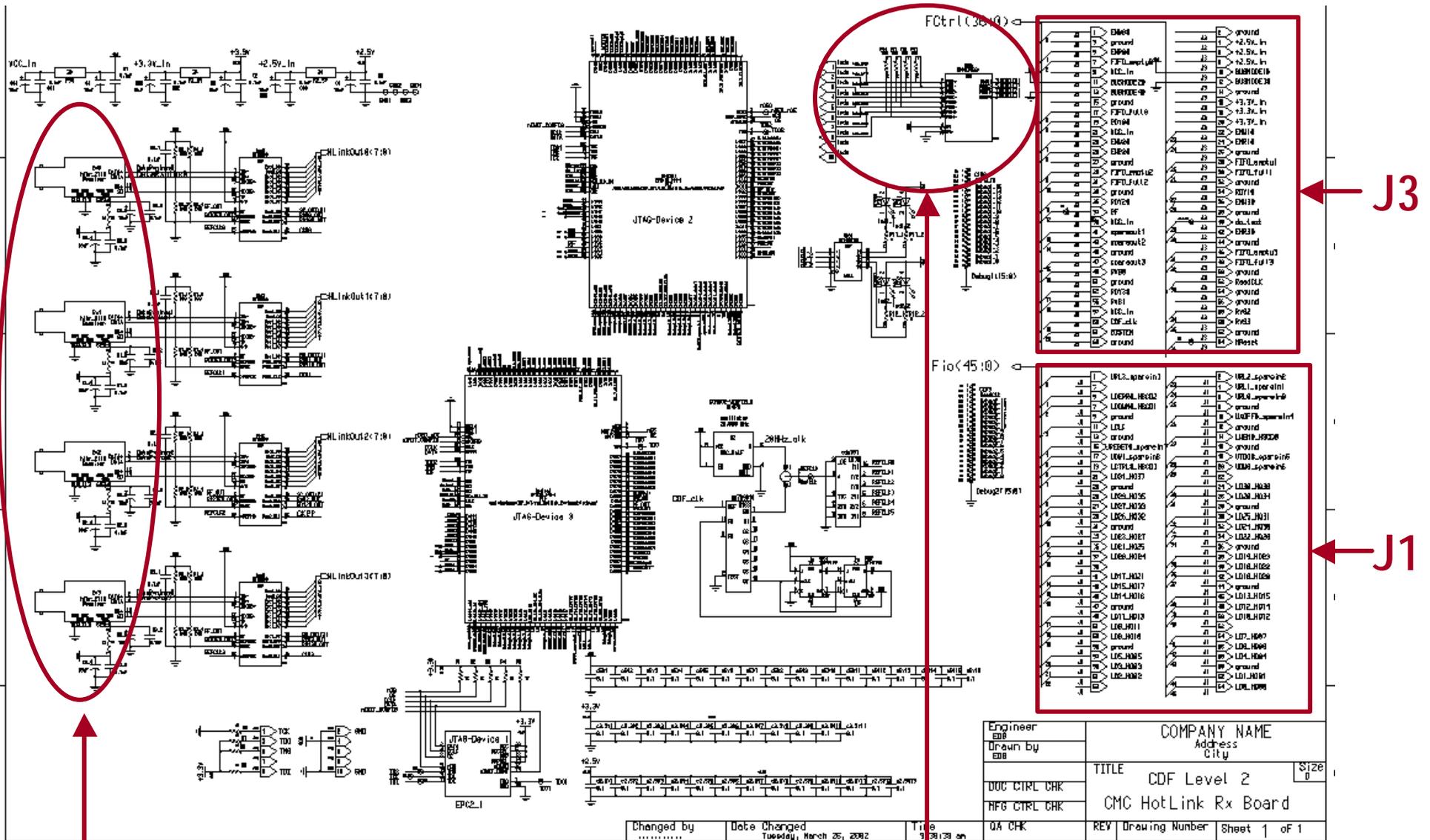
# Subsystem specifics

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- **CLIST:**
  - 6 HOTlink input channels + 1 LVDS
  - 20 MHz on-board oscillator
- **MUONLIST**
  - 16 HOTlink input channels
  - CDF clock x 4 (33 ns)
- **ISOLIST**
  - 7 TAXI input lines
  - 12 MHz on-board oscillator
- **RECES**
  - 12 TAXI inputs
  - CDF clock



# HOTlink receiver schematics



HOTlink optical rx

LVDS Rx (for CLIST)

Engineer eeb	COMPANY NAME	
Drawn by eeb	Address	
	City	
DOC CTRL CHK	TITLE	Size
NFG CTRL CHK	CMC HotLink Rx Board	
QA CHK	REV	Sheet 1 of 1
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	Tuesday, March 25, 2002	9:28:13 am

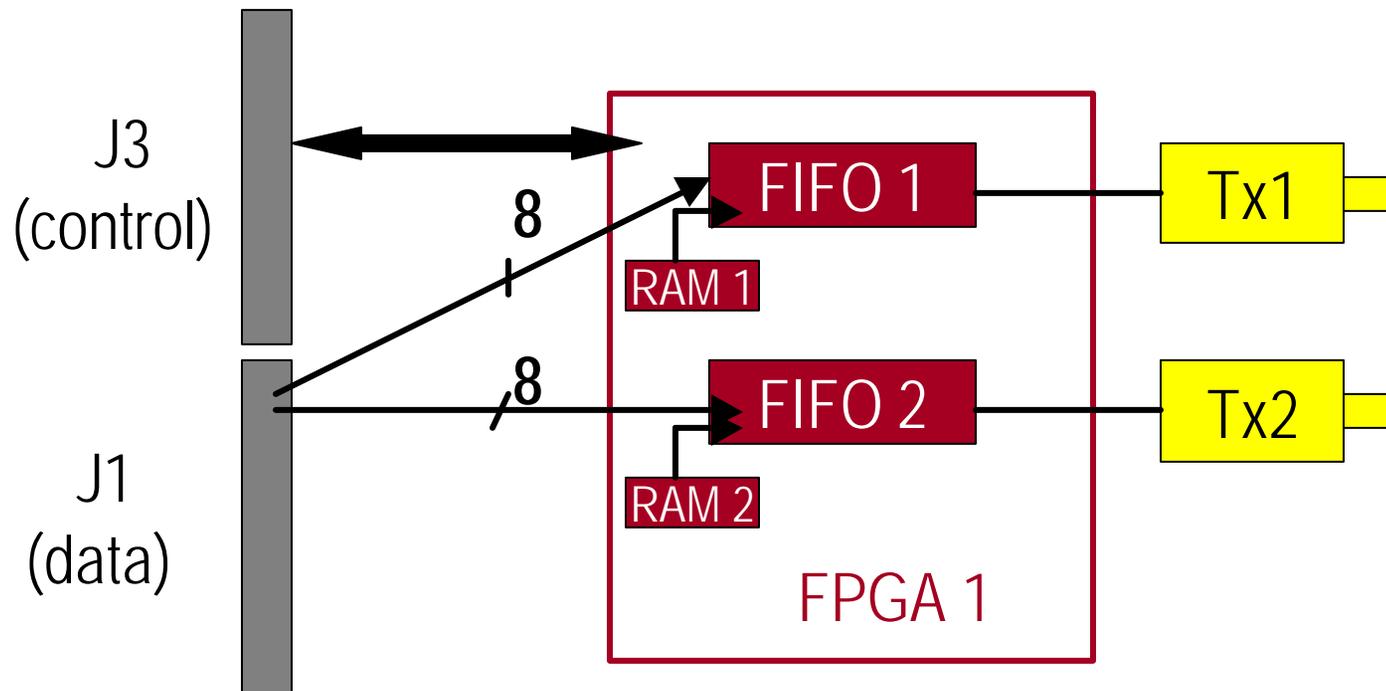
# Modes of operation

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- There are two main modes that a mezzanine card can operate in
  - Normal data transmission, where data emulating the real system are driven from the motherboard
  - Test mode, designed to test the mezzanine cards themselves before the motherboard becomes available
    - Note that for HOTlinks there is a special built-in test mode feature
    - The reason we need both a Tx and a Rx is so that this testing is possible.
      - In the future, we can also use the Rx to record the data for subsequent playback in the transmitter.

# Firmware implementation

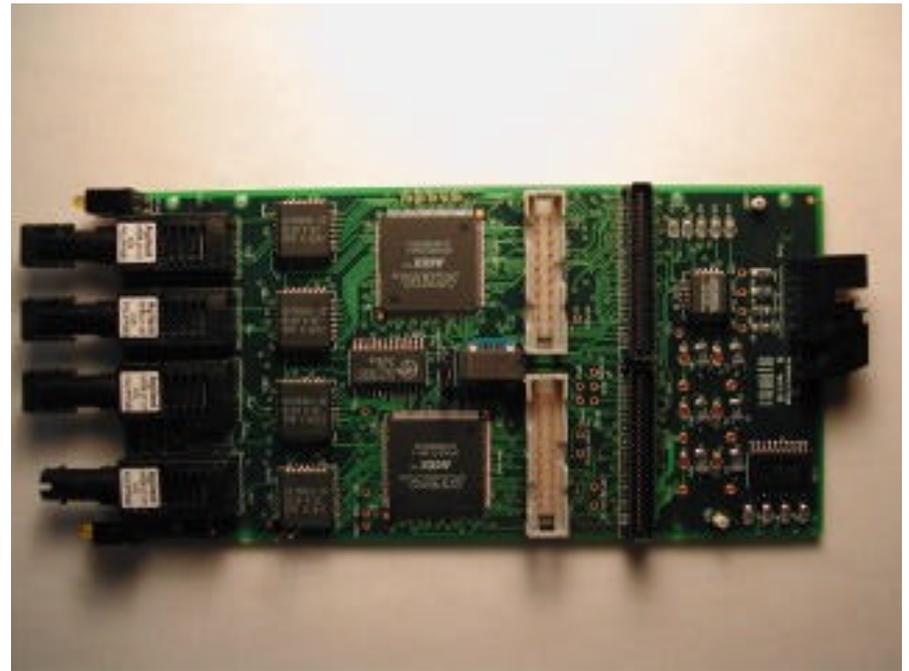
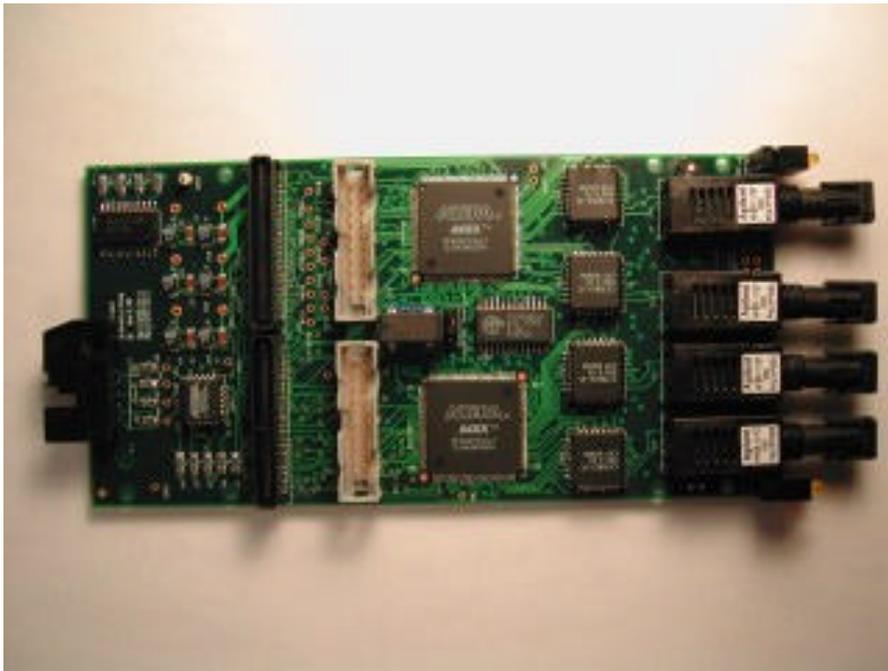
- In normal mode, data and control signals are received from the motherboard through J1 & J3
- For each channel, the 8-bit data are stored in the corresponding FIFO inside the FPGA, and then passed on through HOTlink, TAXI, or LVDS connectors to the receiver
  - In the test mode, the test pattern can be driven through internal RAMs



# Prototype board testing

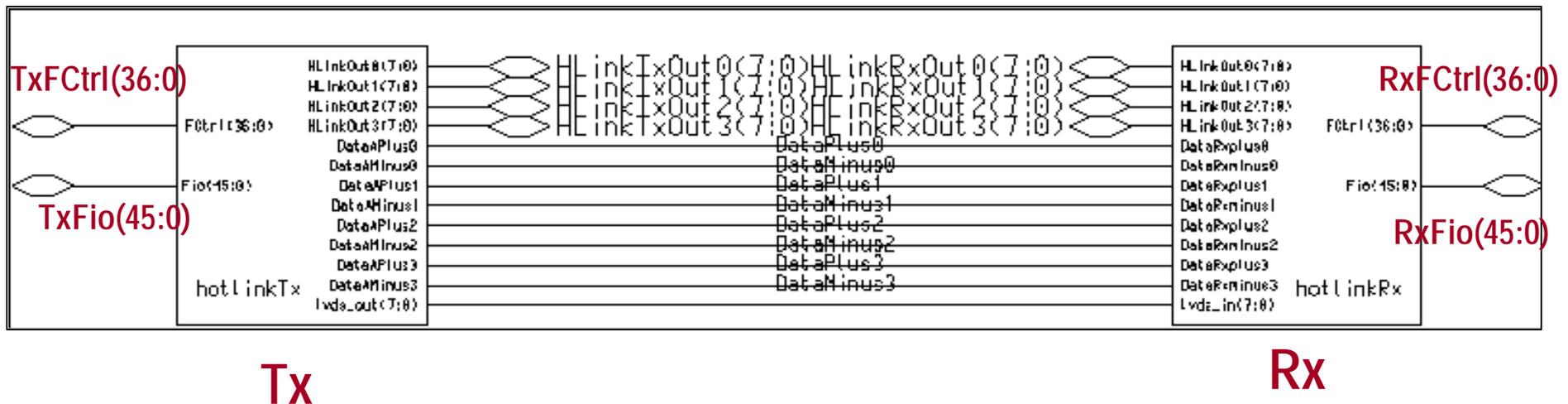
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Currently, have one pair of HOTlink Tx/Rx mezzanine cards that is being tested at U. Chicago (NK, Peter Wittich)



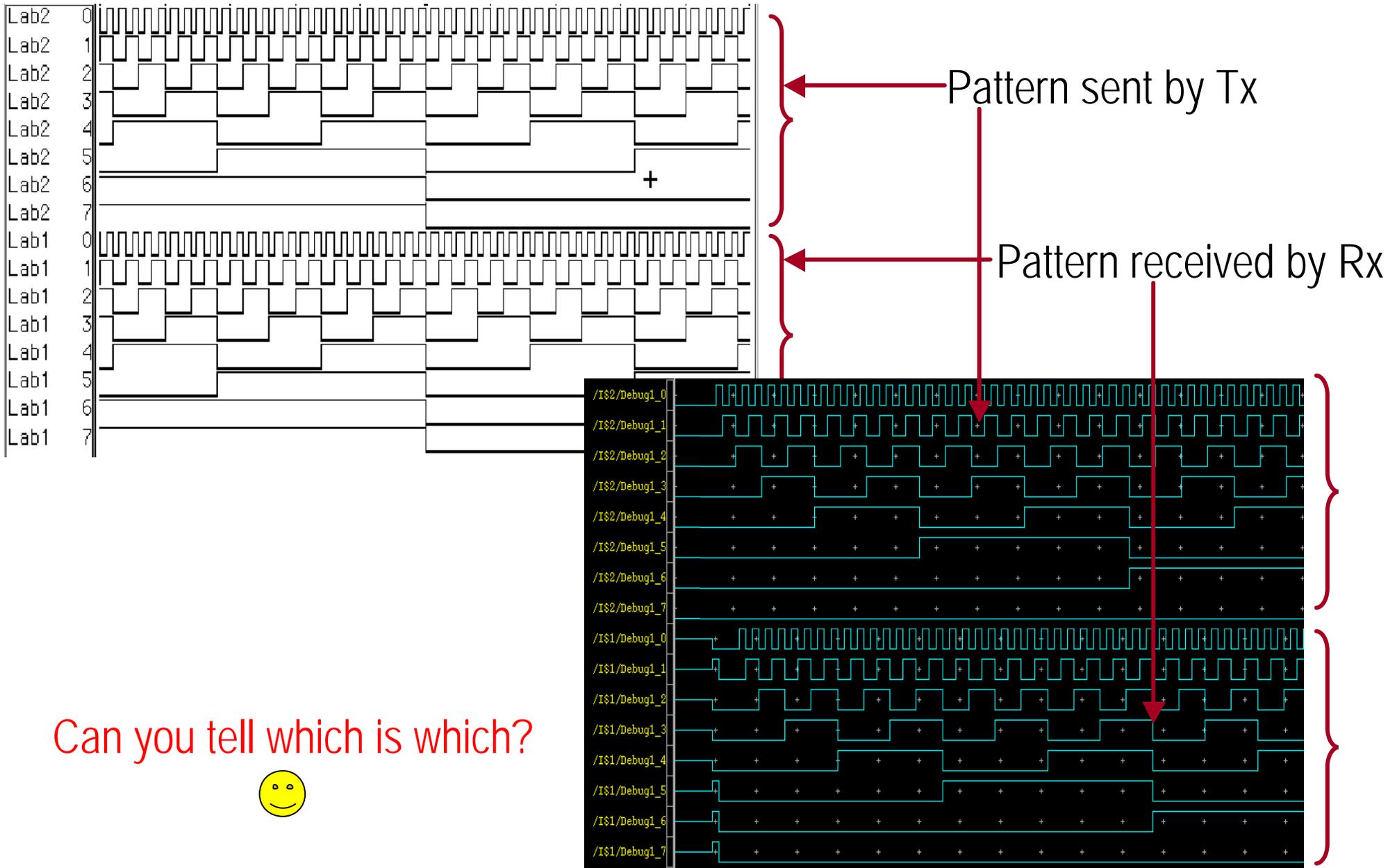
# Simulation

- Before the prototypes were built, the boards were simulated extensively using Mentor Graphics QuickSim II real-time simulation
- The Tx and Rx were simulated individually, and the joint Tx/Rx system was simulated using the following simple trick



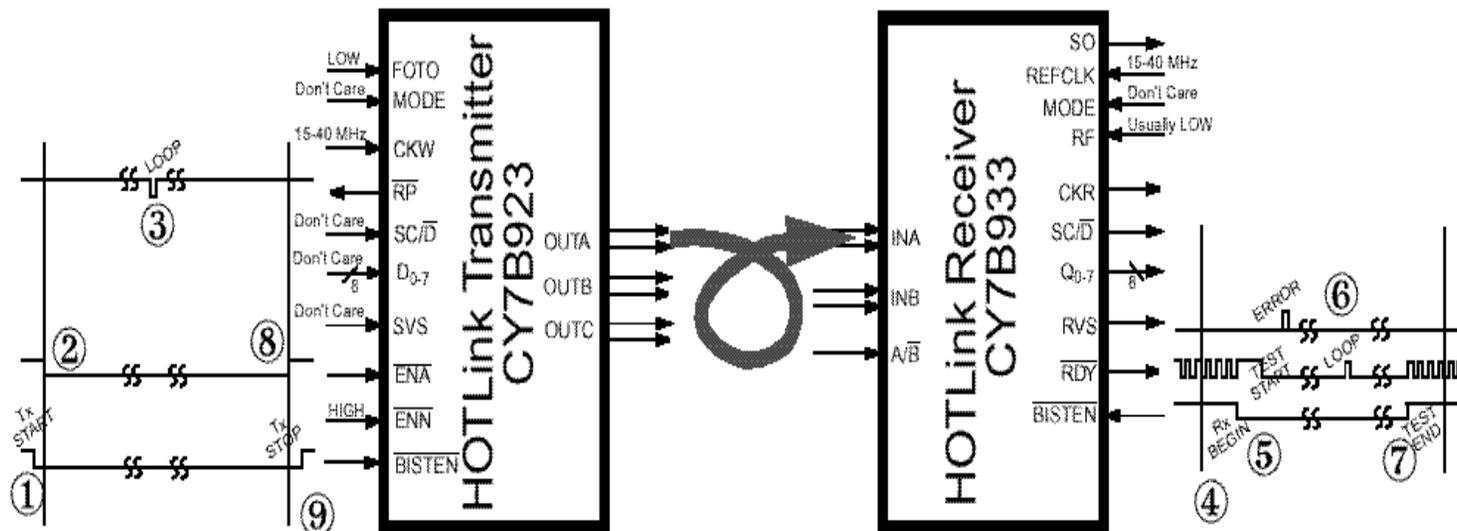
Because things worked in simulation, we were more confident that the design was functional -- and indeed, there were few surprises during testing

# Simulation vs. real system test



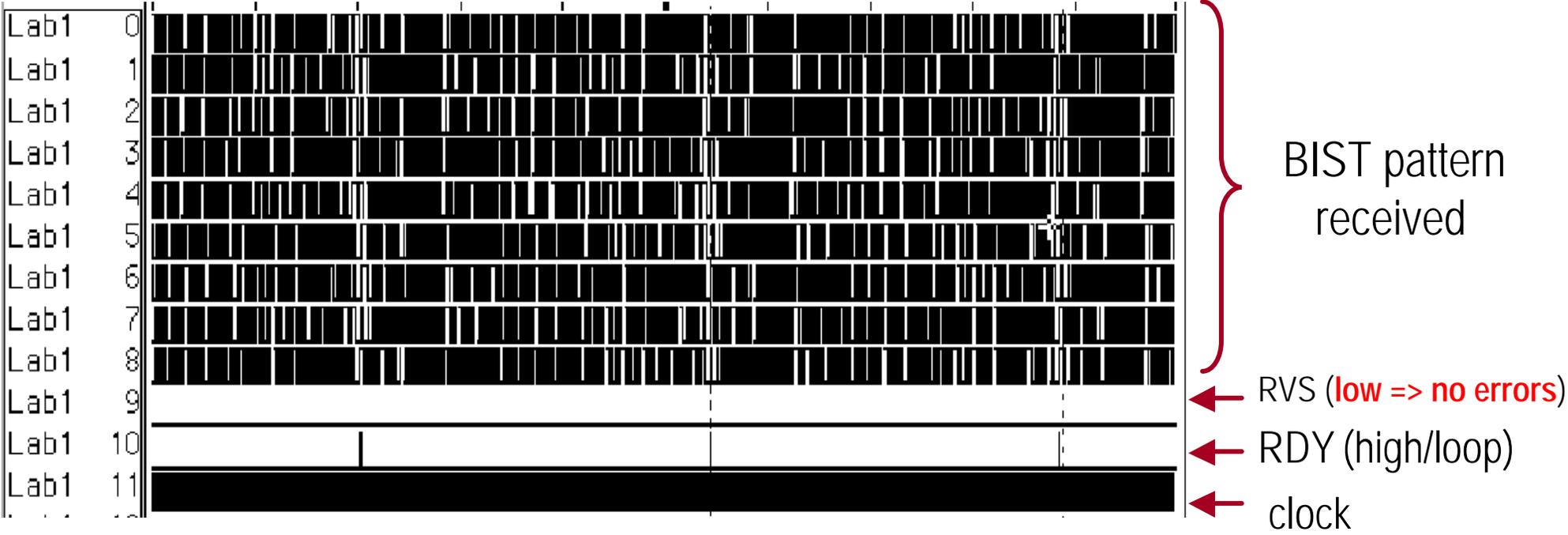
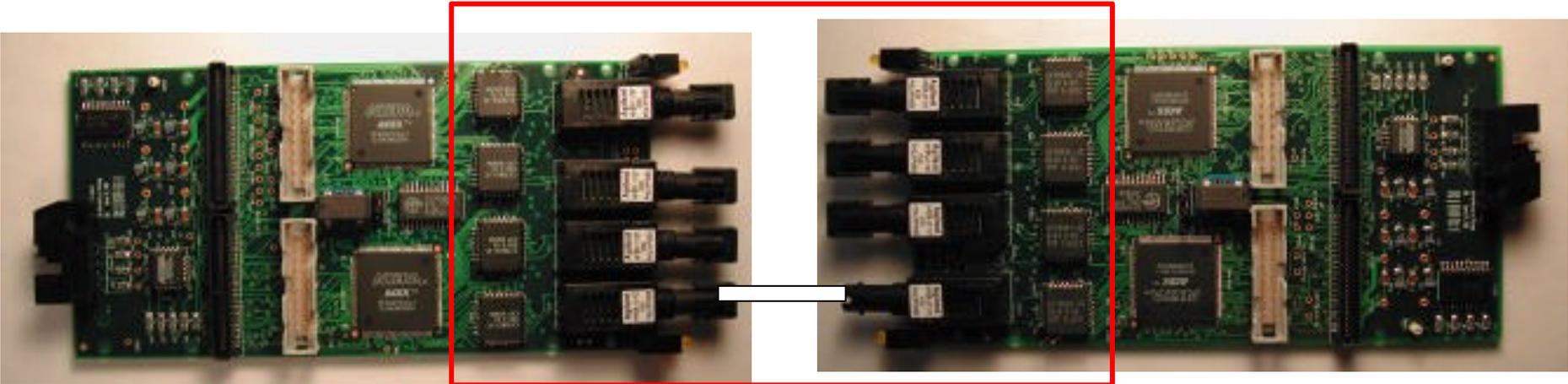
# BIST mode

- **BIST = Built-In Self Test**, a feature that enables the HOTlink user to perform an unambiguous, real-time test of the entire link.
  - There's no need to add or remove any components from an operational system!



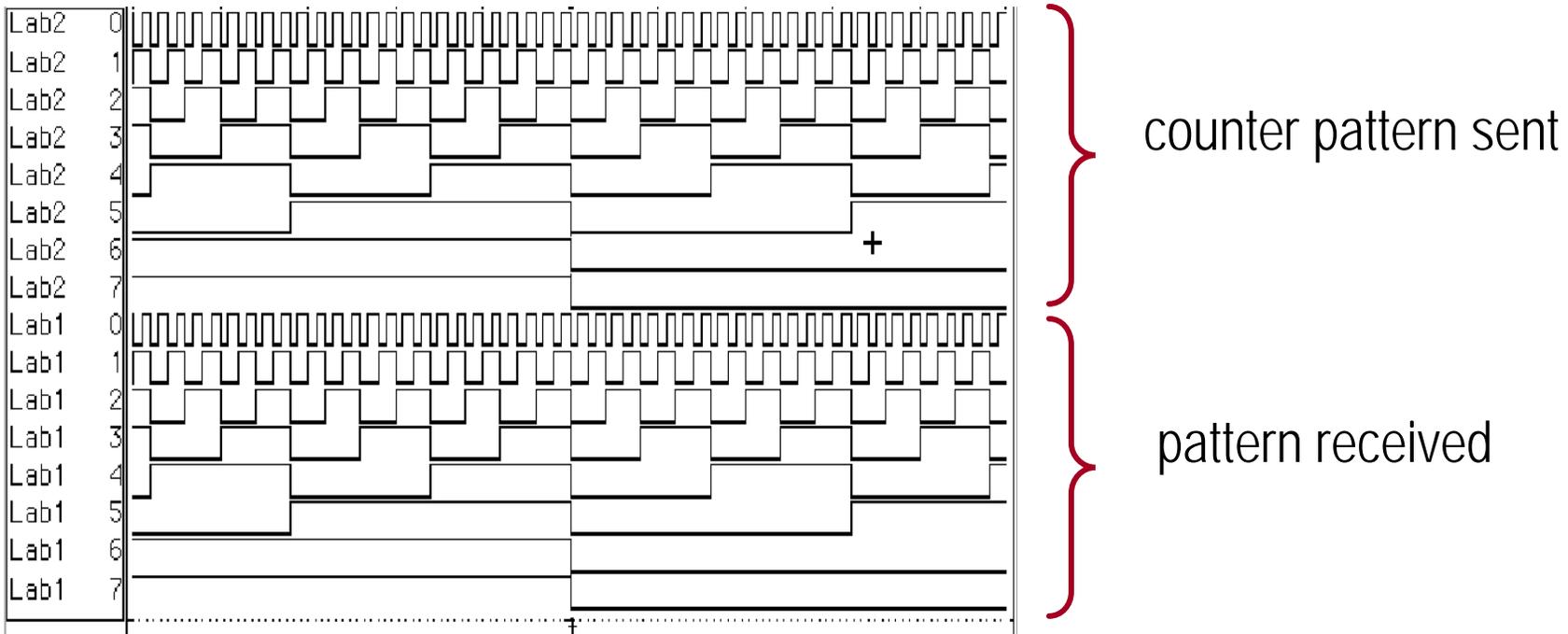
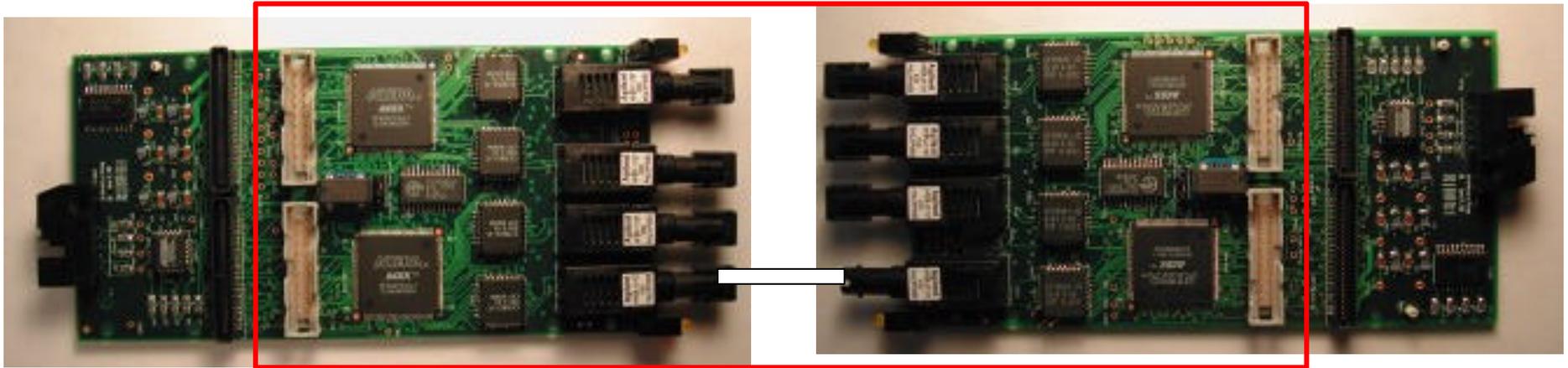
- When BISTEN\* and one of the enables (ENA\* or ENN\*) are enabled, HOTlink Tx creates a continuous 511 character pattern, which HOTlink Rx then checks character-by-character.
  - If any errors are found, they are flagged by the RVS (Received Violation Signal) output.

# BIST mode testing



All four channels work fine in this mode

# Driving patterns through FPGAs



**All four channels work fine in this mode**

# Conclusions and future plans

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- Mezzanine cards provide an interface from the Pulsar board to the L2 systems under test
- At the moment, have a HOTlink Tx/Rx prototype pair under test at UC
  - The testing is going very well -- no major problems seen so far
  - Still need to test the LVDS case
- After the testing is completed, plan on producing 11 (+ 6 spares) HOTlink Tx/Rx pairs, and start working on the TAXI case
  - Expect the TAXI case to go fast

**Feedback is always welcome!**