



Alpha Firmware Tests

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Trigger Hardware Meeting



PIO Firmware

- Firmware for reading Reces
- New vhdl design from Rick Kwarciany.
- Successfully tested reading Reces
- Alpha arbitrates with interface boards – Can read Reces at any time. (reduce tail for Reces triggers)
- Takes 500ns of MBus time for reading
- Uses 64 bit burst transfers on PCI bus => only 13us to read all Reces data on a L2A
- Did test reading a single Reces channel for every event during processing
 - For $iphi = 0$, would hang the alpha and MBus every few minutes (at high rate)
 - For $iphi=20$ never saw any problem
 - Will get timeout added to design to add robustness to system
- 64 bit transfers requires new code



Pipeline Fpga

- Control of MBus loading now in firmware
- Reduces number of PCI reads/writes required by software
- Allows startload to be sent whenever L1A arrives
 - Better pipelining performance
 - Versus waiting to get to that point in code loop
- Backend of L2-TS handshake put in firmware. Saves about 2us
- Tests were done without any errors.
- Requires new code to use fpga



DMA Configuration

- Put Optimization into Code instead of fpga
- Use PCI burst transfer to write all 6 DMA buffers
 - Versus 6 separate PCI writes
- Saves about 1 us of overhead time for each event



Full Optimization Test

Use new PIO, Pipeline fpga, DMA config code optimization

- Plus removed DMA config reading, L1 scaler calculation, Timing calculation
- Had Interface boards just sending EOE word. Only trigger crates in partition.
- L1 BC trigger PS of 12 gave L1A rate of 143KHz!!!, L2A rate of 5Hz
- L2 ran with only 1% deadtime!

• Times

- 4 us for MBus loading (pipelined with processing)
- 6 us between data being loaded and alpha ready to check for next event
 - 1.1us Configuration time. Read fpga fifo, configure DMA, enable fpga for next startload
 - 2.6 us Processing: Unpacking, Autoaccept algorithms, error checking
 - 2.3us for L2-TS handshake
 - Times measured using Logic Analyzer

• Remember: < 1 year ago, this max rate was 20KHz.



VME Block Transfers

- Can enable 64 bit PCI burst transfers for VME readout of TL2D
- This causes problems for alpha since PCI bus is heavily used during readout
 - Get errors sending last data and reading DMA buffers
- Option 1 Use readoutlist to reduce average TL2D size
 - L1 scalers- 64 words
 - Reces - 48 words
 - Diagnostic - 50 words
 - L2 trigger word - $N_{\text{words}} = N_{\text{triggers}}$
 - L2 scalers - $N_{\text{triggers}} * 4$
 - Total is 2,248 bytes per event
- Option 2. Put delays in readout code to separate bursts into smaller units
- Option 3. May be able to fix problem running a wire from data fifo ef* pin to fpga, but not certain
- Option 4. Ideally would do all/most of the above anyways.



Plan

- Need to put new code in CVS
- Make official table exe
- Do more Reces tests to better understand problem
- Test without beam
- Test with beam at end of store
- Improvements of not reading DMA buffers should come after new firmware has been running for awhile.
- Improvements for VME readout are separate path
- Once improvements are in place, inform MCR they can up the Luminosity.