Week of 1/something to 1/31

- New 9U status
  Found cause of VME problems w/ new board at FNAL
  → Floating reset line (pins reversed in FPGA constraint file)
  Fixed at Michigan with change in code
  Can use 32 bits of VME address, 1 stuck data bit
  Still need to test with GUI, probably 1/31? at Michigan

- Misc, plans
  Have 2nd board working at Michigan (parallel MB testing)
  Found problem with VME address map of Soo-Bong’s, Version 2
  More spaced-out address map- implemented in code 1/30
  Controller talks to mezzanines, so next:
  → Test HL interface input / DP programming (2/1-7?)
  → Test HL data path from MB test stand to VME b/p Eric’s test
  → Check standalone run w/ muon board in L2 crate at B0

Suggestions as to a date?