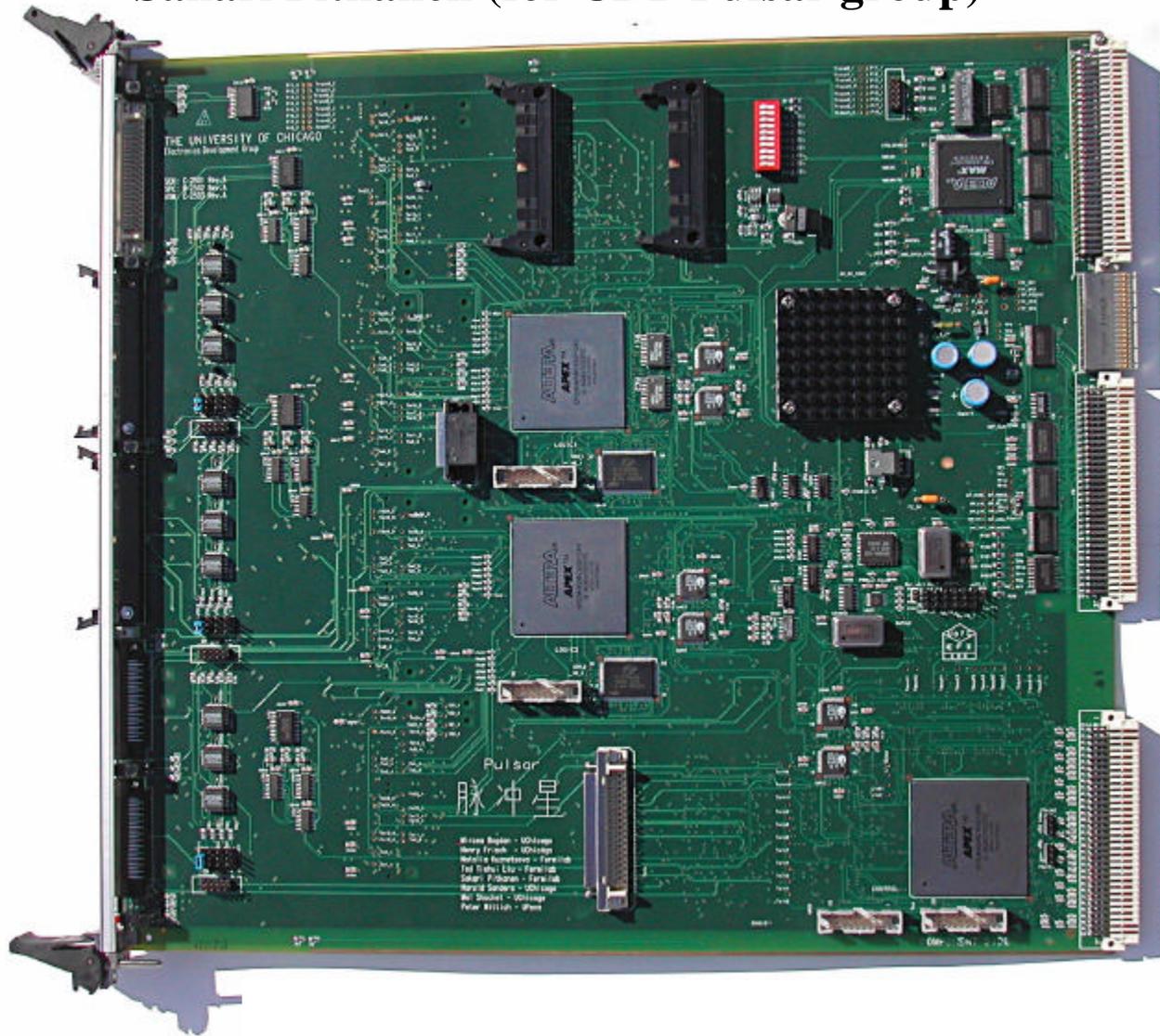


Initial testing results for Pulsar prototype

Sakari Pitkänen (for CDF Pulsar group)



For more information about Pulsar board:

<http://hep.uchicago.edu/~thliu/projects/Pulsar/>

Pulsar design methodology and tools

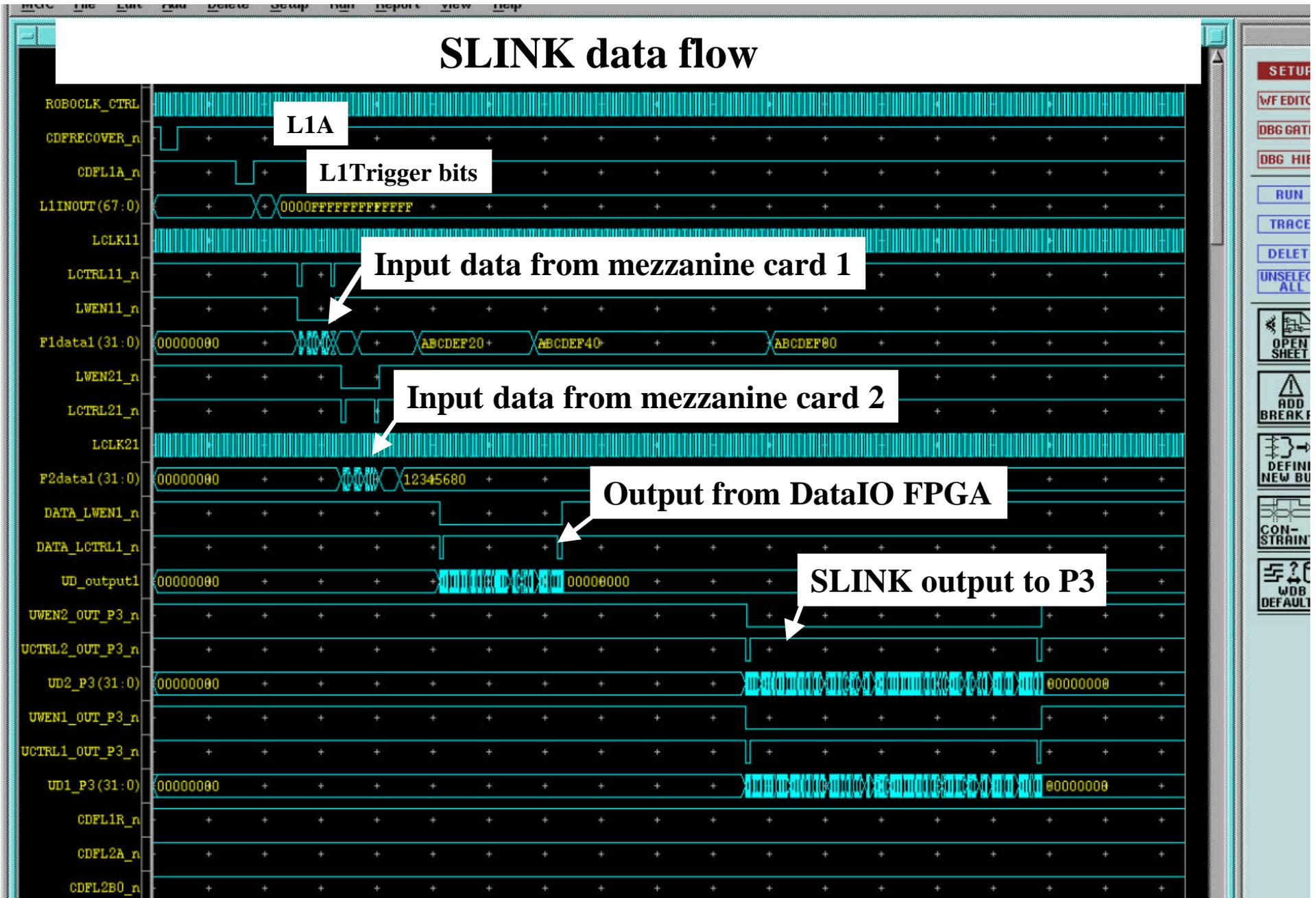
Lots of work went into preparation for the prototype testing before we received Pulsar prototype boards

- Pulsar is designed to be self-testable
- Core firmware was developed to guide and optimize the board design
- A lot of simulation done in design phase (FPGA level and board level)
- Board schematics were carefully verified with extensive board level simulations
- Trace and cross talk analysis to verify layout
- VME testing software developed and tested on other existing boards

Many of the test tools were already used in the design phase

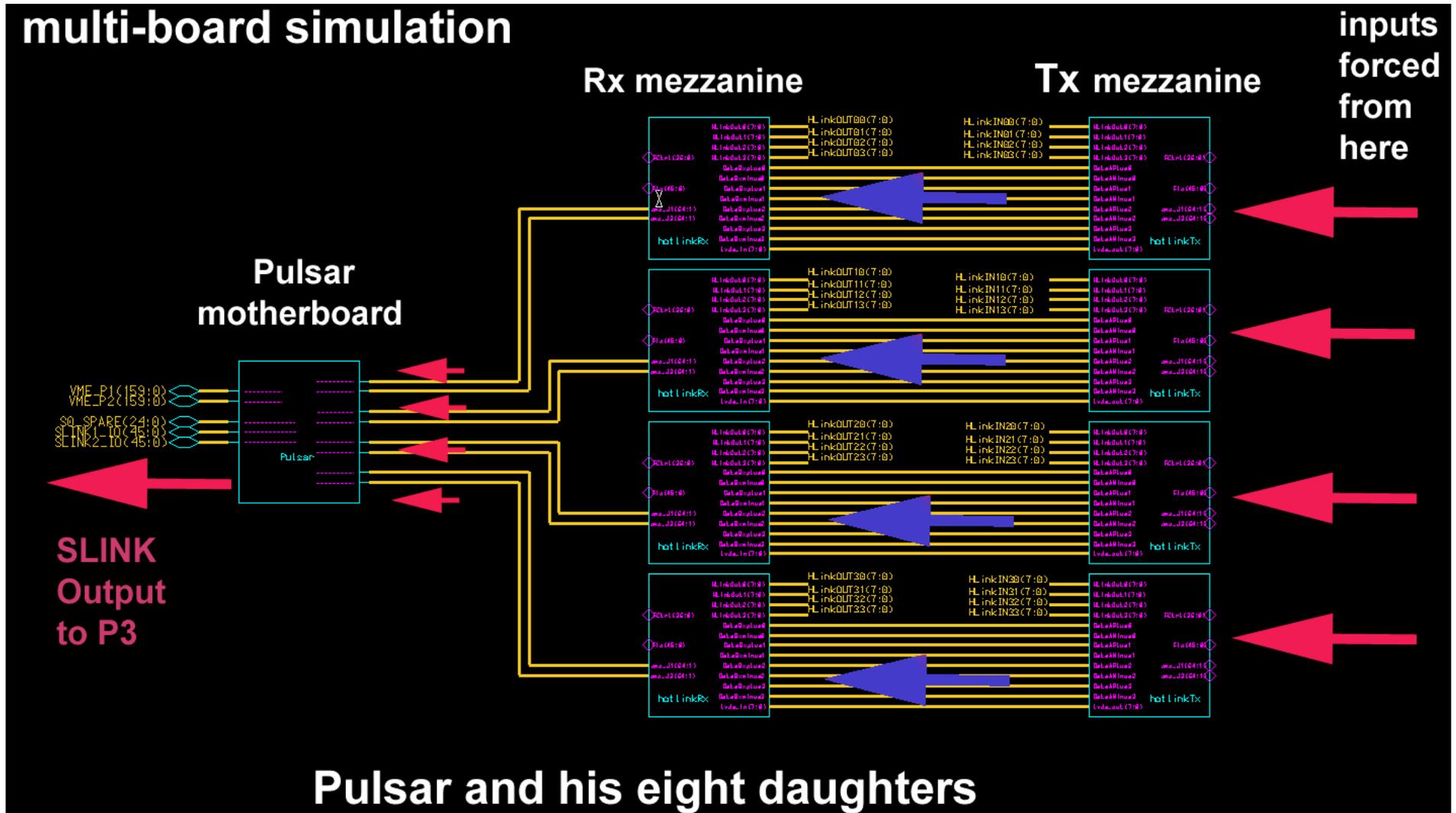
- **Leonardo Spectrum** VHDL synthesis
- **Quartus II** Place and route, and FPGA level simulation
- **QuickSim** Board and multi-board level simulation
- **Interconnect Synthesis** Trace and cross talk analysis
- **IS_MultiBoard** Signal integrity checks between motherboard and mezzanine cards

Board Level simulation



Multi-board simulation

- Performed to verify the design

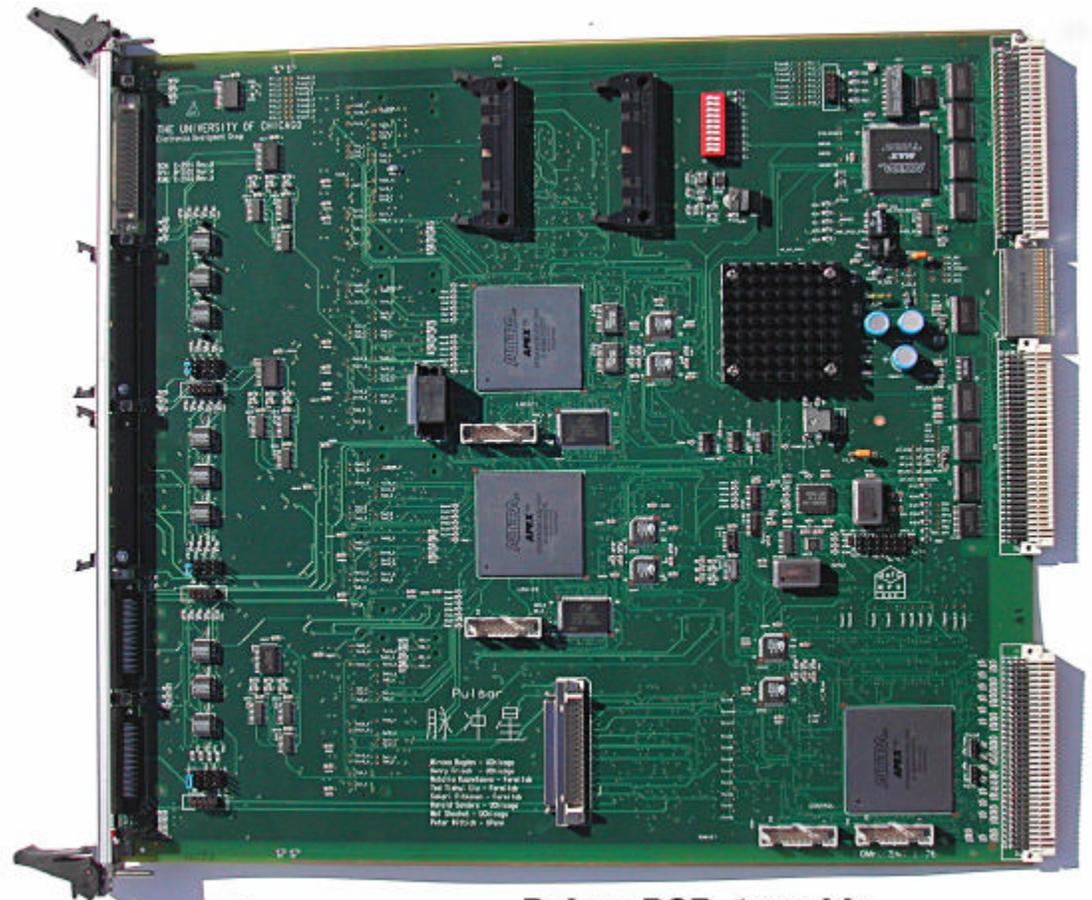
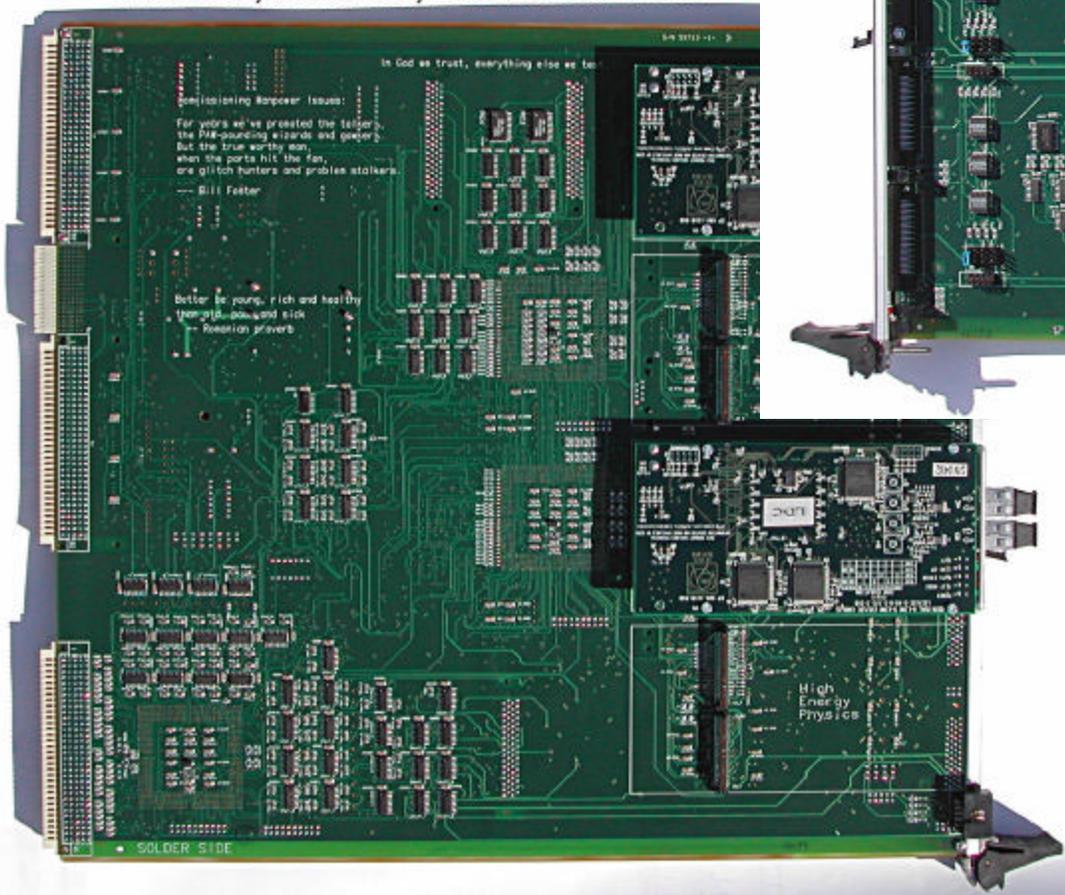


Pulsar and his eight daughters

Two Pulsar prototypes received

Sept. 19th, 2002

Pulsar PCB, bottom side, with two S-Link LDC's

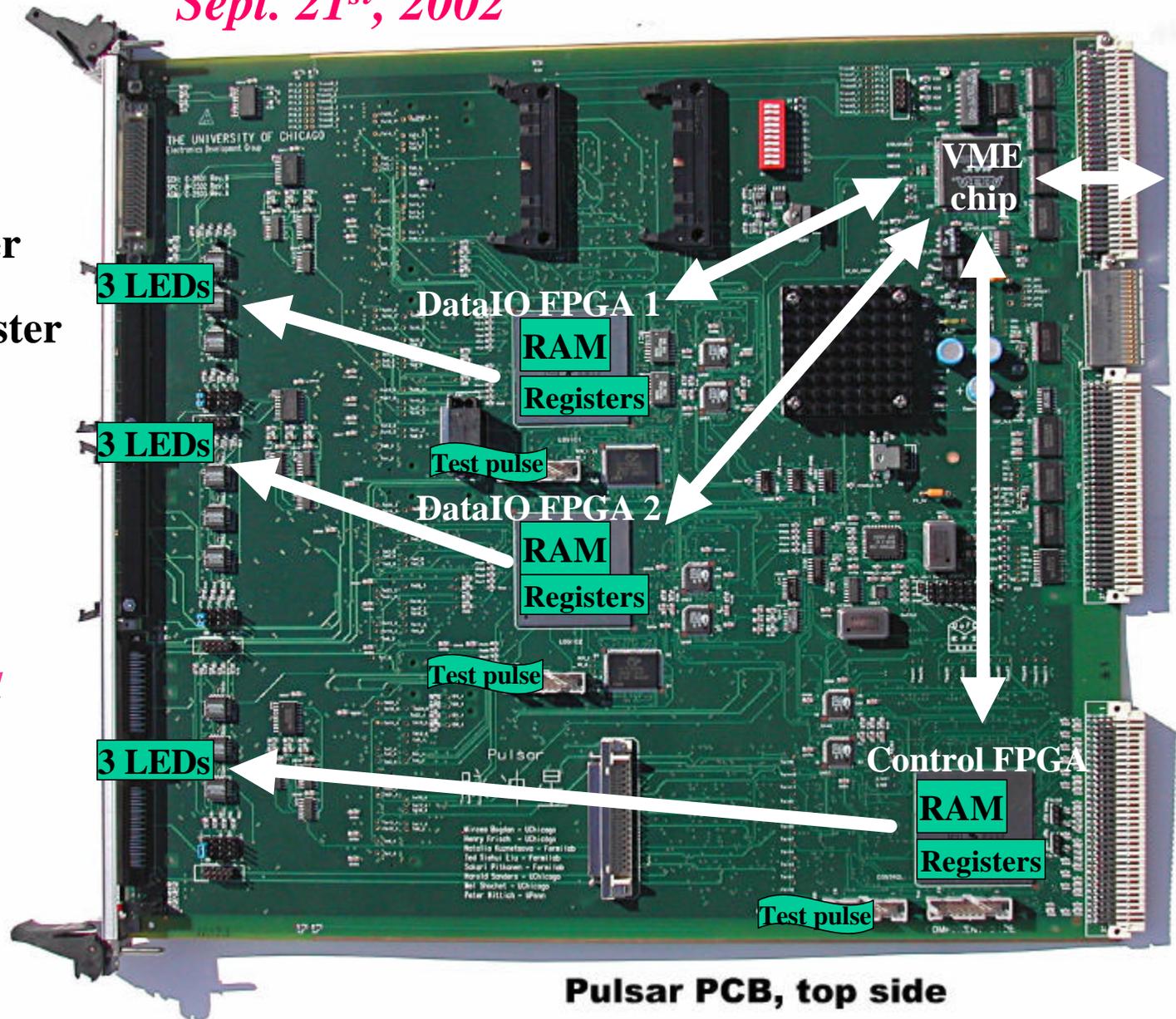


Pulsar PCB, top side

Initial VME access to all three FPGAs

Sept. 21st, 2002

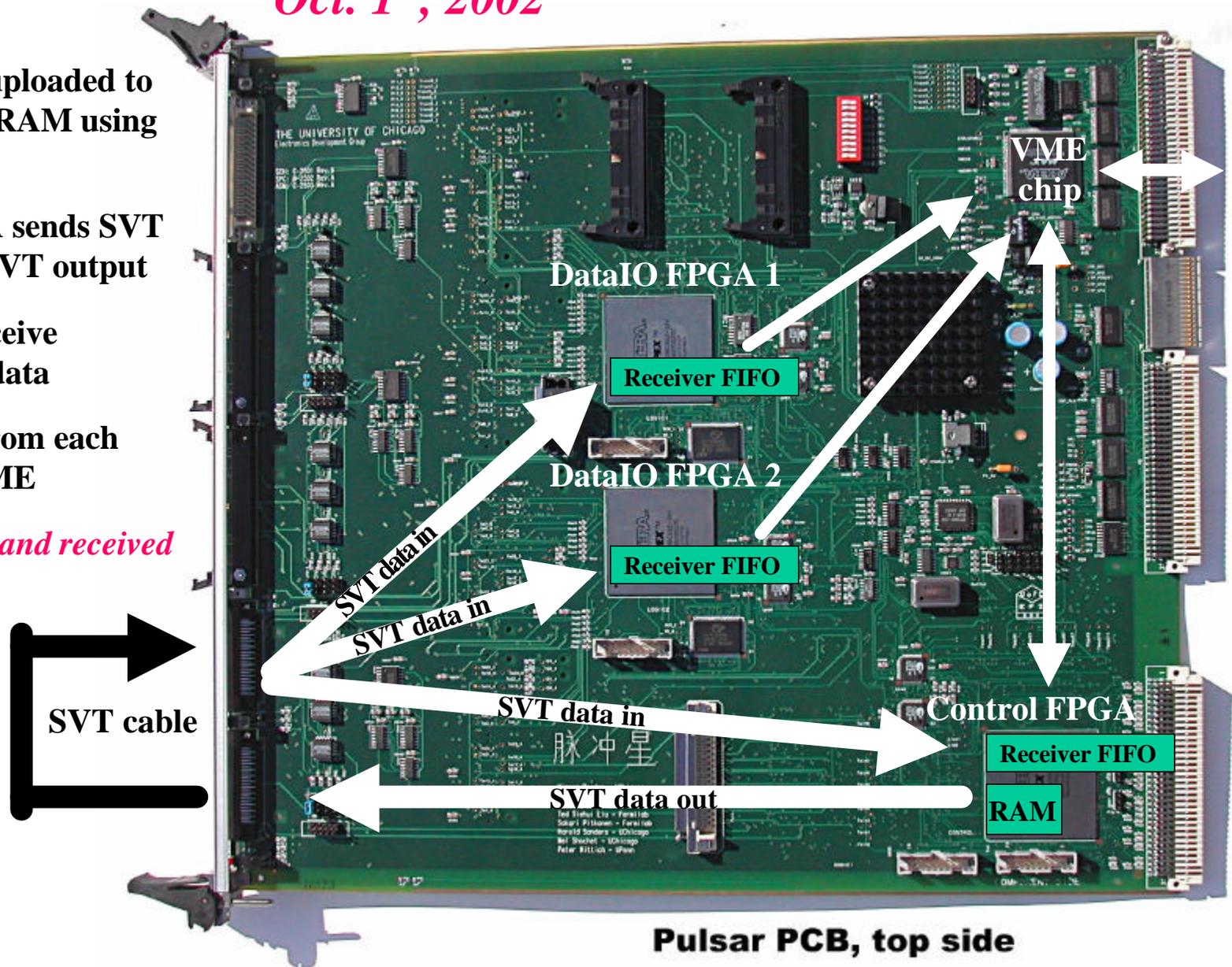
- Read only register
- Read / write register
- LEDs
- Internal RAM
- Test pulse
- *VME access to all FPGAs works*



SVT data path

Oct. 1st, 2002

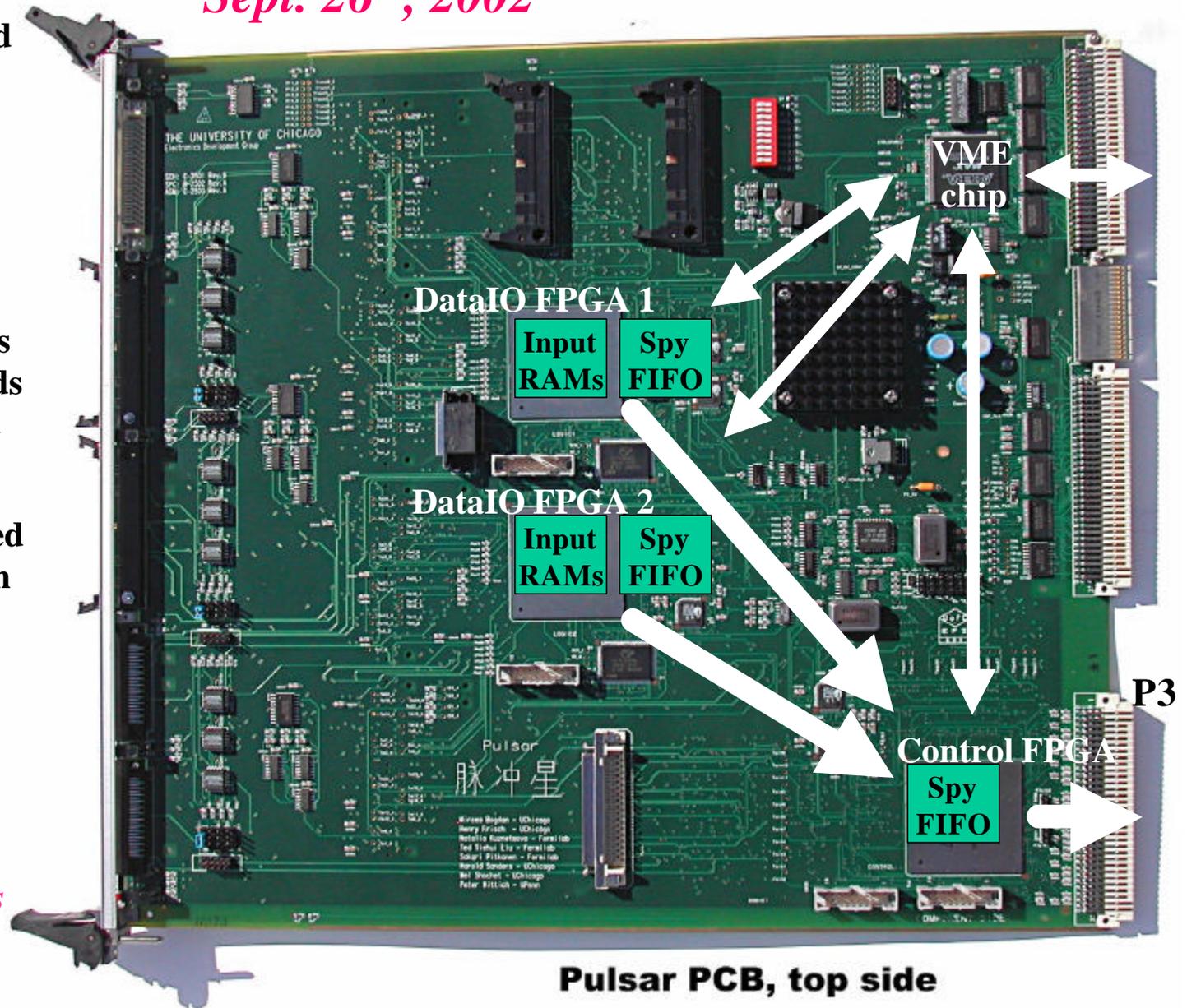
- Input data is uploaded to Control FPGA RAM using VME
- Control FPGA sends SVT data out from SVT output
- All FPGAs receive incoming SVT data
- Data is read from each FPGA using VME
- *Sent SVT data and received SVT data match*



SLINK formatting

Sept. 26th, 2002

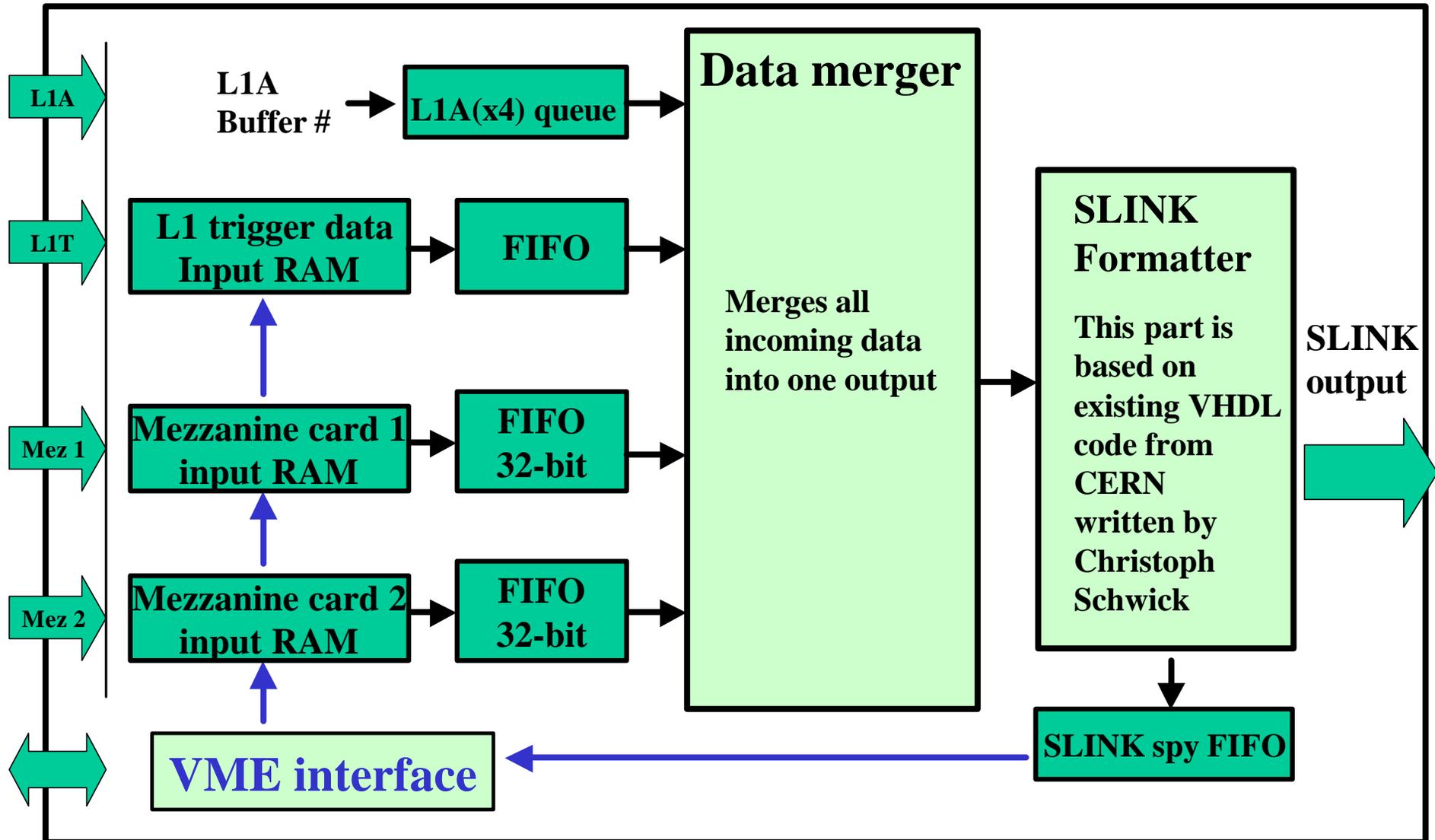
- Input data is uploaded to both DataIO FPGAs
- DataIO FPGAs send merged input data in SLINK format to Control FPGA
- Control FPGA merges incoming data and sends it out in SLINK format from P3
- Outgoing data is stored into a Spy FIFO in each FPGA, and it can be read from the FIFOs using VME
- *Data in the Control FPGA Spy FIFO matches the data uploaded to input RAMs*



SLINK formatting

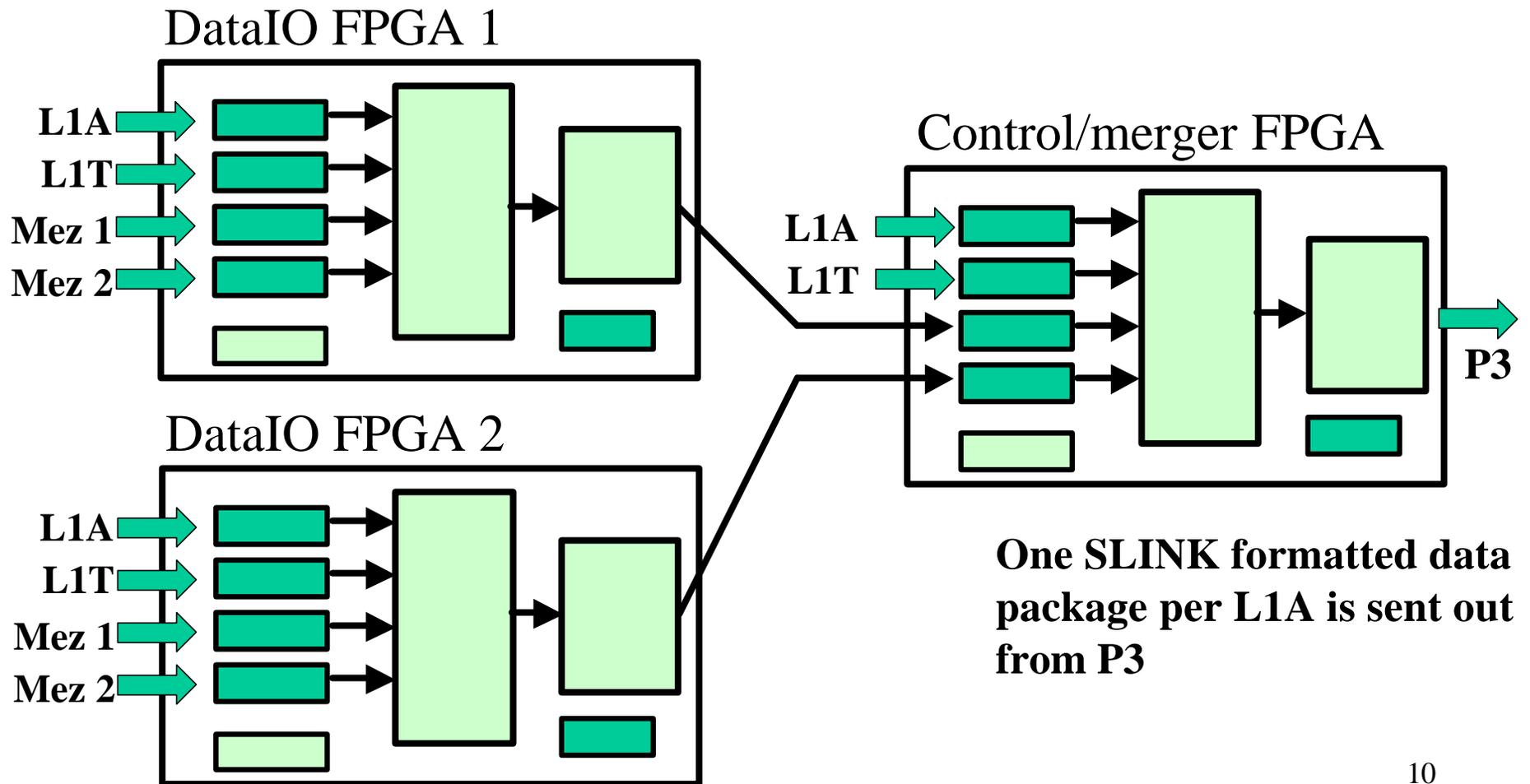
DataIO FPGA firmware:

Input data merged and formatted into SLINK output



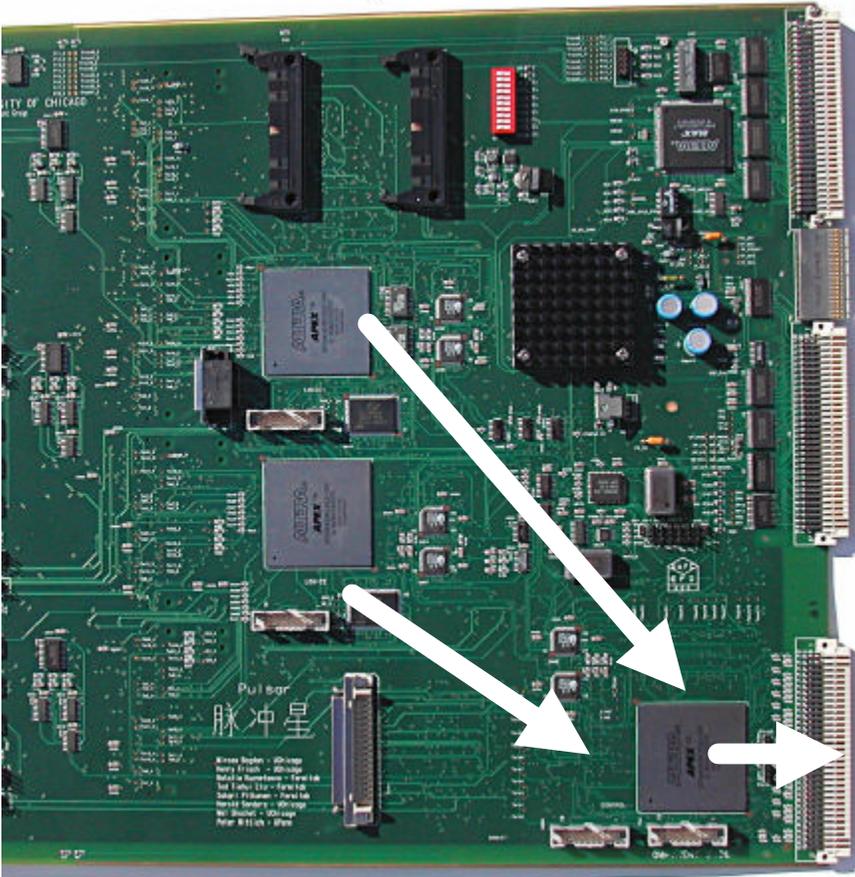
SLINK formatting

Firmware design is similar in all three FPGA's on all versions of the Pulsar

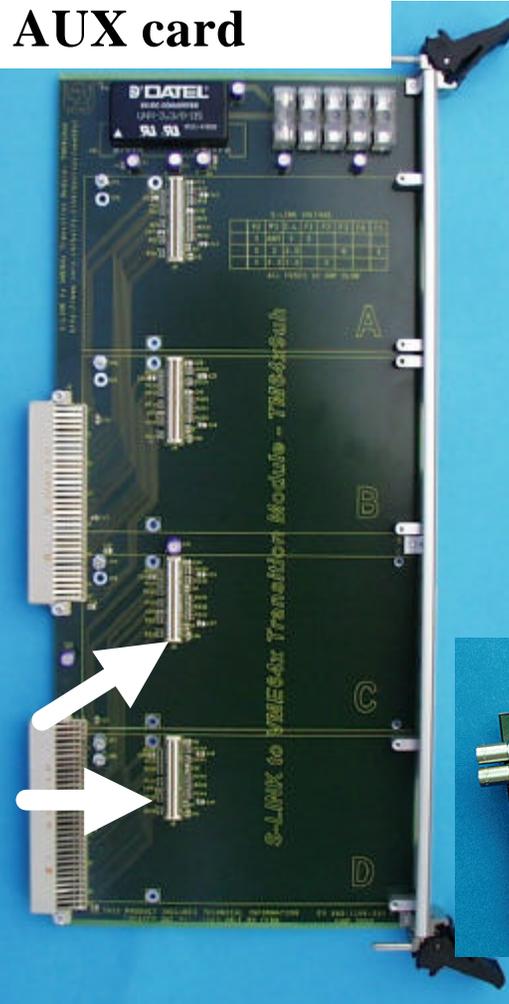


SLINK formatting

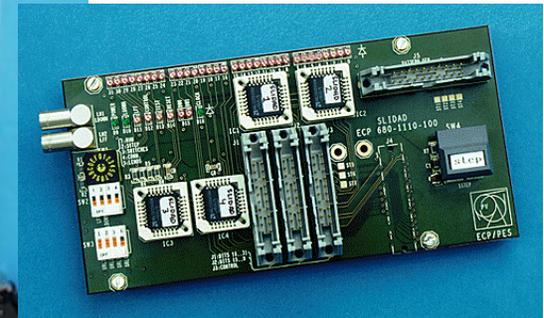
- Outgoing SLINK data goes from P3 to AUX card, which has a SLINK SLIDAD on it
- Outgoing data was checked with logic analyser from SLIDADs debug pins
- *Data seen in the SLIDAD matches the data uploaded to input RAMs*



Pulsar PCB, top side



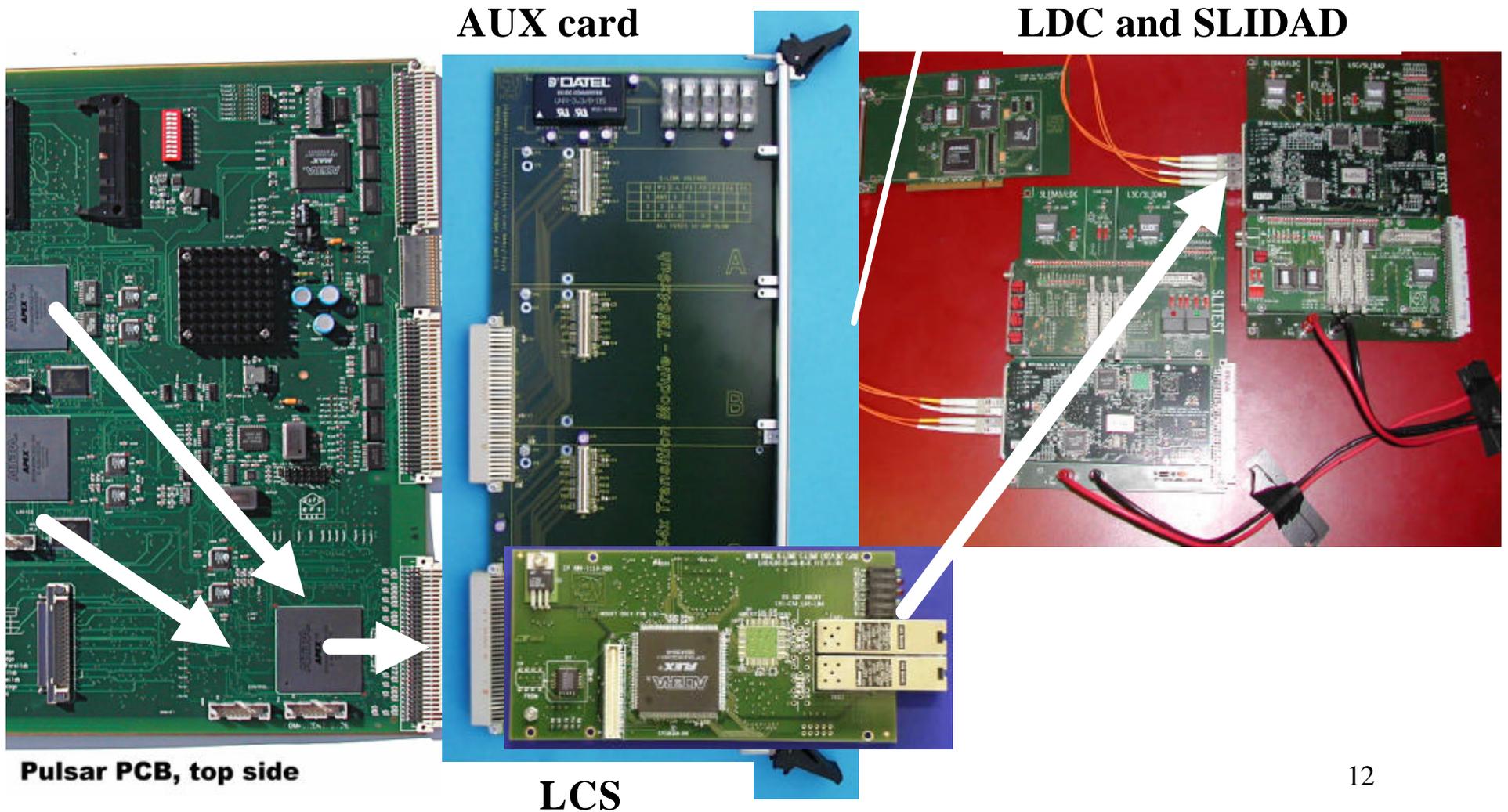
AUX card



SLIDAD

SLINK formatting

- SLINK LSC sends the data trough fiber to SLINK LDC, which is connected to SLINK SLIDAD



SLINK formatting

Oct. 3th, 2002

- Data seen in the SLINK SLIDAD matches the data uploaded to input RAMs

The screenshot displays a logic analyzer interface with two panels. The top panel shows capture settings for 'Waveform 1' with a 1M sample rate. The bottom panel shows a listing of captured data points.

Top Panel Settings:

- 1M Sample LA C
- Waveform 1
- Acq. Control
- Cancel
- Run
- Accumulate Off
- UD X → B0F00000
- Hex D → FFFF0031
- Center Screen
- sec/Div 320 ns
- Delay 979.9 ns
- Markers Time
- X to 0 265.0 ns
- Trig to X 15.00 ns
- Trig to 0 280.0 ns

Bottom Panel Settings:

- 1M Sample LA C
- Listing 1
- Cancel
- Run
- Markers Time
- Trig to X 15 ns
- Trig to 0 280 ns
- X to 0 265 ns

Data Listing Table:

Label>	UD	UCTRL_	UWEN_	LFF_	LFF_	UTEST_	UCLK	UCLK	Ti
Base>	Hex	Hex	Hex	Hex	Hex	Hex	Hex	Hex	Re
91	D0110101	1	0	1	1	1	0	0	
92	D0110101	1	0	1	1	1	0	0	
93	D0110101	1	0	1	1	1	1	1	
94	D0110101	1	0	1	1	1	1	1	
95	D0110101	1	0	1	1	1	1	1	
96	D0110202	1	0	1	1	1	0	0	
97	D0110202	1	0	1	1	1	0	0	
98	D0110202	1	0	1	1	1	1	1	
99	D0110202	1	0	1	1	1	1	1	
100	D0110202	1	0	1	1	1	1	1	
101	D0110303	1	0	1	1	1	0	0	
102	D0110303	1	0	1	1	1	0	0	
103	D0110303	1	0	1	1	1	1	1	
104	D0110303	1	0	1	1	1	1	1	
105	D0110303	1	0	1	1	1	1	1	
106	D0110404	1	0	1	1	1	0	0	

Problems we have had so far

- **Wrong VME buffer chips loaded to the prototype board**
- **One solder bridge**
- **Three cold solder joints on some components**
- **One resistor was not loaded**
- **Small bugs inside firmware which were not found during simulation**

Initial prototype testing done

- **VME access to all FPGAs**
- **SVT data path (in and out)**
- **SLINK data formatting and output to AUX card**

What's left to be done

- **Pulsar → AUX card → SLINK-PCI → PC memory**
- **SLINK mezzanine cards → Pulsar → ...**
- **RF machine clock interface**
- **L1 data path**
- **TS interface connection**
- **SRAM access**
- **Hotlink/Taxi mezzanine cards**
- **Robustness and clock speed testing!**
- **...**

