Initial testing results for Pulsar prototype
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For more information about Pulsar board:
http://hep.uchicago.edu/~thliu/projects/Pulsar/
Pulsar design methodology and tools

Lots of work went into preparation for the prototype testing before we received Pulsar prototype boards

• Pulsar is designed to be self-testable
• Core firmware was developed to guide and optimize the board design
• A lot of simulation done in design phase (FPGA level and board level)
• Board schematics were carefully verified with extensive board level simulations
• Trace and cross talk analysis to verify layout
• VME testing software developed and tested on other existing boards

Many of the test tools were already used in the design phase

• Leonardo Spectrum  VHDL synthesis
• Quartus II  Place and route, and FPGA level simulation
• QuickSim  Board and multi-board level simulation
• Interconnect Synthesis  Trace and cross talk analysis
• IS_MultiBoard  Signal integrity checks between motherboard and mezzanine cards
Board Level simulation

SLINK data flow

Input data from mezzanine card 1
Input data from mezzanine card 2
Output from DataIO FPGA
SLINK output to P3
Multi-board simulation

• Performed to verify the design
Two Pulsar prototypes received

*Sept. 19th, 2002*

*Pulsar PCB, bottom side, with two S-Link LDC's*

*Pulsar PCB, top side*
Initial VME access to all three FPGAs

Sept. 21st, 2002

- Read only register
- Read / write register
- LEDs
- Internal RAM
- Test pulse

- VME access to all FPGAs works
SVT data path

Oct. 1st, 2002

- Input data is uploaded to Control FPGA RAM using VME
- Control FPGA sends SVT data out from SVT output
- All FPGAs receive incoming SVT data
- Data is read from each FPGA using VME
- Sent SVT data and received SVT data match
• Input data is uploaded to both DataIO FPGAs

• DataIO FPGAs send merged input data in SLINK format to Control FPGA

• Control FPGA merges incoming data and sends it out in SLINK format from P3

• Outgoing data is stored into a Spy FIFO in each FPGA, and it can be read from the FIFOs using VME

• Data in the Control FPGA Spy FIFO matches the data uploaded to input RAMs
SLINK formatting

DataIO FPGA firmware:
Input data merged and formated into SLINK output

VME interface

Mezzanine card 1 input RAM

Mezzanine card 2 input RAM

L1 trigger data Input RAM

L1A Buffer #

L1A(x4) queue

FIFO

FIFO

FIFO

32-bit

32-bit

32-bit

Data merger

Merges all incoming data into one output

SLINK Formatter

This part is based on existing VHDL code from CERN written by Christoph Schwick

SLINK spy FIFO
Firmware design is similar in all three FPGA’s on all versions of the Pulsar

One SLINK formatted data package per L1A is sent out from P3
SLINK formatting

• Outgoing SLINK data goes from P3 to AUX card, which has a SLINK SLIDAD on it
• Outgoing data was checked with logic analyser from SLIDADs debug pins
• Data seen in the SLIDAD matches the data uploaded to input RAMs
SLINK formatting

- SLINK LSC sends the data through fiber to SLINK LDC, which is connected to SLINK SLIDAD.
SLINK formatting
Oct. 3rd, 2002

- Data seen in the SLINK SLIDAD matches the data uploaded to input RAMs
Problems we have had so far

• Wrong VME buffer chips loaded to the prototype board

• One solder bridge

• Three cold solder joints on some components

• One resistor was not loaded

• Small bugs inside firmware which were not found during simulation
Initial prototype testing done

- VME access to all FPGAs
- SVT data path (in and out)
- SLINK data formatting and output to AUX card

What’s left to be done

- Pulsar → AUX card → SLINK-PCI → PC memory
- SLINK mezzanine cards → Pulsar → …
- RF machine clock interface
- L1 data path
- TS interface connection
- SRAM access
- Hotlink/Taxi mezzanine cards
- Robustness and clock speed testing!
- …