

# **Current Status of the L2 Decision Crate**



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**CDF Level 2 Trigger System Review**  
**August 1, 2002**

# Outline



- Introduction
- Current status
  - Hardware
  - Software
- How close to Run 2A specifications?
- Conclusions

# Current status

- Run 148948; Store 1583
  - Initial Lum =  $2.8e31$
  - PHYSICS\_1\_02[1,110,306]
  - no Silicon
- L1A/L2A = 11.8 kHz/225 Hz @  $2.5e31$
- Deadtime = 2.6% total
  - 1.0% L2 processing
  - 1.1% L2 or VME
- Trigger continues to work at record Lum!

**XMon Summary**

Run 148948 Latest Event 528835  
 Run Type Physics Data Type Beam Data  
 Experiment Type Physics Run 2a  
 Partition 0 Tev Store 1583  
 Physics Table PHYSICS\_1\_02[1,110,306]  
 Myron mode NO Latest Event Flag 0

Activate Time 14:49:30 2002.07.26 (from database)  
 Current Time 15:29:19 2002.Jul.26 (from LRIH bank)  
 Terminate Time 15:29:11 2002.07.26 (from database)

Time	seconds	%
Live	2290.83	97.42
Dead	60.67	2.58
Run	2351.50	100.00
Gfred	2351.50	100.00

Luminosity	no GLIVE			GLIVE		
	Initial	Current Event	Run Average	Initial	Current Event	Run Average
Instantaneous ( $\text{cm}^{-2} \text{s}^{-1}$ )	$2.79e+31$	$2.50e+31$	$2.63e+31$	$0.00e+00$	$1.95e+31$	$2.55e+31$
Integrated ( $\text{nb}^{-1}$ )	9.56	73.80	64.25	0.00	60.24	60.24

Level	count	rate (Hz)	Hot trigger bits	Cold trigger bits
FRED L1 accepts	27654224	11760.23	N/A	N/A
L1 accepts	26937895	11455.60	9 15	25 27 30
L2 accepts	528835	224.89	12 51	13 14 15 16 18 28 33 34 38
L2 rejects	26409053	11230.70		39 50 58 59 68 69 70 79 80 81 82 83

# Current Status w/Silicon

- Run 148950; Store 1583
  - Initial Lum =  $2.3e31$
  - PHYSICS\_1\_02[1,110,306]
  - Silicon biased
- L1A/L2A = 8.6 kHz/200 Hz @  $2.2e31$
- Deadtime = 4.9% total
  - 0.7% L2 processing
  - 1.3% L2 or VME
- Trigger continues to work at record Lum!

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### XMon Summary

Run 148950 Latest Event 783824  
 Run Type Physics Data Type Beam Data  
 Experiment Type Physics Run 2a  
 Partition 0 Tev Store 1583  
 Physics Table PHYSICS\_1\_02[1,110,306]  
 Myron mode NO Latest Event Flag 0

Activate Time 16:08:16 2002.07.26 (from database)  
 Current Time 17:15:04 2002.Jul.26 (from LRIH bank)  
 Terminate Time 17:17:09 2002.07.26 (from database)

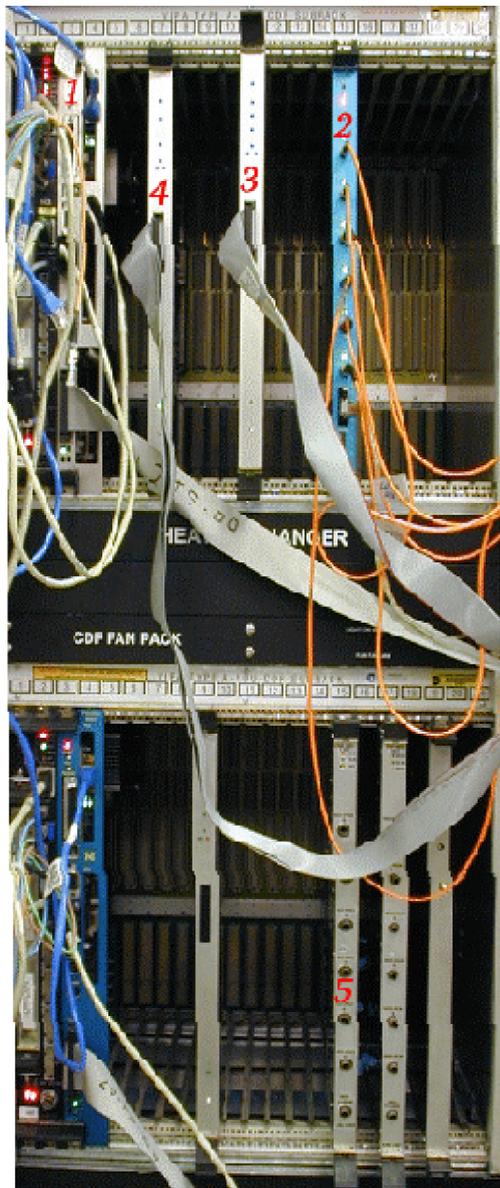
Time	seconds	%
Live	3781.18	95.08
Dead	195.51	4.92
Run	3976.69	100.00
Gfred	3976.69	100.00

Luminosity	no GLIVE			GLIVE		
	Initial	Current Event	Run Average	Initial	Current Event	Run Average
Instantaneous ( $\text{cm}^{-2} \text{s}^{-1}$ )	$2.25e+31$	$2.07e+31$	$2.17e+31$	$0.00e+00$	$0.00e+00$	$2.10e+31$
Integrated ( $\text{nb}^{-1}$ )	128.37	219.07	90.70	68.56	150.94	82.37

Level	count	rate (Hz)	Hot trigger bits	Cold trigger bits
FRED L1 accepts	35933038	9035.91	N/A	N/A
L1 accepts	34195930	8599.09	15	1 5 7 24 25 27 30
L2 accepts	783824	197.10	15 16 77 82	1 3 22 28 33 34 38 39 47 50
L2 rejects	33412065	8401.98		58 59

# L2 Decision Crate

*BOL2DE00 - 2RR30C T*



1. ALPHA
2. CLIST
3. SVTLIST
4. XTRPLIST
5. ISOLIST

*On the Backplane :*  
A. L1 INTERFACE  
B. ReCES

*BOL2DE01 - 2RR30C B*

- L2 processor: Alpha
- Backplane: Magic Bus
- 9U cards:
  - Clusterlist
  - Tracklist (XTRP/SVT)
  - Isolist
- Transition cards:
  - L1 interface
  - Reces (SMX)

# L2 Hardware



- Recommendations for summer 2002 from L2 review committee in December 2001:
  - complete tests of new backplane and mods to the individual interface cards
    - As of June shutdown both L2 decision crates have new backplanes and been tested with full systems
    - All boards modified for TTL *except* one ISOlister at Argonne for use in their PECL teststand
  - have more than one fully tested and working board of each type at B0

# L1 interface



- 1 board needed per L2 decision crate
- 2 physics-ready spares at B0
- 24/7 pager coverage (Greg)
- Board repair at Argonne by engineers
- Future plans:
  - replace/upgrade = none
  - build more spares = none

# Clusterlist



- 1 board needed per L2 decision crate
- 2 spares:
  - 1 with "VME" problem at Michigan
  - 1 physics-ready at B0
- 24/7 on-site coverage (Heather)
- Board repair at Michigan (Monica) or B0 (Heather)
- Future plans:
  - replace/upgrade = none
  - build more spares = none

# XTRPlist



- 1 board needed per L2 decision crate
- 2 physics-ready spares at B0
- 24/7 on-site coverage (Matt)
- Board repair at UCLA (Jane) or B0 (Matt)
- Future plans:
  - replace/upgrade = none
  - build more spares = none

# SVTlist



- 1 board per L2 decision crate
- 1 board in SVT for VME readout
- 1 physics-ready spare at B0
  - Conversion between SVTlist and XTRPlist is simple so XTRPlist and SVTlist spares can easily be swapped
- 24/7 on-site coverage (Matt)
- Board repair at UCLA (Jane) or B0 (Matt)
- Future plans:
  - replace/upgrade = none
  - build more spares = none

# ISOList



- 1 board needed per L2 decision crate
- 1 physics-ready spare at B0
  - 1 PECL board at Argonne
- Expert coverage (Steve K.)
- Board repair at Argonne by engineers
- Future plans:
  - replace/upgrade = none
  - build more spares = none

# Reces



- 4 boards needed per L2 decision crate
- 2 spares at B0:
  - 1 physics-ready; 1 needs testing
- Expert coverage (Masa, Karen)
- Board repair at Argonne by engineers
- Future plans:
  - replace/upgrade = none
  - build more spares = none

# Alpha



- 1 board needed per L2 decision crate
- 2 physics-ready spares at B0
- Expert coverage (Stephen)
- Board repair at Michigan (Stephen)
- Future plans:
  - details in Stephen's talk

# L2 Software

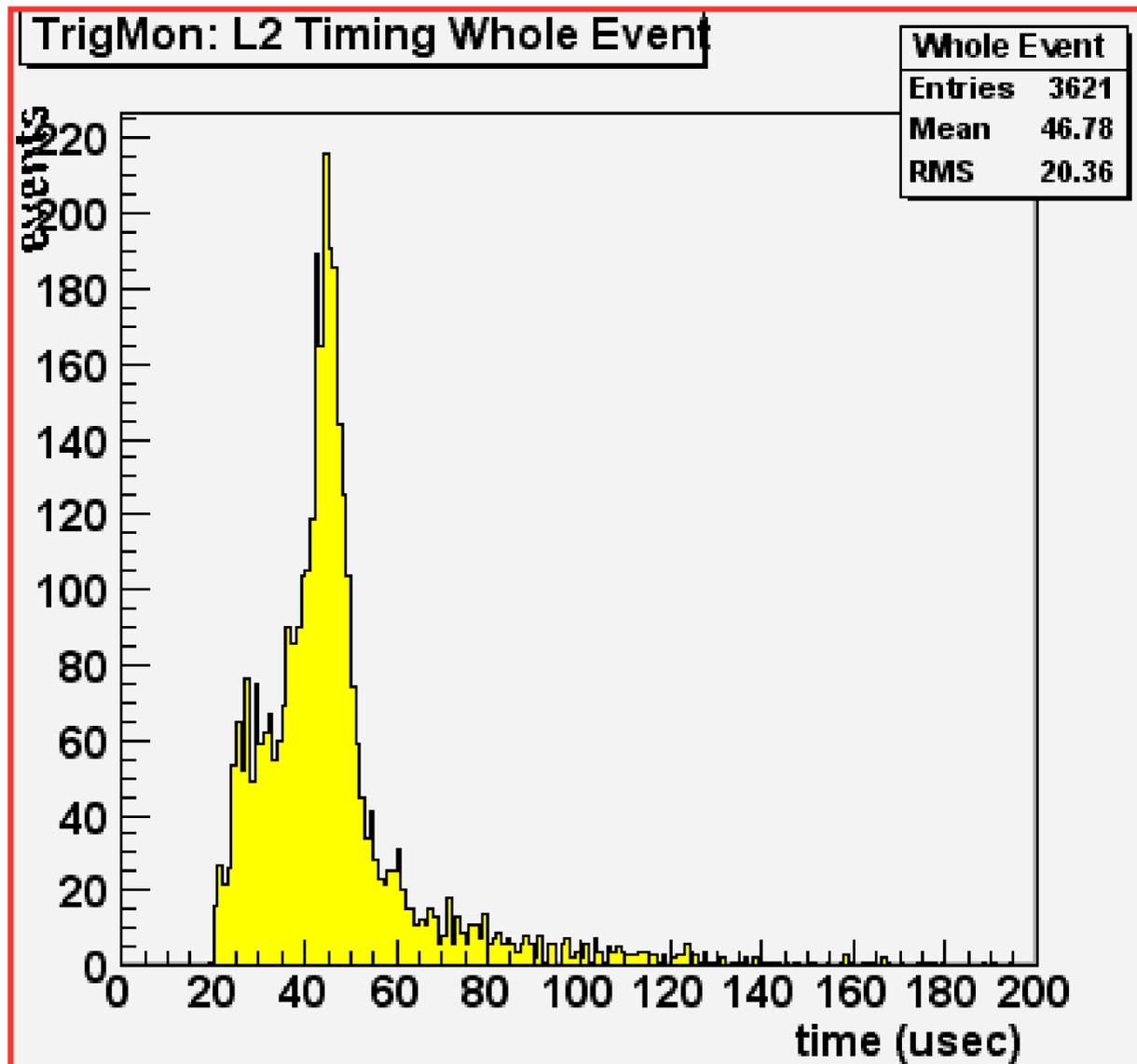


- Current default code for physics:
  - error checking at L2
  - unpacks data only when required for a trigger algorithm
  - optimized in compiler
- Each iteration of L2 code is given a unique tagset
- L2 trigger algorithms:
  - Jets
  - Photon (+ SVT)
  - Electron (+ SVT)
  - Shower Max
  - SVT track
  - Hadronic B
  - J/Psi  $\rightarrow$  ee
  - Electron + XFT track

# L2 error handling

- Error checking done within the Alpha
  - Alpha checks:
    - L2 buffer number per Clist cluster
    - L2 buffer in end of event word from XTRP/SVTlist
    - Number of Magic Bus transfers by L1 interface
  - If an error is detected, the Alpha doesn't send a decision to the TS → "L2 decision timeout"
    - Shift crew must HRR to clear L2 buffers
    - At  $L > 1.5e31$  timeouts come every 2-3 hrs
- L1/L2 error trigger
  - events with errors in the data can be sent to a error filter at L3
  - still in development

# L2 processing time



- Current times in the L2 system:
  - Mean L2 processing time: 25  $\mu$ s
  - Mean SVX/SVT processing time: 29  $\mu$ s
  - Mean data load on Magic Bus: 5  $\mu$ s

# How close to Run 2A specs?

- Goals from CDF 4213:
  - Target L1A/L2A rate = 45 kHz/300 Hz
  - Target deadtime at these rates  $\sim 5\%$
- Current configuration:
  - David's L2 timing MC suggests  $\sim 10\%$  deadtime from L1 at 20 kHz L1A rate  
( $L = 5e31$ )
  - L2 can handle rates at  $\sim 1/2$  of the Run 2A specs for deadtimeless trigger

# Conclusions



- L2 trigger is now one step ahead of delivered  $L \sim 2e31$
- L2 hardware has met the L2 review expectations for summer 2002
- L2 trigger algorithms approaching specifications from CDF 4718
- L2 software continues to improve timing and stability