The Silicon Vertex Trigger Upgrade at CDF

Ivan K. Furić
University of Chicago
(for the CDF Collaboration)

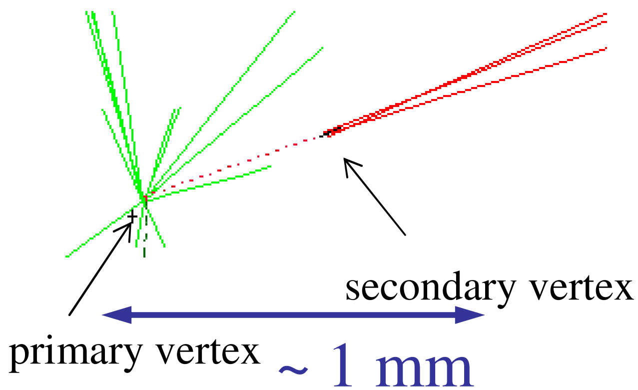
SVT Motivation

- trigger on B hadronic decays
  - Large B production cross section for B physics (CP violation in B decays, Bs mixing ..)
  - new particle searches, eg. Higgs, Supersymmetry

- particularly important at hadronic colliders
  - overwhelming QCD background $O(10^3)$

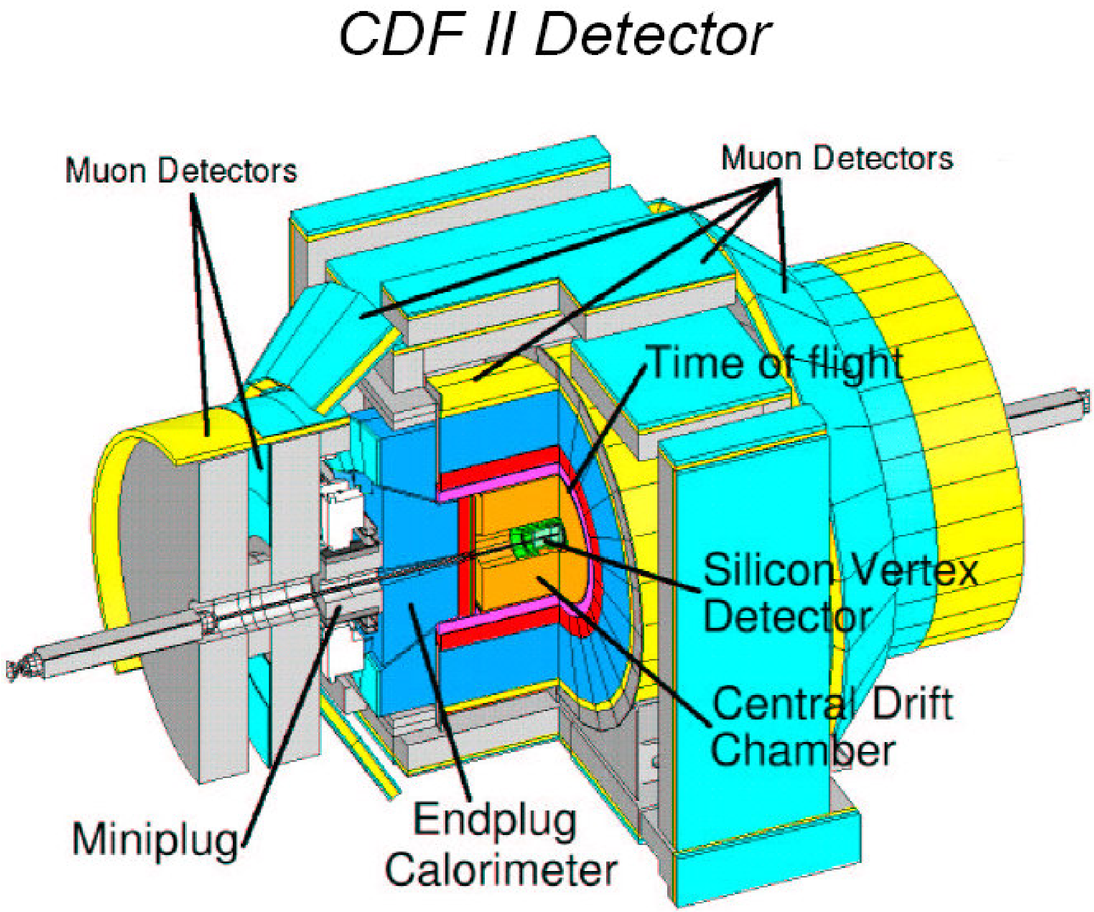
- detect displacement of B decays using the fact that $\tau(B) \approx 1.5$ ps

- typical track displacement few hundred μm need SI tracking information



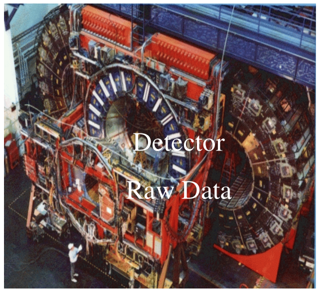
Technical challenge!

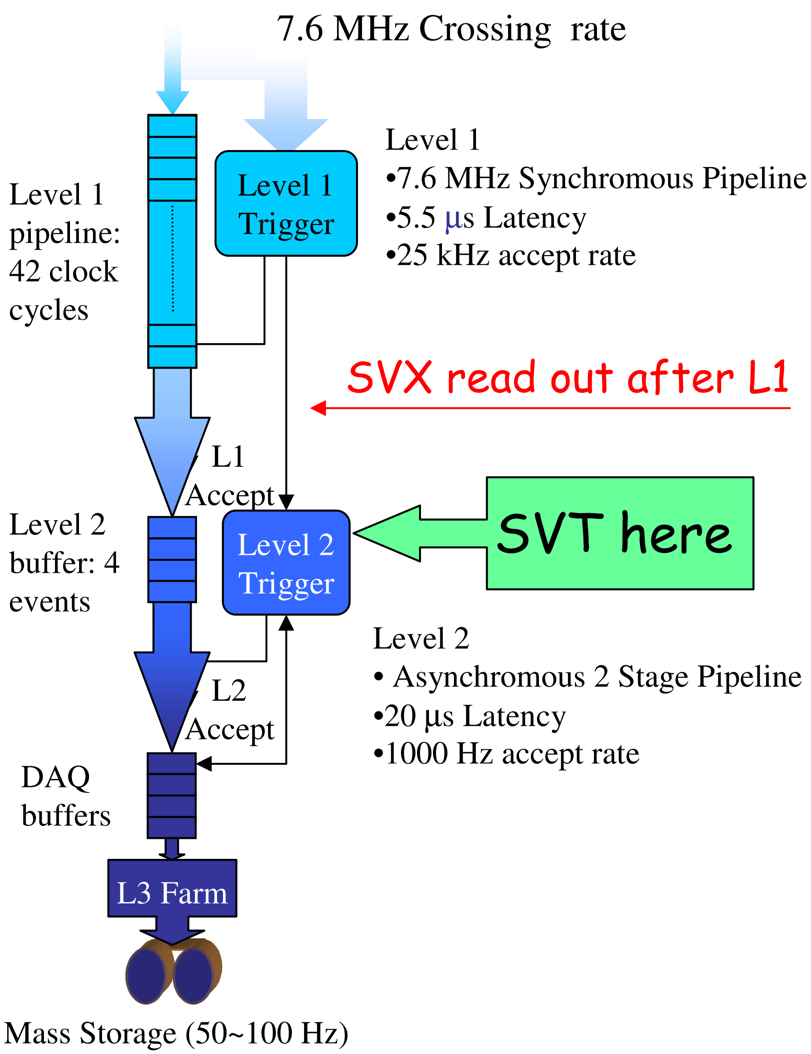
The CDFII Detector



– CDF: multi-purpose experiment, broad physics program
– Tevatron: E_{CM}=1.96 TeV, T_{bunch} = 396 ns, L ~ 100 $\times 10^{30} cm^{-2}s^{-1}$

SVT Design Constraints



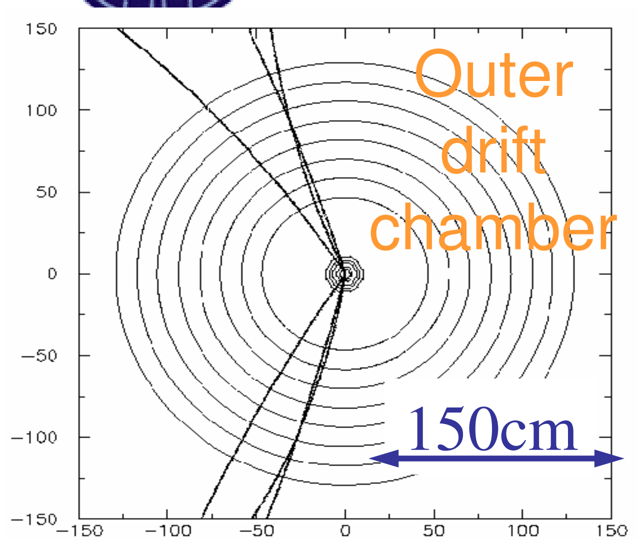


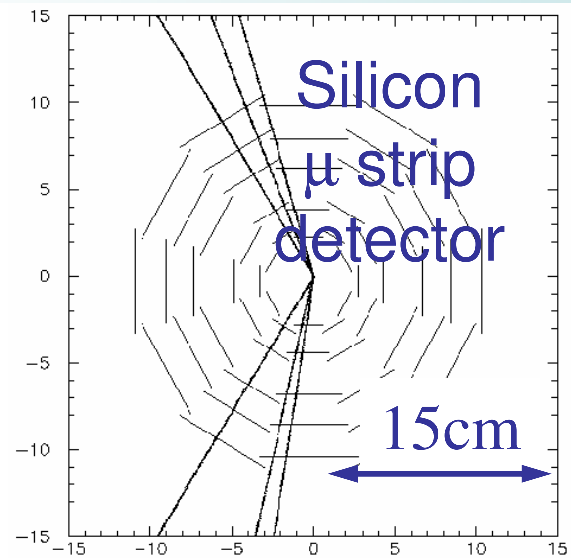
- $\sim$ 25 kHz input rate
- O(10^3) SVX strips/event
- 2-D low-res COT tracks (XFT)

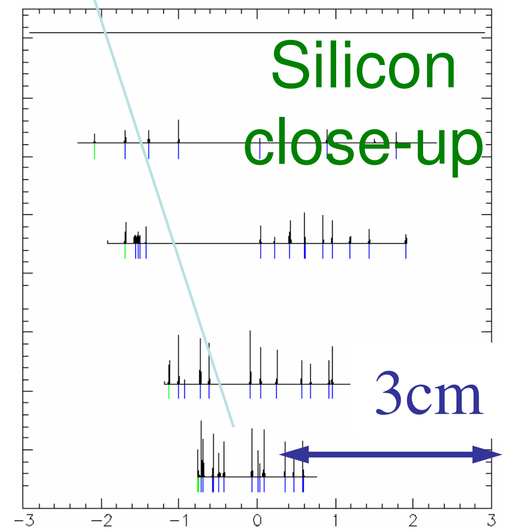
- latency O(20) µsec
- no dead time
- resolution $\approx$ offline

- parallelization is key to processing speed

Operating principle







Input (every Level 1 accept):

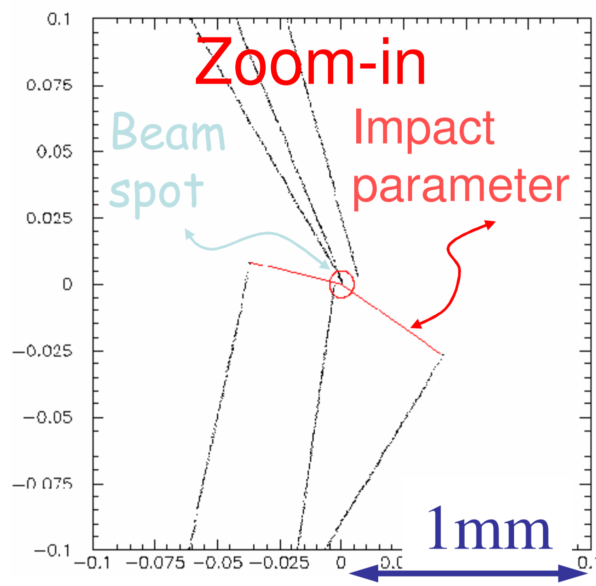
outer drift chamber trajectories

silicon pulse height for each channel

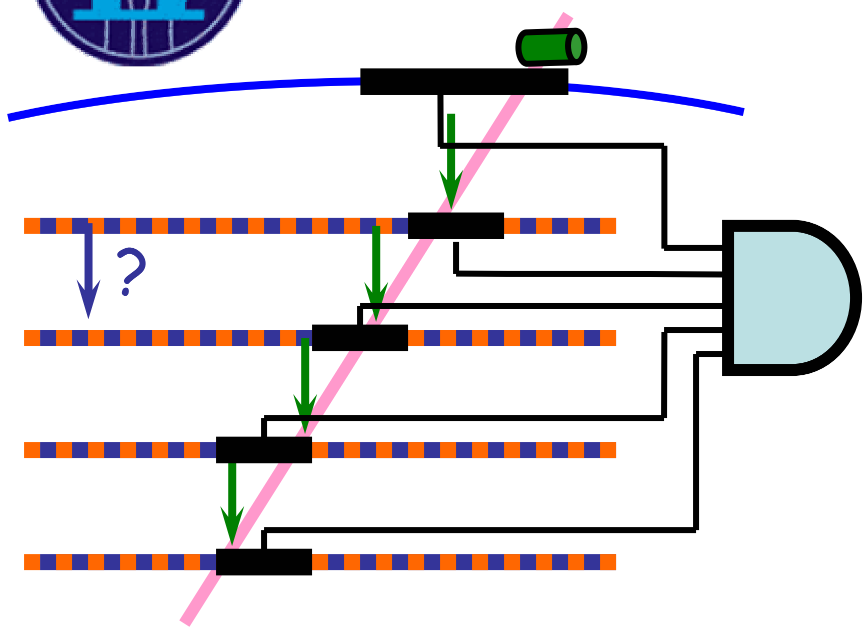
Output (about 20 microseconds later):

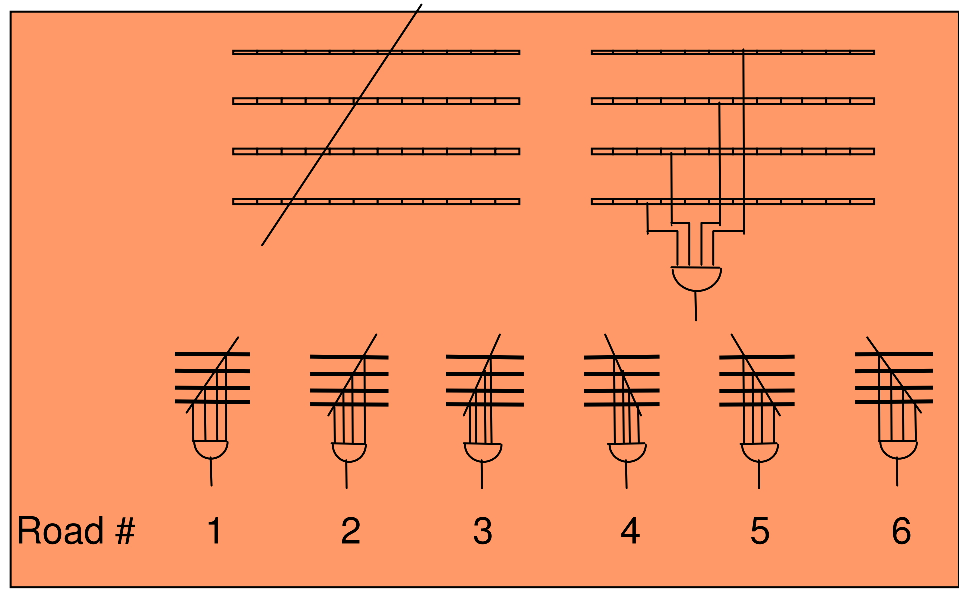
trajectories that use silicon points

impact parameter: $\sigma(d)=35\mu m$



Pattern Recognition

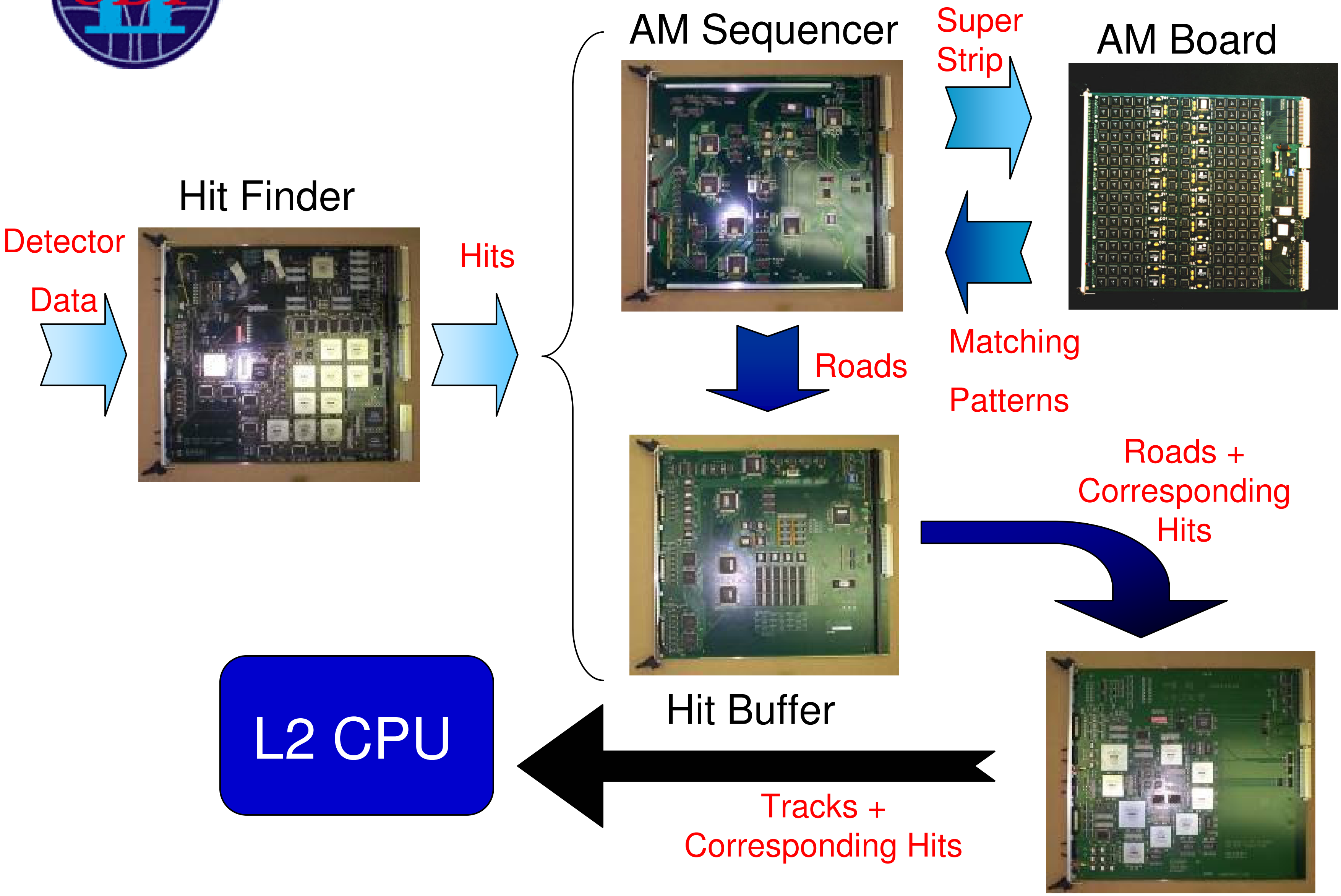




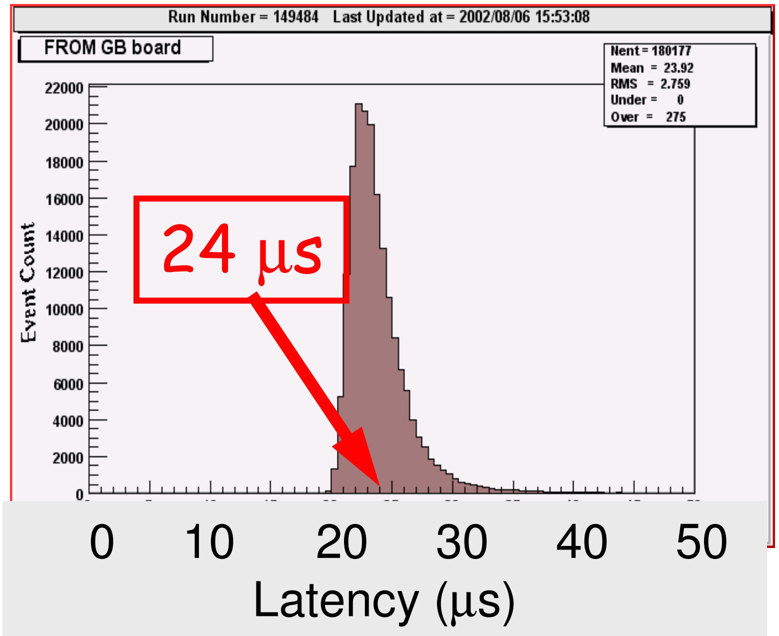
B	I	N	G	O
2	17	35	48	61
10	21	39	53	66
14	20	free	55	65
8	25	41	52	62
6	16	37	46	67

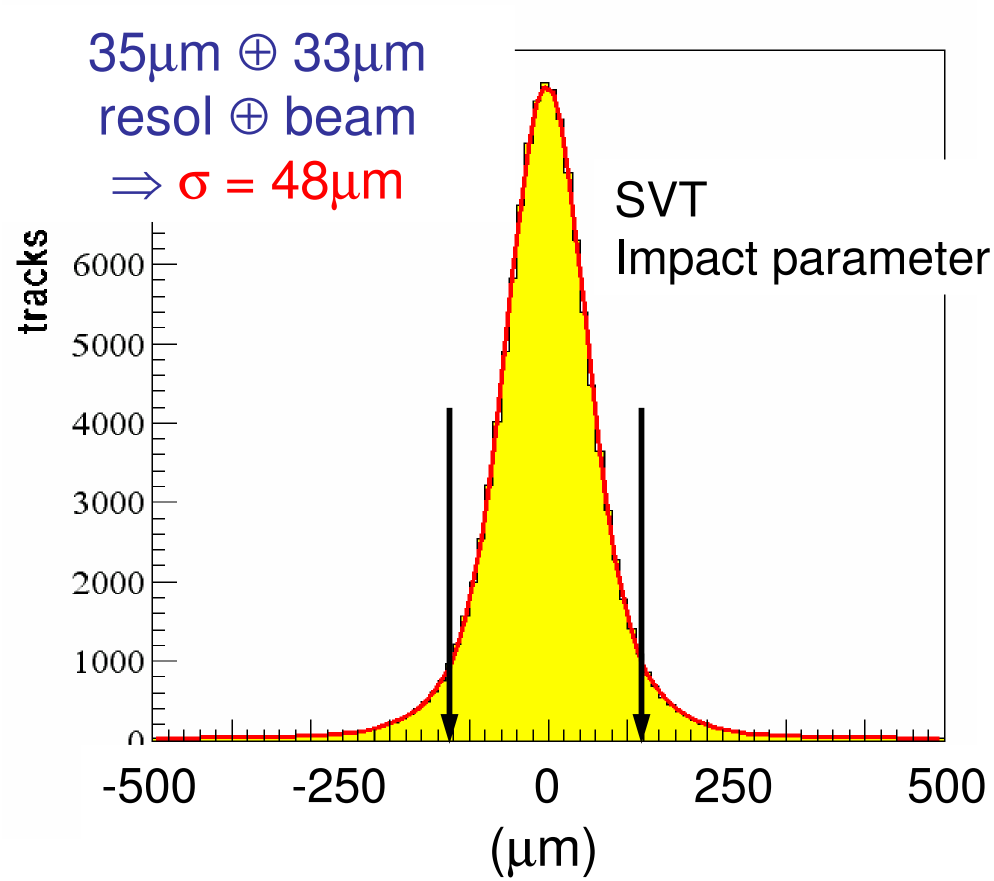
- The way we find tracks is a cross between
  - searching predefined roads
  - playing Bingo

The SVT Data Pipeline



Performance @ 50×10^{30} cm^{-2} s^{-1}

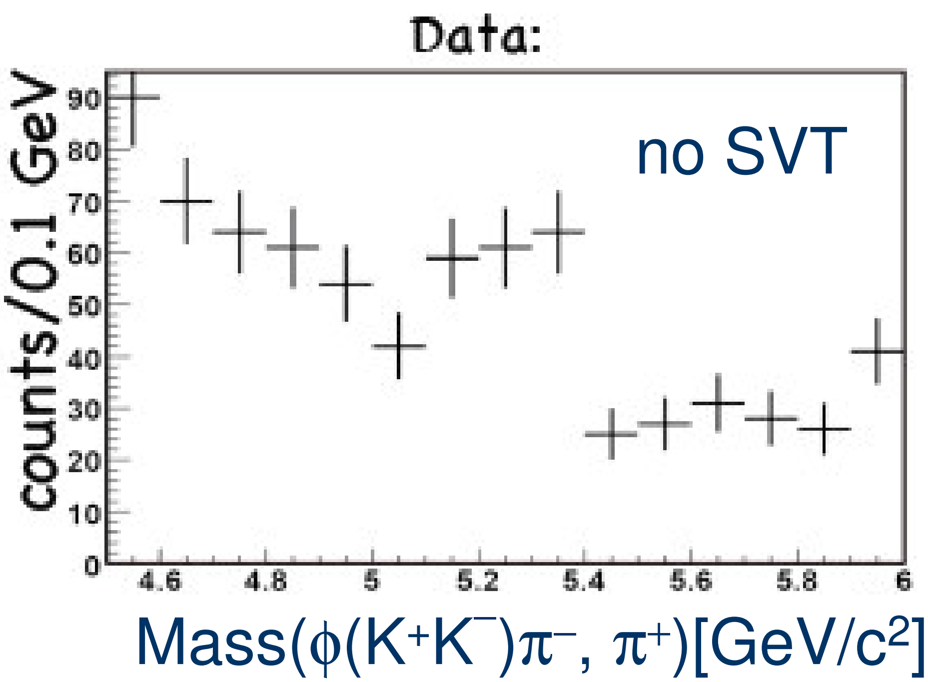


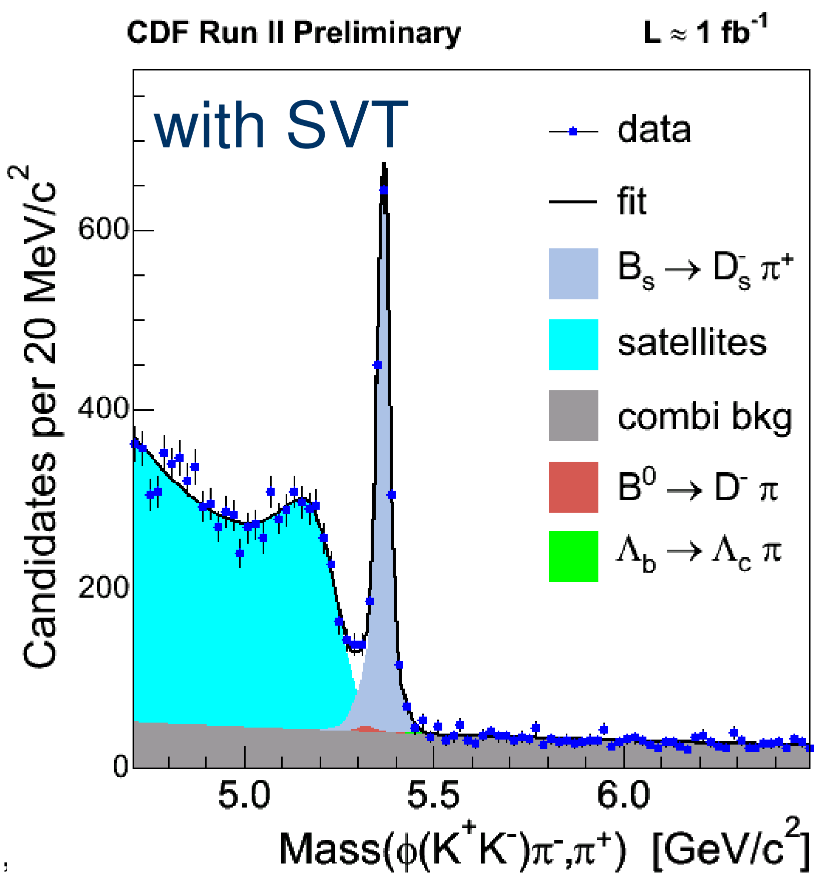


- efficiency ≃ 90% for
  - $p_T \geq 2$ GeV/c,
  - $|d_0| < 1$ mm

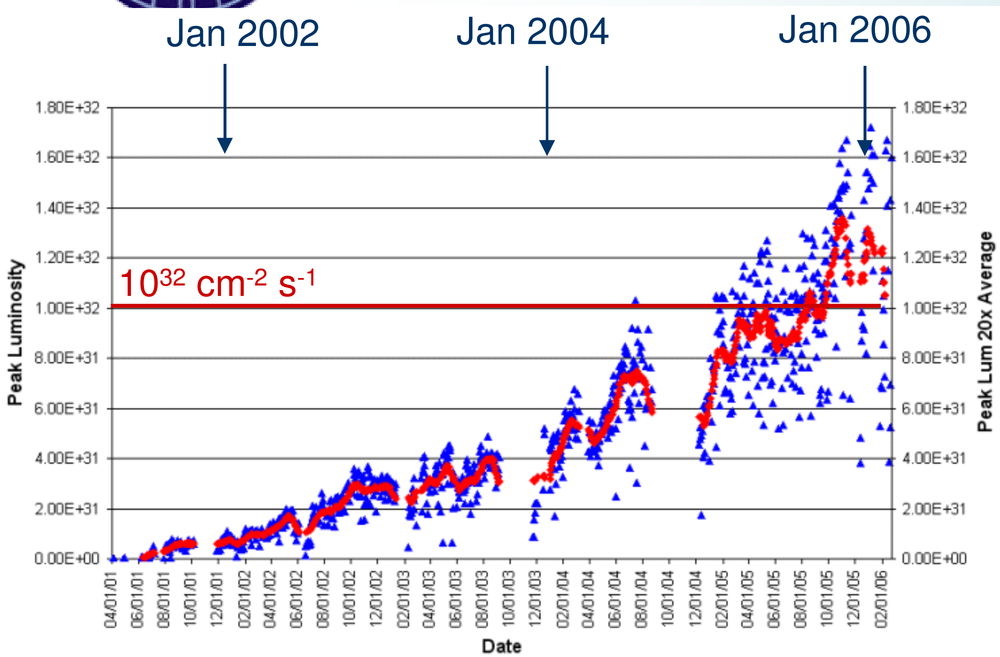
Results from SVT Triggers

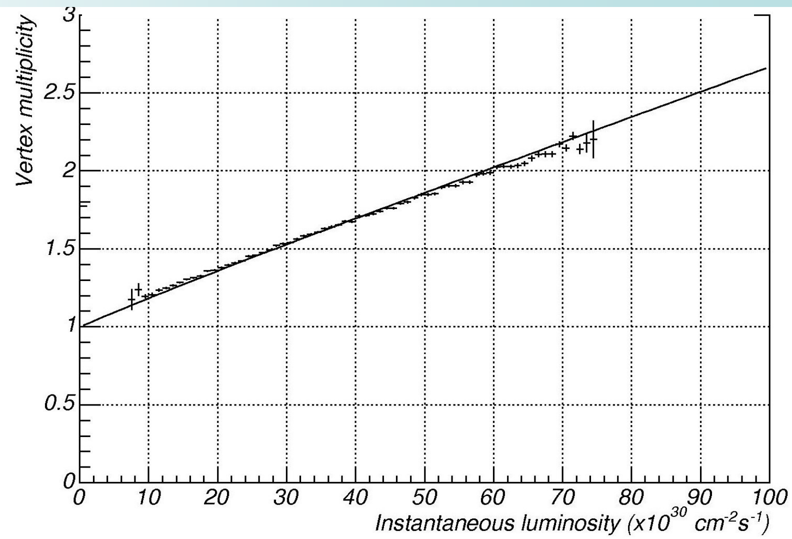
- 11/67 submitted CDF publications possible due to SVT
- not counting recent B_s mixing measurement
- significant power for B_s mixing measurement comes from hadronic $B_s \to D_s\pi$ decays



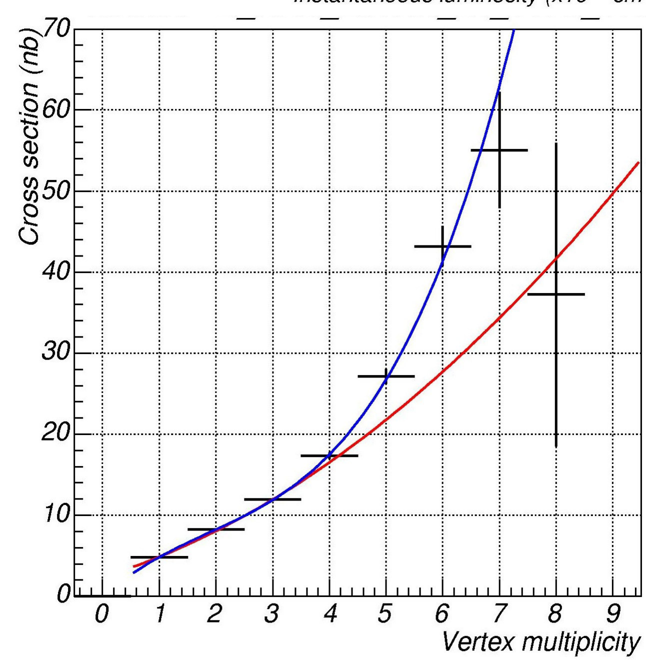


Why Upgrade?



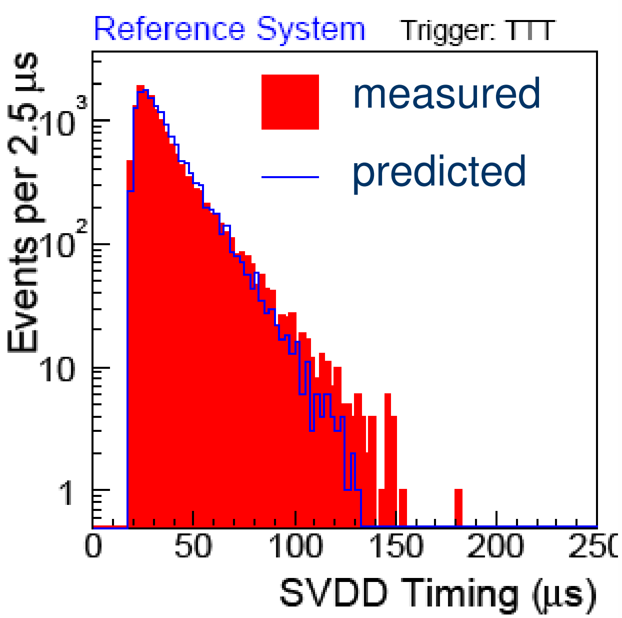


- fake rate ~ luminosity^n
- cut down rate of fake tracks
- increase number of patterns:
  - 32k pattern → 512k pattern



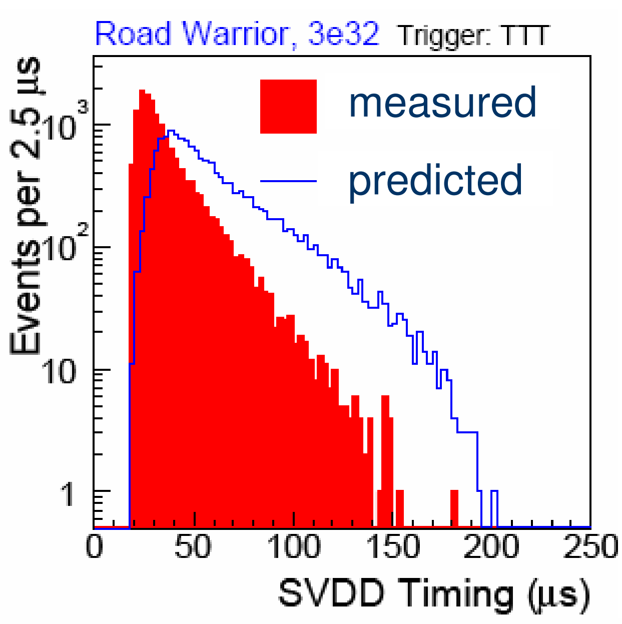
Timing at High Luminosity

low lum (50×10^{30})



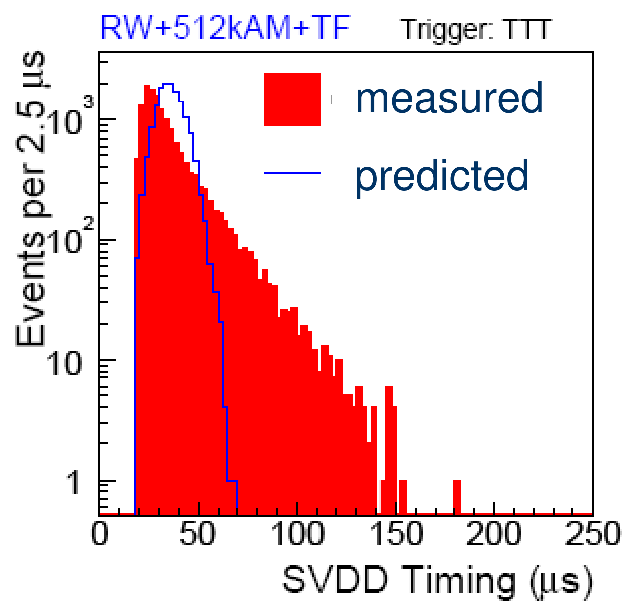
frac(t>50µs)~17%

no upgrade



frac(t>50µs)~57%

with upgrade



frac(t>50µs)~7%

- without upgrades, the SVT would cause significant dead time

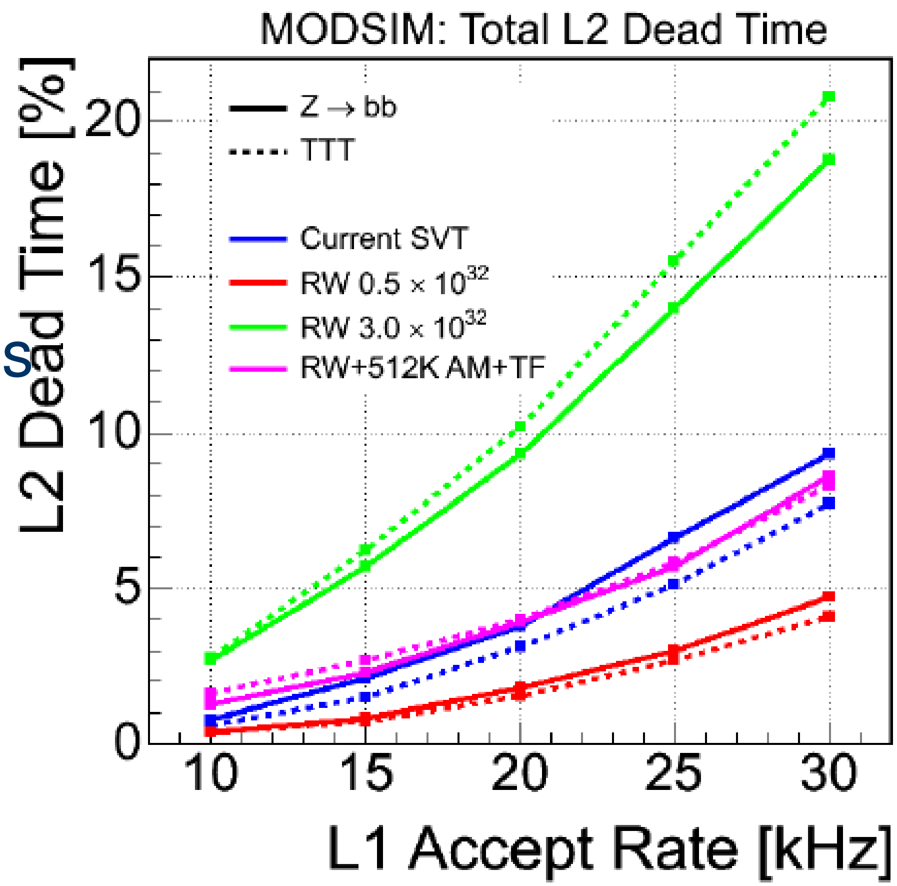
Upgrade Projects

- increase number of patterns
- upgrade to boards with faster clocks
- AM $\rightarrow$ AMS/RW, upgrade AM chip
- HB $\rightarrow$ HB++, use new board (Pulsar)
- TF $\rightarrow$ TF++, use new board (Pulsar)

Expected Performance

upgrade goal:

- maintain performance at high lum. (300×10^{30} cm^{-2}s^{-1})
- no increase in dead time
- no resolution or efficiency loss

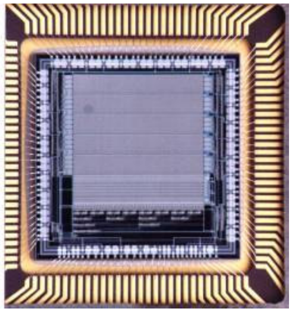


max. L1 rate, 300×10^{30} cm^{-2}s^{-1}
dead time $\leq$ 5%

Old SVT	Upgraded SVT
13 kHz	23 kHz

New AM chip

- Parallel pattern recognition is performed
  by the Associative Memory
  an array of AMchips
- Pattern recognition happens during detector readout!
- Standard Cell UMC 0.18 μm
  10×10 mm die - 5120 patterns (was 128)
  6 input hit buses (4Gbit/s)
  tested up to 40 MHz, simulated up to 50 MHz
- designed and developed at INFN Pisa
- more information: CDF Public Note 7339

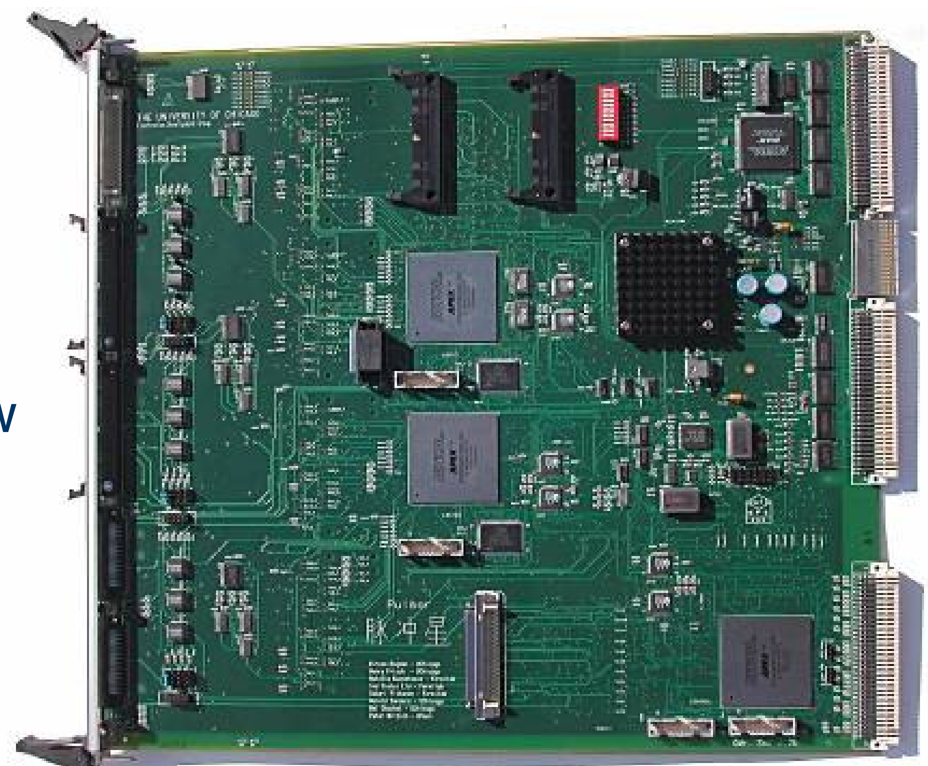


Original AM chip

Pulsar in upgraded SVT

The Pulsar board is a programmable board:

- 3 powerful FPGAs
- embedded RAM
- all CDF connectors
- modular mezzanines
  - RAM extension



Pulsar PCB, top side

- fast clocks [70 MHz] to handle data flow
- SVT interfaces built on board
- developers concentrate on firmware (= board functionalities)

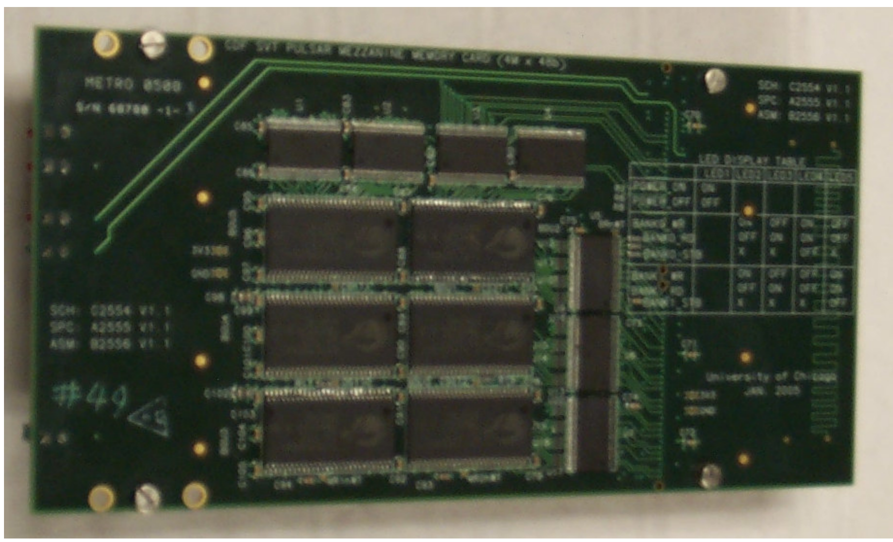
  - board design: Mircea Bogdan
  - Pulsar board documentation:

http://hep.uchicago.edu/~thliu/projects/Pulsar/Pulsar_hardware_design/

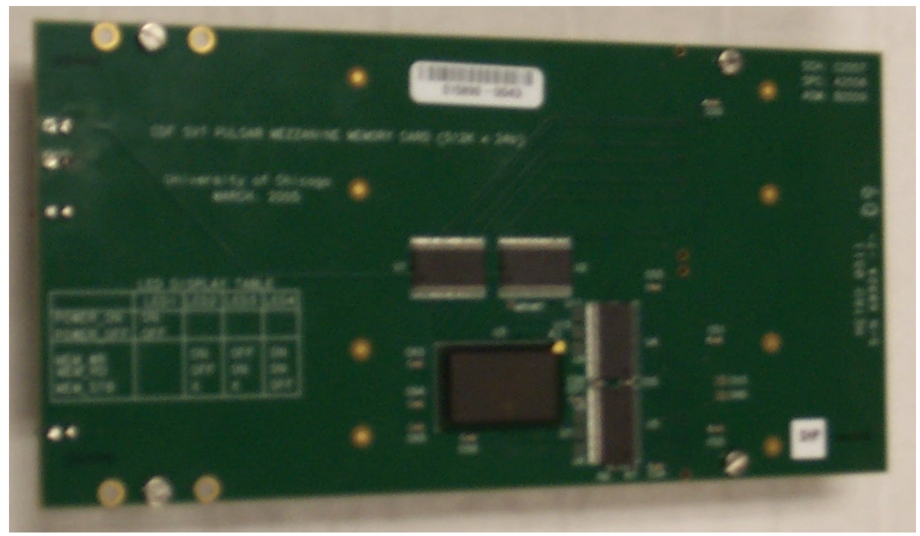
Mezzanine Memories

- provide memory capacity on Pulsar for pattern lookups

4M $\times$ 48 bits memory card



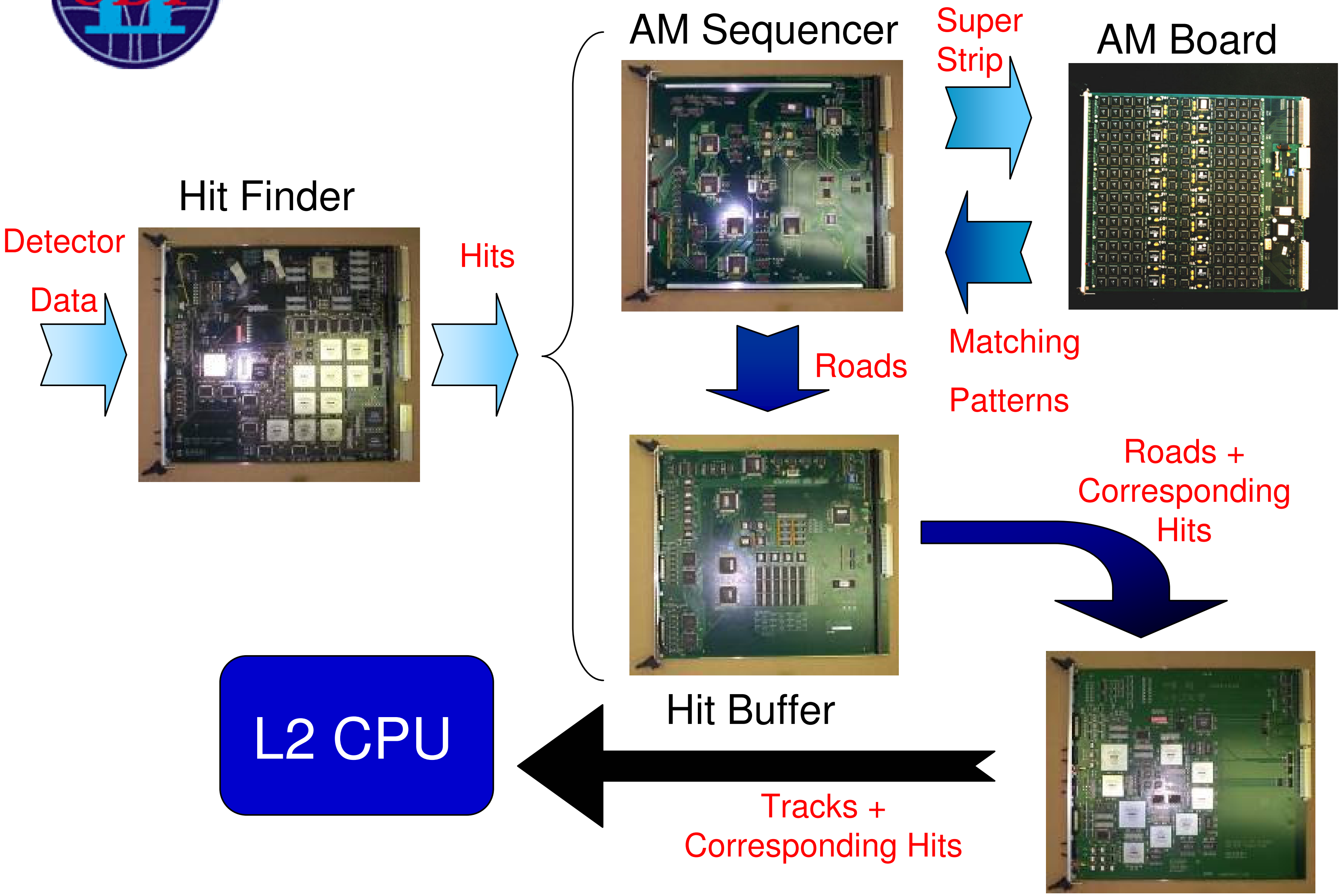
512K $\times$ 24 bits memory card



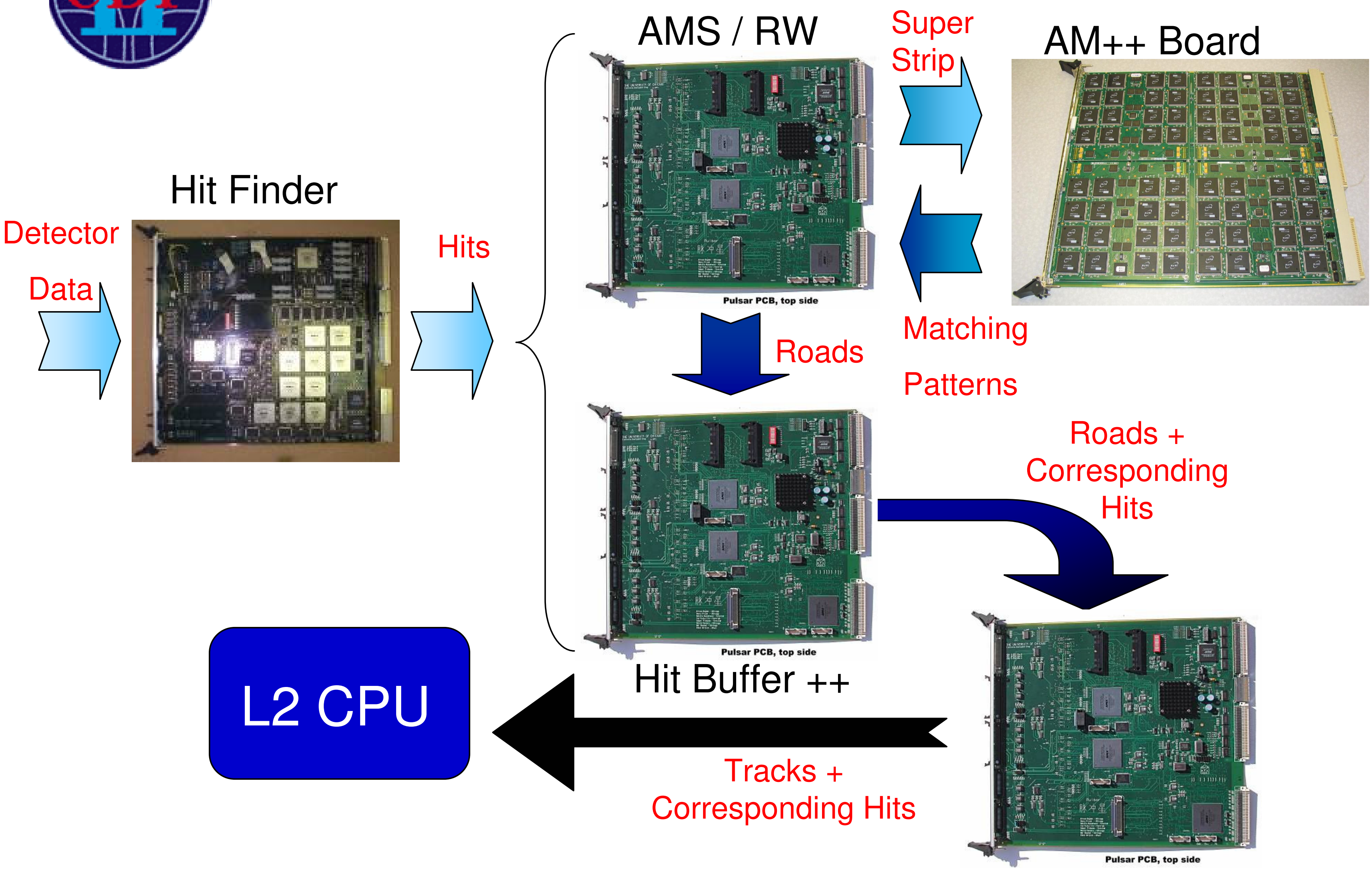
http://edg.uchicago.edu/~tang/Memory/sram_M4M.html

http://edg.uchicago.edu/~tang/Memory/sram_512K.html

The SVT Data Pipeline

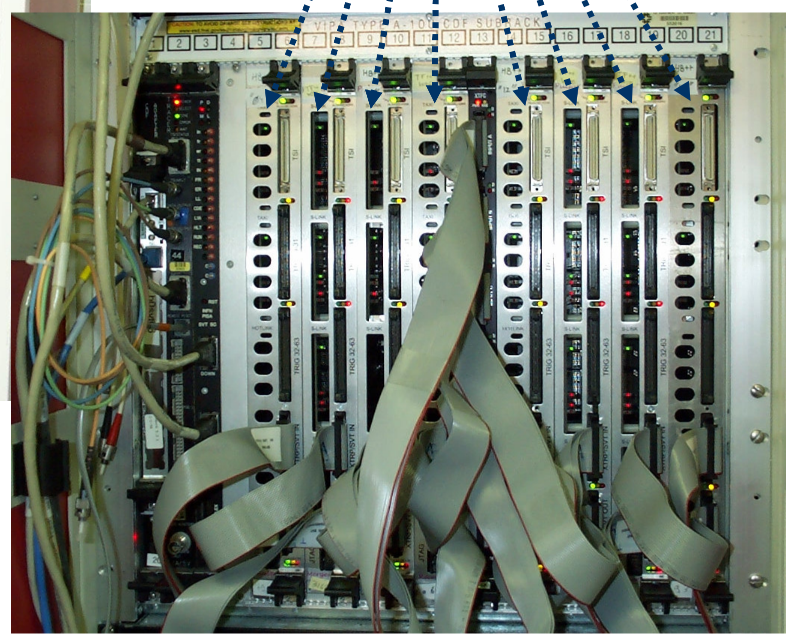


The SVT++ Data Pipeline



SVT crates in CDF counting room

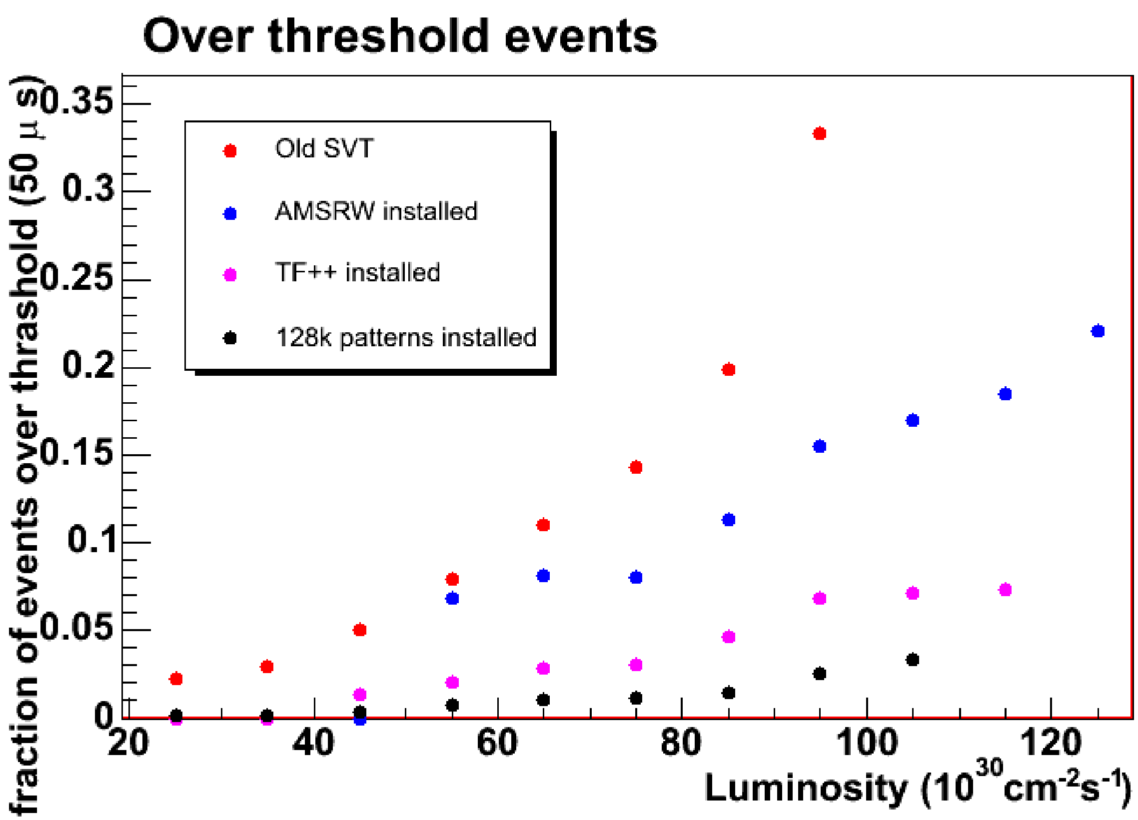
TF++, HB++
Pulsars



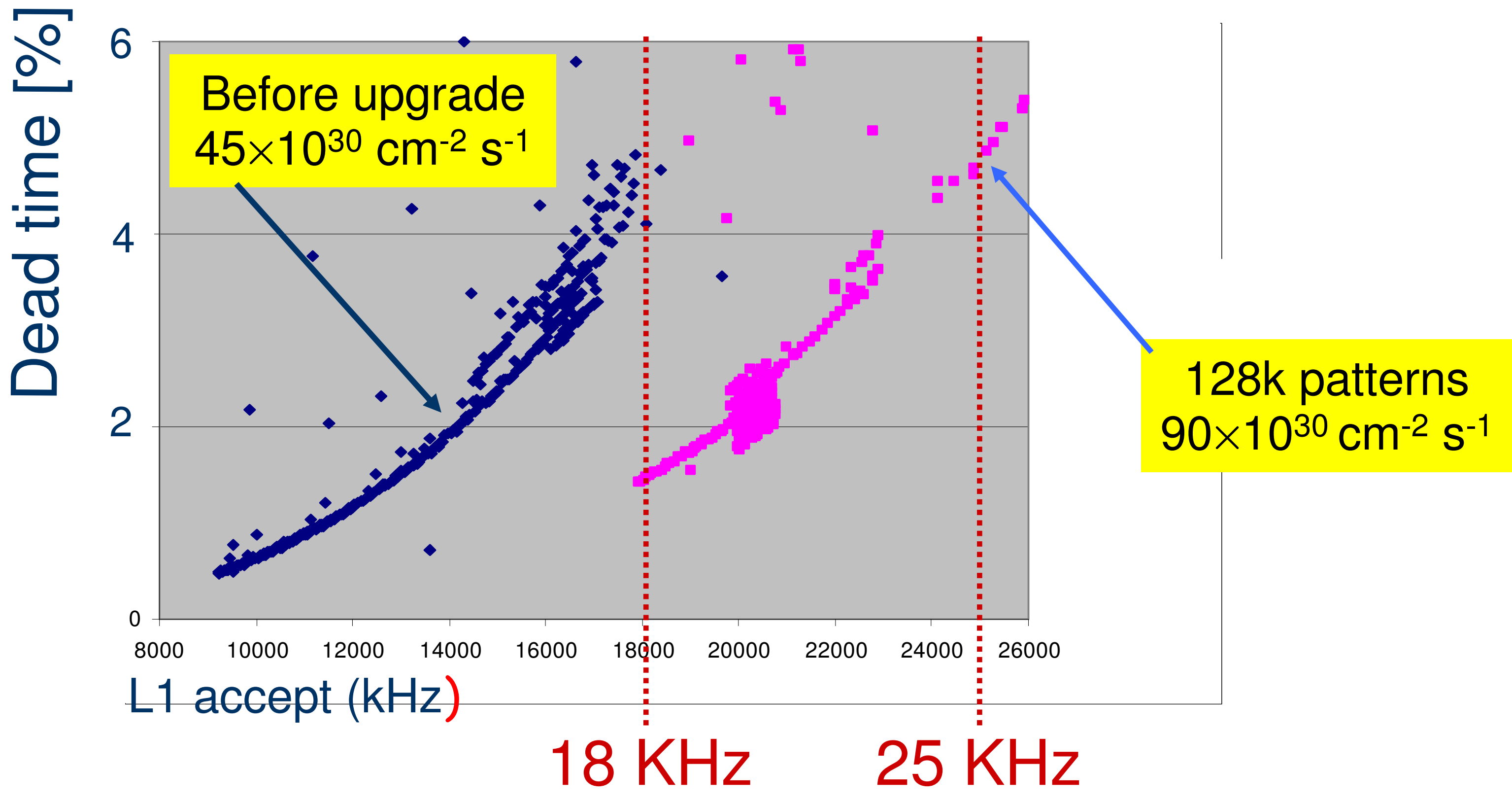
(+2 crates not in picture)

Timing with 128k patterns

- 1st stage: upgrade TF++, AM++ (128k patterns)
- completed ~ July 2005



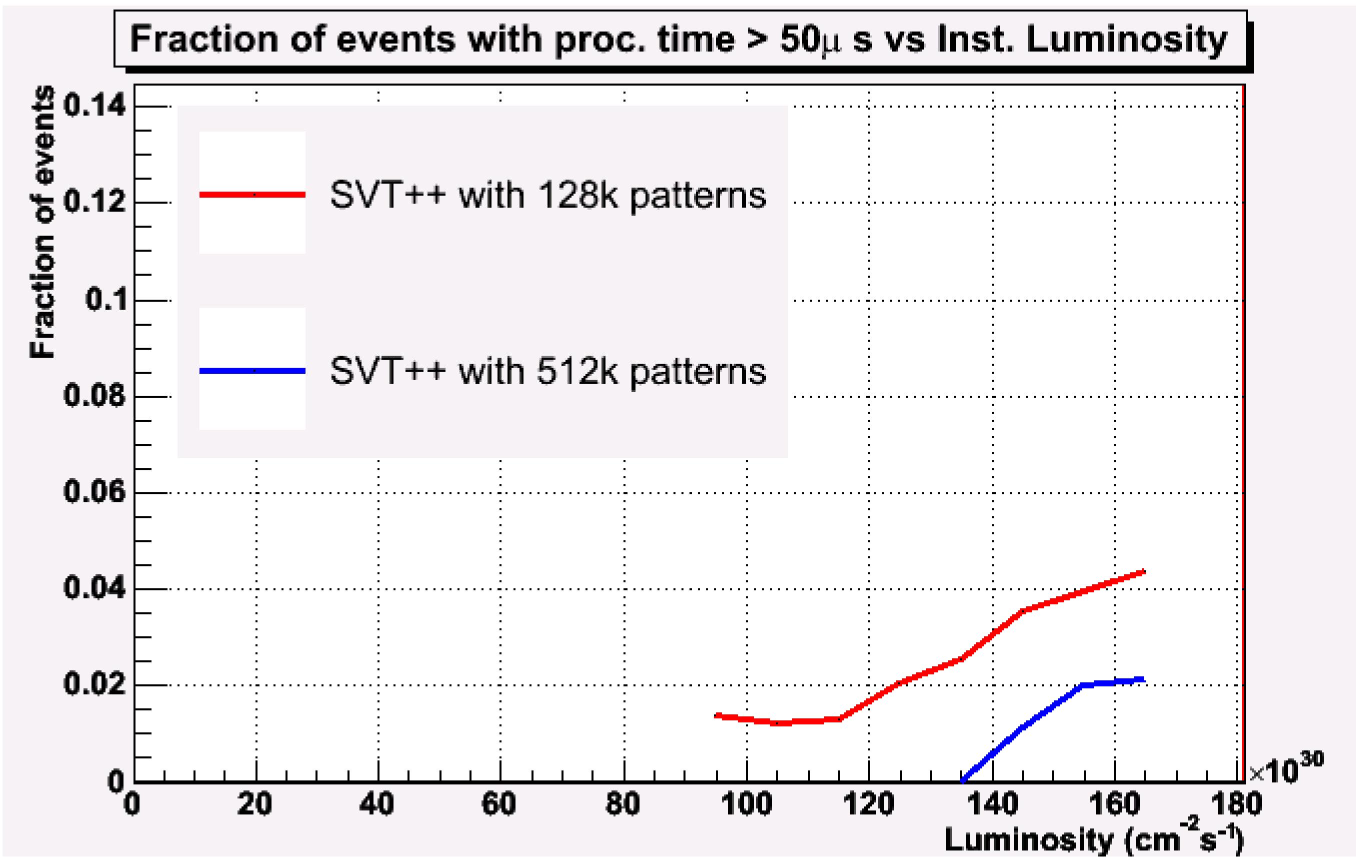
Dead time with 128k patterns



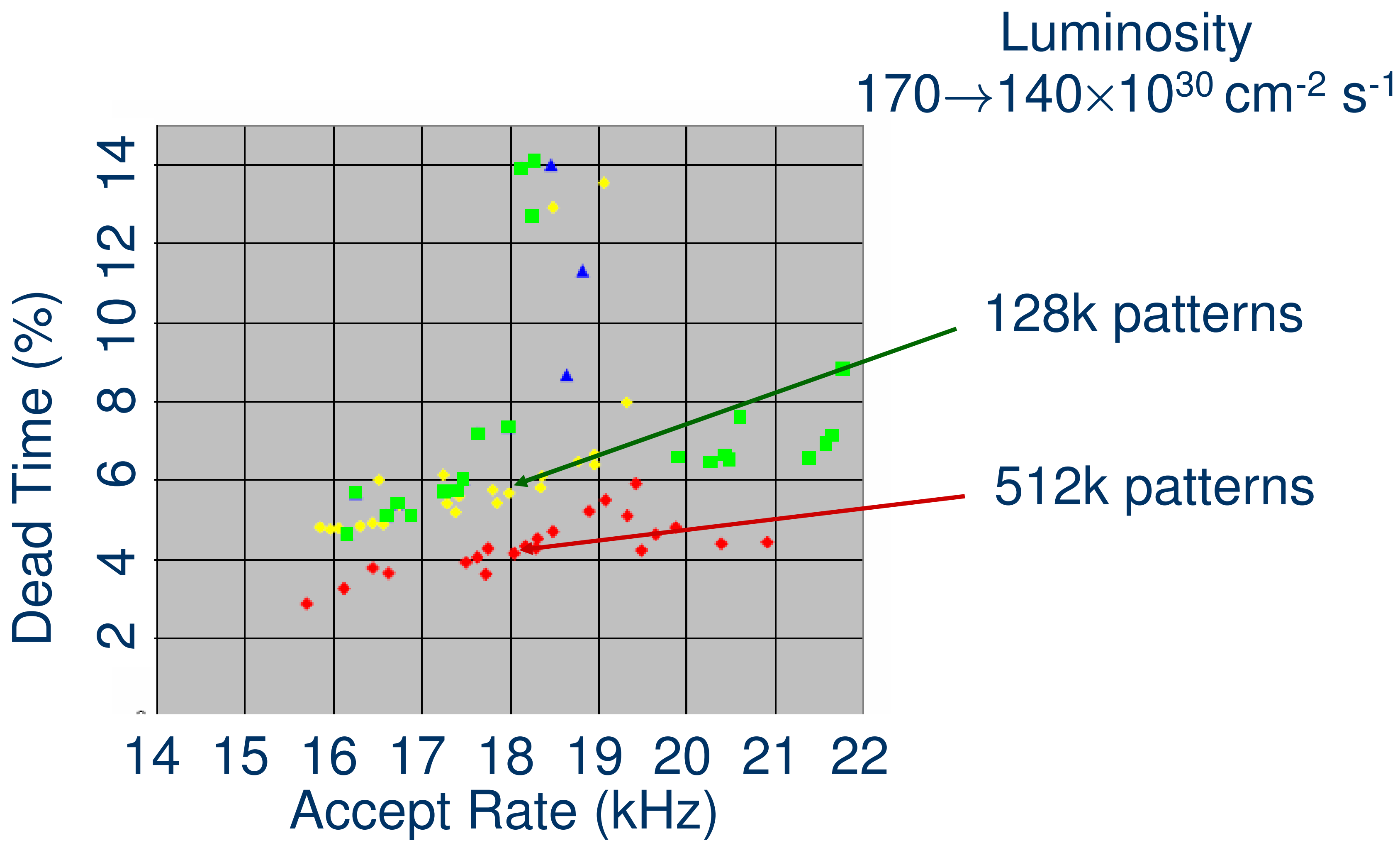
- new SVT operating at twice the luminosity, higher accept rate → same total dead time

Timing with 512k patterns

- 2^{nd} stage: HB $\rightarrow$ HB++, 512k patterns
- completed ~ Feb 2006



Dead time with 512k patterns



Conclusions

- SVT is a great success as part of the CDFII detector
- Tevatron luminosity is constantly increasing
- to cope with the higher data rates, SVT was upgraded

- new AM chip developed
- AM, HB, TF boards upgraded using multi-purpose Pulsar

- SVT upgrade successfully completed in < 2 years
- stay tuned for more excellent physics results!

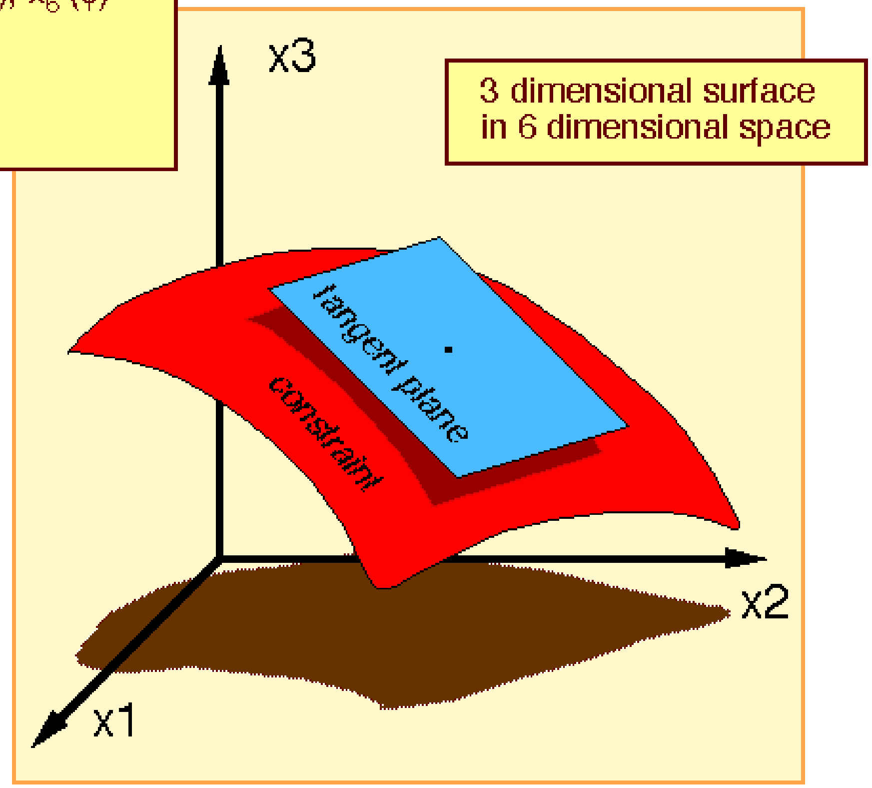
Backup

Constraint surface

6 coordinates: x_1, x_2, x_3, x_4, x_5 (P_T), x_6 (ϕ)

3 parameters to fit: P_T , ϕ , d

3 constraints



tangent plane:

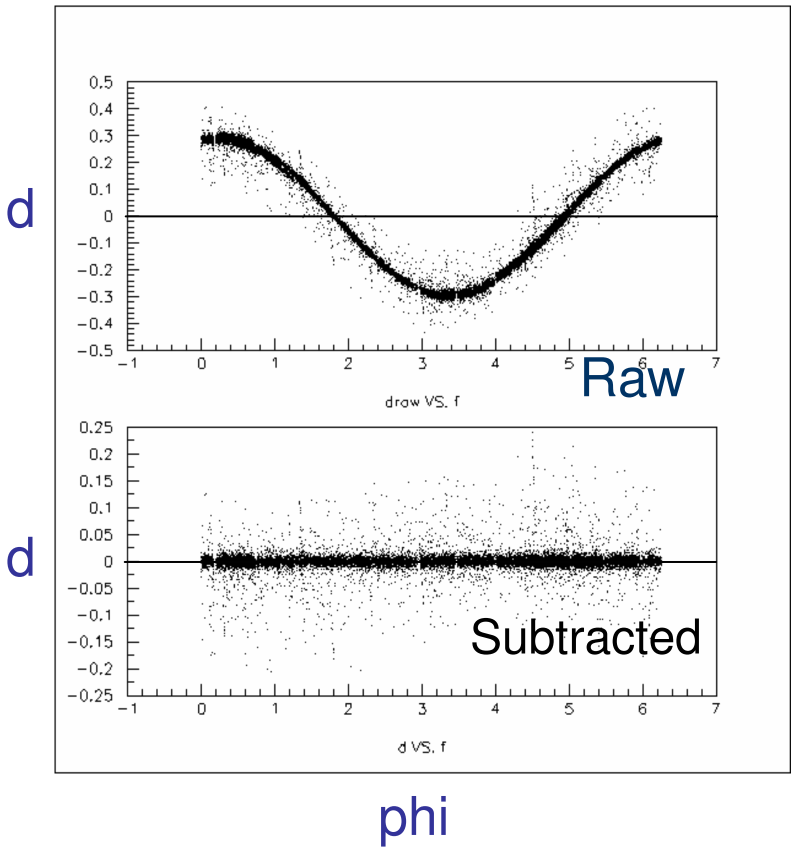
$$\sum_{1}^{6} a_i x_i = b$$

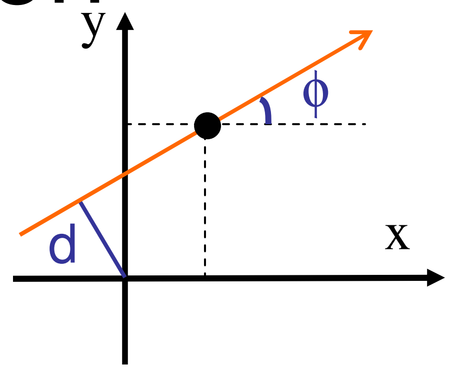
track parameters:

$$d \approx c_0 + \sum_{1}^{6} c_i x_i$$

Linear approximation is so good that a single set of constants is sufficient for a whole detector wedge (30° in ϕ)

Online beamline fit & correction





$\langle d \rangle = Y_{beam}\cos\phi - X_{beam}\sin\phi$